Ceramic Interconnect Technology Handbook

Edited by

Fred D. Barlow, III
Aicha Elshabini

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Dedication

To our families

Aicha Elshabini

Fred D. Barlow III

Preface

Ceramic interconnects includes a variety of technologies which have found widespread use in electronics for more than 50 years. The combination of electrical and mechanical properties that ceramics offer as well as the attractive features of many of the process technologies has made them a mainstay for a variety of applications. Historically, many of these applications have included aerospace, military systems, radar, power electronics, automotive electronics, and other harsh environment applications where the need for high operating frequencies, high power densities, or the need for operation at elevated temperatures made ceramics the logical choice. Today ceramics, and the related interconnect technologies, are still the best solution for many of these same applications, as well as a growing area of new applications such as wireless components and modules, Micro-Electro-Mechanical Systems (MEMS) packaging, and micro-fluidic devices.

This text is designed to be a comprehensive source of information regarding ceramic interconnect technologies and is intended as a reference book on the subject as well as an in-depth tutorial on the topic. Each chapter has been prepared by an expert in the field. In each case the authors are actively involved in the practice of each technology and in some cases were involved in developing the technology.

The book is composed of nine chapters, each of which covers a distinct aspect of ceramic interconnect technology. Chapter 1 provides an overview of the array of technologies that make up ceramic interconnects including, thick film, thin film, multi-layer ceramics, and direct bond copper. This chapter also provides a historical perspective and a set of examples of electrical applications that use ceramic interconnects. Chapter 2 addresses the design of ceramic products from an electrical perspective. This chapter also describes simulation and electrical testing. Thermo-mechanical design is addressed in Chapter 3. This chapter provides a detailed discussion of thermal design as well as mechanical stress and strain as it relates to electronics based on ceramic process technologies. Chapter 4 describes the common ceramic materials that are used in electronics today. An overview of these materials and there preparation is described as well as their electrical, thermal, and mechanical properties. Screen printing, which has been a cornerstone of ceramic technology for decades, is described in detail in Chapter 5. This chapter describes the materials, and processes that are used to produce thick film interconnects. Chapter 6 addresses the key subject of multilayer ceramics. This technology has been growing in market share due to its ability to fabricate a wide range of electrical functions in compact cost effective modules. Chapter 7 describes photo-defined and photo-imaged techniques

for fabrication of thick film interconnects. While screen printing is still the dominate method used to fabricate thick film interconnects, photo-defined and photo-imaged techniques are growing in popularity due to the ability to fabricate fine traces and structures that exceed the limits of screen printing technology. Chapter 8 provides a detailed discussion of copper interconnects that are used in conjunction with ceramic substrates. These technologies include thin film, plating, as well as direct bond copper (DBC) and active metal braze (AMB) methods. Chapter 9 provides a comprehensive discussion of integrated passive components including design, fabrication, and trimming methods.

Editors

Fred Barlow is an associate professor of electrical engineering at the University of Idaho. He earned a Bachelor of Science in physics and applied physics from Emory University, and his Master of Science and Ph.D. in electrical engineering from Virginia Tech. Dr. Barlow has published widely on electronic packaging and is co-editor of *The Handbook of Thin Film Technology* (McGraw Hill, 1998). In addition, he has written several book chapters on thin films, packaging, and components and devices. His research interests include electronic packaging for power electronics, high temperature applications, as well as for microwave and millimeter wave systems. He currently serves as the editor-in-chief of the *Journal of Microelectronics and Electronic Packaging*.

Aicha Elshabini is the dean of engineering at University of Idaho. She is a professor of electrical and computer engineering and was named a distinguished professor of electrical engineering in 2003. She served as department head of electrical engineering at University of Arkansas from 1999–2006. She also served in the Bradley Department of Electrical and Computer Engineering Department at Virginia Tech from 1979–1999. She obtained a Bachelor of Science degree in Electrical Engineering at Cairo University, Egypt in 1973 in both electronics and communications areas, a Master's degree in electrical engineering at the University of Toledo in 1975 in microelectronics, and a Ph.D. degree in electrical engineering at the University of Colorado, at Boulder in 1978 in semiconductor devices and microelectronics. She is a fellow member of IEEE/CPMT Society (1993) Citation for 'Contribution to The Hybrid Microelectronics Education and to Hybrid Microelectronics to Microwave Applications', a fellow member of IMAPS Society (1993), The International Microelectronics and Packaging Society, Citation for 'Continuous Contribution to Microelectronics and Microelectronics Industries for numerous years'. Dr. Elshabini was awarded the 1996 John A. Wagnon Technical Achievements Award and the 2006 Daniel C. Hughes Jr. Memorial Award for lifetime achievement in microelectronics from The International Microelectronics and Packaging Society (IMAPS).

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Aicha Elshabini, Gangqiang Wang, and Dan Amey

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1.1 Ceramics in Electronic Packaging

1.1.1 Introduction and History

Modern ceramic substrates and packages are sophisticated combinations of glasses, ceramics, and metals that can form compact cost-effective solutions for a variety of applications. Because of the unique sintering process used to fabricate these materials, a wide range of conductors, dielectrics, resistive materials, and even magnetic materials can easily be incorporated into a given ceramic body. In addition, many of the ceramic interconnect technologies used today are inherently multilayer in approach and provide tremendous design flexibility for high-density circuitry. Ceramics are widely used as thick-film substrates, thin-film substrates, insulators, dielectrics, and/or structures that are capable of withstanding temperatures up to 1000°C.

Ceramic materials have a long successful history of application in the electronics industry. Ceramics were the first type of insulating base material for modern mass-produced circuitry. Disclosure of their World War II use in a miniature radio proximity fuse [1,2] spurred the development of ceramic-based circuits and culminated in the early 1950s in a modular three-dimensional concept of circuitry as we know it today. The use of thick-film metallization, or silver "paint" as it was then called, was in use in electronic capacitors in volume production for consumer applications in the early 1950s. Even then, the size, cost, and high-frequency advantages were evident. It took much longer (into the late 1960s), but ceramic interconnect technology continued to stay at the forefront of electronic packaging applications offering the same advantages — cost-effective high density, environmental performance, reliability, and quick turnaround — which continue to be the primary advantages in the choice of ceramic technology. Table 1.1 summarizes the key characteristics of ceramic interconnect technologies [3].

1.1.2 Functions of Ceramic Substrate

The function of the substrate is to provide the base onto which thin-film circuits and/or thick-film circuits, which make up the electrical circuits, are fabricated and various multilayer films are deposited. In addition, the substrate provides the necessary mechanical support and rigidity needed to produce a reliable functional circuit. It must have adequate thermal management ability to ensure proper temperature operation, and it must possess a proper electrical insulation to withstand circuit voltages without breakdown. One can think of the substrate as the foundation on which the circuit traces and components are mounted and supported. Ceramic materials are often used for thin- and thick-film applications, because ceramics have high thermal conductivity, good chemical stability, and are also resistant to thermal and mechanical shock [4].

TABLE 1.1

Characteristics of Ceramic Interconnect Technologies

Characteristics	Thick Film	Thin Film	Multilayer Ceramic	Direct Bonded Copper
Substrate size XY (mm)	127–150	127–150	125–225	127–175
Z thickness (mm)	0.6–1.2	0.6–1.2	0.5–3.25	Copper 0.175–0.5
Number of layers	1–6	2–4	25	Double side
Line width (μm)	125	25	50–150	>175
Line pitch (μm)	250	50	100–300	>35
Via diameter (μm)	250	20	100–200	
Via pitch (μm)	500	50	225–625	
Resistor (Ohm/sq.)	10, 100, 1k, 10k, 100k	10–350	LTCC 10, 100, 1k, 10k	
Capacitor (pF/mm²)	400	10–300, up to nF	LTCC 100	

Source: Imhof, H. and Schless, T., 2004 IMAPS-CII/NEMI Technology Roadmaps: Interconnection Substrates — Ceramic, January 2005, http://www.imaps.org/cii/cii_roadmap_2004.pdf.

1.1.3   Ceramic Advantages and Limitations

Ceramic materials offer desirable mechanical and electrical properties for electronics applications. Compared to other crystalline materials, ceramics possess high modulus of elasticity and are rigid materials to ensure minimum distortion under high-loading and high-temperature conditions, a higher compressive strength than alloy steel, and a higher tensile strength than porcelain. In addition, they offer higher strength than glass, extremely high dimensional stability, low differential magnitudes of thermal expansion, high electrical resistivity over broad temperature ranges, and high chemical inertness relative to various processing and operating conditions.

Ceramic substrates are essentially metal oxides or nitrides, and are often mixed with glasses and fired at an elevated temperature. This results in a hard and brittle structure possessing many desired characteristics. Ceramic materials possess high mechanical strength and low thermal expansion to withstand operating conditions; high electrical resistivity over a wide temperature range with adequate dielectric strength to withstand applied voltage without dielectric breakdown; high chemical inertness to most chemicals and etchants; relatively low dielectric constant and low dissipation factor to avoid capacitance effect and electrical losses; and high thermal conductivity and a higher tolerance to temperature extremes to allow proper thermal management [5]. These substrate materials possess specific mechanical parameters (measured in terms of compression strength, tensile strength, modulus of elasticity, dimensional stability, flexural strength, and thermal coefficient of expansion), physical parameters (measured in terms of camber, surface finish, specific gravity, and water absorption), chemical parameters (measured in terms of materials compatibility and chemical reactivity),

electrical parameters (measured in terms of dielectric constant, dissipation factor, resistivity, and dielectric strength), and thermal parameters (measured in terms of thermal conductivity).

Conventional thick-film technology is a sequential process necessitating artwork, stencil, deposition or printing, and firing each layer separately at temperatures exceeding 800°C. There is also a limit on the number of layers to be produced. Although passive components can be readily fabricated, the values of these components produced are not of tight tolerance, and trimming is often necessary to bring them to the desired values.

1.1.4 Ceramic Compositions

Ceramic materials commonly used for substrate applications require temperatures on the order of 850 to 1900°C for their fabrication, thus becoming naturally immune to lower-temperature processing [5–8]. Basic ceramic compositions include electrical porcelain (50% clay [$Al_2Si_2O_5(OH)_4$] and 25% each of flint, SiO_2 and feldspar [$KAlSi_3O_8$]), steatite (commercial steatite compositions are based on 90% talc [$Mg_3Si_4O_{10}(OH)_2$] plus 10% clay), cordierite ($Mg_2Al_4Si_5O_{18}$, useful for high-temperature applications), forsterite (Mg_2SiO_4), alumina or aluminum oxide (Al_2O_3), beryllia or beryllium oxide (BeO), magnesia (MgO), zirconia (ZrO_2), and aluminum nitride (AlN). High-alumina porcelains have a great tolerance for compositional variations, and because the dielectric constant does not vary through a wide range of temperatures, they are of most interest in electronic device applications (–50°C to +250°C). Steatite porcelains (with electrical properties varying at low frequencies) are low-loss materials commonly used as components for variable capacitors, coil forms, and general structure insulation.

Cordierites possess a low thermal expansion coefficient and, consequently, high thermal shock resistance. Forsterites have a higher resistivity and a lower electric loss with increasing temperature owing to the absence of alkali ions in the vitreous phase. Beryllia or beryllium oxide is stable in air, vacuum, hydrogen, carbon monoxide, argon, and nitrogen at temperatures up to 1700°C. Magnesia is suitable for insulating thermocouple leads and for heating core elements. Alumina, beryllia, AlN, and silicon carbide (SiC) are common ceramic substrates.

1.1.5 Ceramic Substrate Manufacturing

High-purity powders are processed through ball milling to the proper particle size [9–17]. Organic binders, solvents, plasticizers, and other additives are added to provide stability, packing density, and grain uniformity to the mixture to achieve a specific paste rheology for the material to flow freely during processing, maintaining cohesiveness and uniform characteristics. The mixture is either powder-pressed to final shape to form a compacted tape, then subjected to a heat treatment to sinter the material, or a sheet with

```
                          Grind
                            |
                           Mix
                            |
                          Form
                            |
   ┌────────────────────────┼────────────────────────┐
   |                  Plastic form                     |
Powder press          extrude, roll,               Sheet cast
to final shape           emboss
   |                        |                          |
   |                       Dry                         |
   |                        |                          |
  Dry              Punch to shape
   |                        |
   └────────────────────────┤
                            |
                   Low temperature
                   prefire to remove
                   organic binders
                            |
                   High Temperature
                      Sintering
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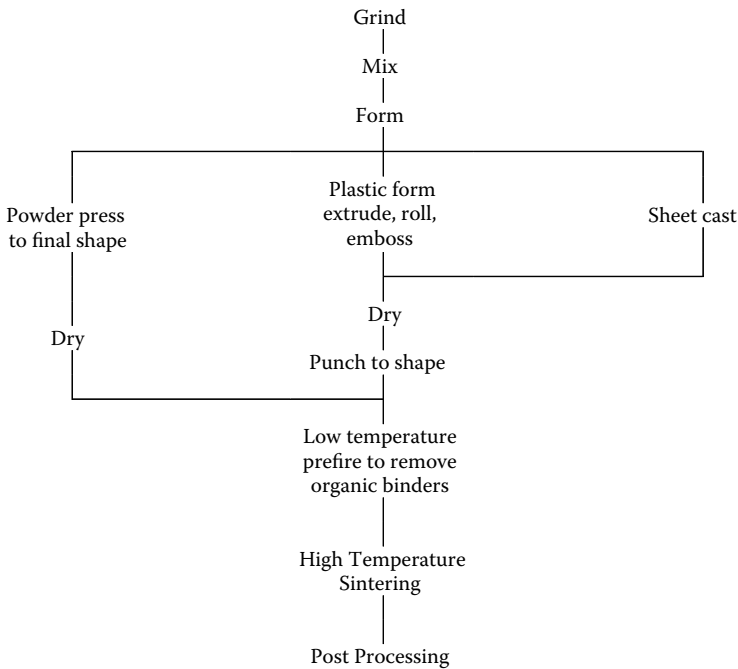
FIGURE 1.1
Ceramic substrate manufacturing.

a uniform thickness is cast through a slurry flowing with a knife edge suspended above a film carrier at the desired tape thickness, and then dried and punched to shape, followed by a heat treatment to sinter the material. The sheet can also be cast through extrusion forcing the material in fluid form to pass through a die. The oxide powder is often prefired at 300–900°C to remove most of the organic additives (about 99.9%). Sintering takes place by firing at higher temperatures to remove the plasticizers, any remaining organic binders, and the additives, resulting in material shrinkage and densification of the tiny particle aggregates. Recrystallization of these fine homogeneous grains will occur while passing through the liquid phase of the material at these high temperatures, resulting in a strong substrate with a good smooth surface. Figure 1.1 depicts typical manufacturing processes.

1.2 Electrical Properties of Ceramic Substrates

Electrical parameters of interest for the ceramic substrates include volume resistivity, dielectric constant, dissipation factor, and dielectric strength

[18–20]. These parameters may be critical under certain operating conditions, such as high frequency and/or high voltage. The electrical resistivity in ohm-cm is a measure of the resistance a material would offer to the current flow in an applied DC field. Usually, the resistivity is high in values exceeding 10^{14} Ω·cm for most ceramic substrates at room temperature and operating over a broad range of temperatures. As the temperature increases, one would notice a sharp decline in the electrical resistivity of these ceramics reaching 10^6 Ω·cm at 1000°C.

The dielectric constant K is the measure of the ability of the material to store the electric charge relative to vacuum, a dimensionless quantity. The dielectric constant value of ceramics varies at room temperature in the range from 5.5 to well above 10, depending on the type of ceramic (i.e., composition), the temperature and the frequency of operation, the particle size, and the purity of the material. The K values increase upon temperature increase for most ceramics. Often, dielectric constant values are provided with measurements conducted at 1 MHz. Measurements also indicate a strong dependence of the dielectric constant value on the frequency of operation; a decline in K is often observed upon a frequency increase. Often, a low dielectric constant is desired to avoid capacitance effect. Typical values of K are 9.7, 6.8, 9.9, and 40, for conventional alumina, beryllia, AlN, and silicon carbide, respectively.

The dissipation factor (DF), or dielectric loss, or loss tangent (tan δ) is a measure of the real or resistive component of a capacitor, and it does determine the energy loss from the material per cycle in the form of heat. With alternating voltages, the charge stored on the dielectric surface has both an in-phase or real component and an out-of-phase or imaginary component, caused by dielectric absorption or resistive leakage. DF is of the form

$$DF = \tan \delta = R_s \, \omega \, C_s = \varepsilon''/\varepsilon'$$

where $\omega = 2 \, \pi \, f$, f is the frequency, R_s is the series resistance, and $1/\omega \, C_s$ is the capacitive reactance. $\in''$ and $\in'$ are the imaginary and the real components of the complex permittivity ε^*, that is $\varepsilon^* = \in' - i \in''$. A low dissipation factor is desired to avoid excessive dielectric losses. The dissipation factor is of the order 0.0001, 0.0012, 0.005, and 0.05% for Al_2O_3, BeO, AlN, and SiC, respectively. The dissipation factor tan δ varies from 0.0014% for 75% aluminum oxide to 0.00022% for 99% aluminum oxide.

The dielectric strength of ceramics in V/mm (or voltage per unit length in general) varies considerably as a function of temperature, frequency, and the material's physical properties (such as density, porosity, purity, and physical dimensions of the ceramic sample). A sharp decline of the dielectric strength of ceramics is experienced upon an increase of frequency and/or temperature. Adequate dielectric strength is needed to withstand an applied voltage without breakdown. Dielectric strength of ≥ 15 KV/mm has been observed for most ceramics (26–24 for Al_2O_3, 9.5 for BeO, and 10–14 for AlN).

1.3   Mechanical and Physical Properties of Ceramic Substrates

Mechanical properties of ceramics include mechanical strength and thermal expansion properties. Ceramics, which are brittle materials, must tolerate processing, operation, handling, or storage fatigue, stresses, and microcracking. Failures are most common along the edges of the substrate perimeter. These stresses can often be relieved with an annealing process. Mechanical failure can be aggravated by a rise in temperature. Due to the brittle nature of ceramics, specific mechanical testing is recommended, such as the Young's modulus, the compression strength, the tensile strength, the thermal coefficient of expansion, the dimensional stability, and the thermal shock failure mechanisms.

The ceramic surface finish is a function of the microgranular structure and the density of the ceramic–glass composite. Small grains, in as-fired ceramic structures, form a smooth surface, and are mainly used for thin-film or fine-line thick-film applications. The centerline average (CLA) is a measure of ceramic surface requirement, 0.381–1 µm (15–40 µin.) for thick-film surface requirement, and 0.127 µm (5 µin.) and less for thin-film surface requirement. It is important to realize that the glass inclusion degrades both the electrical and the thermal properties of the ceramic substrates.

Camber (µm/mm) is defined as the overall deviation from one side of the substrate to the other side as measured along the diagonal of the surface. Substrates 635 µm (25 mil) thick with 1–3 µm/mm (1–3 mil/in.) camber are available as standard. AlN substrates may possess a camber less than 3 µm/mm. The specific gravity is the ratio of the material density to that of the water density.

Table 1.2 lists the mechanical and physical properties of some ceramics at room-temperature operation [3,21].

1.4   Design Rules

The design rules used for a given substrate fabrication will vary from one fabrication facility to another due to variations in the process equipment used and the material set employed. However, some general guidelines are presented here to provide a context for the capabilities of the technology. In general, a number of key geometries must be limited by the ranges of what can be achieved in mass production. These geometries include the conductor width, the conductor spacing, the via size, and the via pitch, just to name a few. Table 1.3 summarizes some of the key design rules and gives representative examples of the ranges one would normally find at a production house. The values are broken into two sets labeled "conventional" and "advanced,"

TABLE 1.2

Mechanical and Physical Properties of Some Ceramics at Room Temperature

Parameter	Alumina Al$_2$O$_3$	Beryllia BeO	Aluminum Nitride AlN	Silicon Carbide SiC
Young's modulus (GPa)	360[a]	350	340	400
Compression strength (Ksi)	290–380[a]			
Tensile strength	17–35 Ksi or 17,000– 35,000 lb/in.^{2}			
Flexural strength	43,000–55,000 (lb/in.^{2}) or 250–400 N/mm^2	>250 MPa or 170–240 N/mm^2	>300 MPa or 280–320 N/mm^2	—
Thermal coefficient of expansion[b] TCE (ppm/°C)	5.3–6.7[a]	6.9	2.7–4.1[a]; silicon is 2.6; GaAs is 5.7; T 25–200°C	3.7
Coefficient of thermal endurance F (representing thermal shock resistance)	3.7 (0.9 for glass and 13.0 for silica)	3.0	4.6	3.7
Thermal conductivity (W/m·K)	20–35[c]	250	160–190[a]	270
Density (Kg/m^3) or (g/cm^3)	3.8–3.9[a]	2.9–3.0	3.28–3.3[a]	3.1–3.2
Surface finish (µm/m)	2.5–3	5 µin. maximum	<0.6 µm <25 µin.	
Dielectric strength (kV/mm)	18	>26	>15	0.07
Dielectric strain (V/mil), 25 mil thick	240–210[a]			
Camber	0.002 in./in. for 10 mil, 0.003 in./in. for 25 mil, and 0.004 in./in. for 40 mil	< 0.003 in./ in.	< 0.0025 in./ in.	—

[a] As the purity of material increases (and/or increase in alumina content), the value increases.
[b] The thermal coefficient of expansion of a given material is the slope of the linear thermal expansion vs. temperature. The differential magnitudes of thermal expansion between two materials are considered key design parameters and should be kept to a minimum.
[c] Increases with wt% of aluminum oxide, with 96% alumina being considered as standard.

respectively. The conventional design guidelines fall within the capabilities of virtually all manufacturers, whereas the advanced guidelines are only available from a smaller number of manufacturers.

TABLE 1.3

Summary of Typical Ceramic Design Rules

Parameters	Standard	Custom
Maximum substrate size (fired)	6 × 6 in.	6 × 6 in., or
		8 × 8 in.
Number of layers	<15	> 15
Layer thickness	0.010–0.025 in.	0.002–0.010 in.
Tolerances		
Length and width	±0.8%, or ±2 mil	±0.5%, or ±1 mil
Thickness	±10%, or ±2 mil	±5%, or ±1 mil
Chamber	3 mil/in.	1 mil/in.
Conductor width	0.007 in. minimum	0.004 in. minimum
Conductor spacing	0.007 in. minimum	0.004 in. minimum
Via diameter	0.007 in. nominal	0.005 in. nominal
Via cover pad	0.014 in.	0.006 in.
Via center to center	0.024 in.	0.010 in.
Via center to center (with one conductor)	0.034 in.	0.020 in.
Sheet resistivity	0.012 Ω/□	0.008 Ω/□
Via hole resistance	0.010 Ω/□	0.005 Ω/□

Note: One square (□) is equivalent to any given square area of conductor.

1.5 Thick Films on Ceramics

1.5.1 Introduction and Background

Ceramic substrates provide the base onto which all thick-film circuits are fabricated. Ceramic materials are used in substrate applications primarily because of their high mechanical strength, high electrical resistivity over a broad temperature range, and chemical inertness relative to a variety of processing conditions. Because ceramic substrates can withstand temperatures in excess of 1000°C, thick-film materials are often fired at temperatures of about 1000°C and lower. Thick-film technology comprises specially formulated pastes applied using screen printing, fired onto a ceramic substrate in a definite pattern, and sequenced to produce electrical components, interconnections, and a complete functional circuit. These pastes possess an organic binder to make them thixotropic in nature with dual viscosity: viscous at rest and flowing with motion [22]. These pastes possess essentially a functional phase to produce a film with desired electrical properties. Depositing successive layers result in multilayer interconnection formation containing integrated passive components, added active chips, and integrated circuits (see Figure 1.2).

The thickness of a film is typically on the order of 12–25 μm (0.5–1 mil). After the film has been printed on a substrate, it should be allowed to settle to eliminate the mesh impression in the pattern. The settling time varies from 5 to 20 min depending on the viscosity of the paste. The film is then
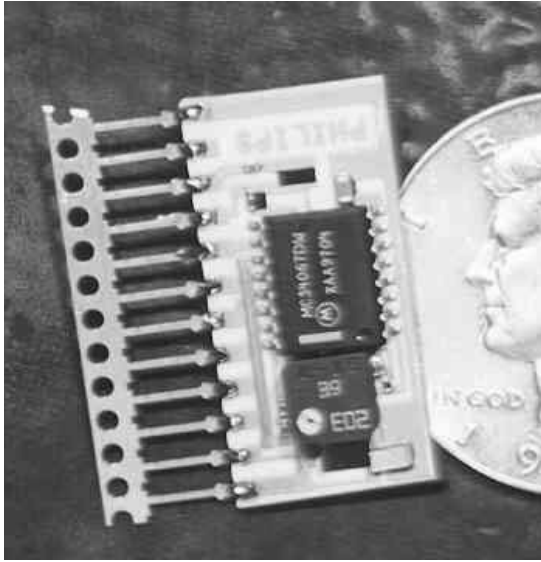
FIGURE 1.2
A thick-film circuit.

dried to remove the volatiles while the binder remains. Drying temperatures vary from 100 to 150°C for 5–15 min using an oven with circulating air. The film is then fired in a multizone tube furnace. The organic binders and solvents are burned out in the first phase. The metallic elements are either oxidized or reduced to develop the required characteristics of resistivity, temperature, and voltage coefficients, and then a sintering of the glass materials occurs to adhere the film to the substrate and protect the metallic elements. A uniform airflow is maintained through the furnace in a direction opposite to that of advancing substrates, so that the volatile organic materials will be removed [23].

In conventional thick-film technology, each successive layer is built up by successive printing and firing of conductive and insulating layers. The pastes are applied by the conventional screen-printing process, followed by drying at 100–150°C to remove solvents. Resistors, capacitors, and inductors can be patterned, as well as conductors. As many as four dielectric printing and firing steps with accompanying via-fill printing and firing may be required for each layer. Firing takes place at temperatures of 500–1100°C. This essentially sequential process becomes less cost-effective as the number of conductive layers increases.

In the past screen printing in high-volume production operation is 200- to 250-μm vias and 150-μm lines and spaces. Today a number of manufacturers produce circuits with 100-μm vias and 75-μm spaces and trace design rules. The trends are toward smaller and smaller vias on tighter pitches with finer lines and spaces. Design rules that include 30- to 50-μm vias are under evaluation.

To obtain finer lines and smaller vias, one can use photoimageable thick-film process for dielectric and conductors and diffusion patterning. The photoimageable thick-film process involves the use of a photoactive paste printed on a substrate and exposed through artwork or a mask to define circuit characteristics, lines, and vias. The materials are developed in an aqueous process and then fired using the conventional thick-film technique. Copper, silver, and gold metallizations are used, and layer counts of up to 10 circuit layers are possible.

1.5.2   Screen Preparation and Inspection

The screen mesh is made by weaving stainless steel wires to form a long sheet. Common meshes are woven in a plain weave pattern, with each wire simply going over and under only one wire at a time, thus there is more open area for a given mesh count and wire size. The mesh count designates the number of wires per unit length. The mesh count can vary from 80 wires per inch to print solder paste to 400+ wires per inch for fine-line printing. The screen mesh is stretched over the screen frame with certain tension. The screen frame is made from cast aluminum, with the bottom of the frame machined to be parallel to and at a fixed distance from the top; thus the screen is made parallel to the printer. The screen is an important factor in determining the thickness of the deposition printed during the screen printing process.

Screen printing is the process by which a thick film paste is applied to the substrate in the desired pattern. A pattern is formed by exposing a stainless steel mesh screen that has been coated with a photosensitive material (referred to as *emulsion*) to UV light through a film of the desired pattern, placed in direct contact with the emulsion. Stainless steel adds a high degree of control and precision in comparison with other materials, and it is resistant to wear and stretching. Emulsion thickness must also be controlled and held constant. Taking precautions to align the film positive or pattern to the wire mesh of the screen is important (using a microscope and/or vacuum frame). Exposure time and distance vary with the light source. Emulsion is hardened by UV light exposure where it is not protected by the dark areas of the film. The protected portion can be simply washed away with water, leaving openings in the emulsion corresponding to the dark areas in the film. After exposure, the screen is washed in water at 90–110°F for 30–60 sec. A light-pressure water spray from the substrate side of the screen is used to wash the emulsion from the pattern area. The screen is allowed to dry thoroughly, (if heat is used, it should not exceed 120°F). Any voids can be repaired using block-out material. Screen tension must be controlled if fine pattern definition and thickness control are to be maintained (a screen tension gauge is used). The screen is then mounted on the screen printer, and proper adjustments are made to secure it. The paste is applied to the top of the screen, a substrate is placed underneath it, and the paste is forced through

the openings in the screen with an accelerated squeegee and by applying the right pressure.

1.5.3   Screen-Printing Process

The screen printer is one of the main pieces of equipment used in thick-film production. As for the screen mounting, the mounting plate must allow easy accessibility to the screen frame for changes and to the bottom for easy cleaning during the process. The screen mounting must hold the screen frame rigidly in place as the squeegee passes. Open area must be provided for preliminary setup, substrate alignment, and paste addition. The substrate-holding fixture must be capable of accurately locating and registering the substrate; provide a method of rigidly fixing or holding the substrate in a position (vacuum); wear well; be easy to replace (different substrate size); and provide a flat surface. Standard terms include the following: *downstop*, *squeegee pressure*, *squeegee speed*, *attack angle*, *hydroplaning*, and *breakaway* or *snap-off distance*. *Downstop* is a printer feature that limits the maximum up-and-down travel of the squeegee during the printing cycle. Screen damage may result from an improperly set downstop, because this feature prevents the squeegee force from overstraining the screen mesh. The squeegee pressure simply controls the force applied by the squeegee on the screen. The angle of attack is the angle that the squeegee forms with the plane of the screen. Hydroplaning refers to a condition where the squeegee floats on a thin layer of ink on the screen's surface. As the squeegee moves across the screen, it locally deforms the screen so that the snap-off, or distance between the screen and substrate, is reduced to zero. As the squeegee proceeds to the end of its travel, the screen snaps back into the normal free position.

The squeegee material must be compatible with the pastes (neoprene and polyurethane are mostly used). The hardness of the material should range between 50 and 90 durometer. The squeegee angle of attack is between 45° and 60°. The pressure applied to the squeegee should be determined exactly (pressure affects line definition and uniformity of the print).

1.5.4   Substrate Cleaning and Process Environment

Ultrasonic cleaning of prefired substrates with an appropriate solvent is advisable to remove grease, oil, or deposited particulate material. Rinsing is done very thoroughly with deionized water. After inspection and cleaning, the substrates should be stored in a clean, dry, and dust-free area. The facility should have a controlled atmosphere area for material preparation and screen printing to maintain cleanliness. Aqueous cleaning of tape materials is seldom performed because these materials are supplied in a clean condition but are susceptible to damage caused by moisture absorption. Tacky adhesive rollers are normally preferred to remove any particulate debris that may arise during processing.

The furnace is usually located outside the screen-printing area to simplify management of the atmosphere control system. The furnace is vented to the outside to eliminate the organic by-products of the burn-off cycle of the firing process. The thick-film facility should be air conditioned, humidity controlled, and dust controlled. For narrow line widths, dust control in the screening area becomes a necessity. Temperature control has an effect on viscosity. Humidity control has an effect on the rate of solvent evaporation including emulsion life of the screens. Temperature may range from 70 to 80°F. Humidity may range from 30 to 50%. Once the absolute level is set, the temperature should be held ±2°F and humidity ±5%.

1.5.5 Thick-Film Formulations

The basic features of inks or pastes printed and fired on the substrate are particles of metals and/or metal oxides, glass (metal oxides mixture), a binder, and a solvent to make the paste fluid in nature [24–26]. A metallic conductive component comprising one or more precious metals in finely divided powder form with powder sizes ranging from 1 to 10 μm in size. Structural shape and particle morphology are critical parameters that affect the desired electrical characteristics, and controlling these parameters ensures uniformity of the fired film properties.

Films using a glass or frit have a relatively low melting point on the order 500–600°C, but, in general, they pose a difficulty for subsequent component assembly processes because of the presence of glass on the surface. Chemically, the molten glass reacts with the glass in the substrate. In addition, the glass flows into and in between the features in the substrate surface. Both mechanisms result in adhesion of the film to the substrate surface. The glass creates a matrix for the active particles, holding them in contact with each other to promote sintering and to provide electrical passage of current. Common thick-film glasses are based on Ba_2O_3/SiO_2 with modifiers such as PbO, Al_2O_3, Bi_2O_3, ZnO, and BaO to change the physical characteristics of the film. In the case of metal oxides, a pure metal is mixed with the paste, and it reacts with oxygen atoms on the surface of the substrate to form an oxide. The conductor adheres to the oxide by sintering during the firing stage. During firing, the oxides react with broken oxygen bonds on the surface of the substrate, resulting in molecular-bonded materials with good adhesion. This class of materials needs to be fired at 900–1000°C. In addition, some materials referred to by mixed bonded systems use both reactive oxides and glasses, thus resulting in good properties with a moderate firing temperature.

The organic binder, a nonvolatile organic, serves the purpose of holding the active elements and the adhesion elements in suspension until firing of the film takes place, and it also provides the paste with the desired fluid characteristics needed for screen printing. The organic binder, such as ethyl cellulose

and various acrylics, starts to burn off at about 350°C and has to oxidize completely during firing to avoid film contamination.

To provide the proper flowing paste viscosity, the solvent or thinner should be volatile in nature and may evaporate at about 100°C. Terpineol, butyl carbitol, and complex alcohols may play the solvent role. In addition, some plasticizers may be added to the solvent to modify the thixotropic nature of the paste to promote the printing process. The paste must have the minimum pressure required to produce a flow. The paste also must possess a nonlinear shear rate/shear stress ration, meaning as the shear rate increases (because of squeegee pressure and motion), the paste becomes thinner. All these ingredients are mixed together in proper proportions and milled for a certain duration of time to ensure thorough mixing, distribution and dispersion within the paste, and to complete the formulation process. The percent solids parameter, 85–92% by weight, measures the ratio of the weight of the active and adhesion elements to the total weight of the paste, and this parameter has to be controlled precisely to produce a good flow of the paste with a well-defined line definition of the fired film.

1.5.6 Heat Treatment Processes for Pastes

Thick-film components include passive components, such as conductors, resistors, dielectrics (both capacitors and insulators), varistors, filters, couplers, transmission lines, and other components. To achieve these electrical elements with desired electrical properties, thick-film materials are formulated into pastes or inks possessing a certain viscosity to undergo a specific heating cycle. These pastes or inks do differ in density, viscosity, solid contents, and function served in the electrical circuit. As stated earlier, the printing process requires a screen-printing machine equipped with a good screen possessing the right specifications. Printing the inks on the substrate involves a squeegee pressing the ink through a stencil on the screen. The ink at the bottom of the screen contacts and wets the substrate because of the surface tension of the ink, and the substrate pulls the ink through the openings of the screen when the screen snaps back off the substrate.

After depositing the film through screen printing, the film should be given sufficient time to set in order to promote the print leveling and remove the mesh impression. The settling time varies from 5 to 20 min, depending on the viscosity of the paste. The film is then placed in an oven with circulating air for drying for a period of 15 min at 100–150°C to remove the organic solvent. The organic solvent should be removed slowly because rapid evaporation of the solvent may cause void and blister formation.

After drying, the particles in the film are bound together with a plastic-like material (ethylcellulose or similar) to bond the film to the substrate and hold the particles together until the substrate is fired. The film is then fired in a belt or box furnace, according to a certain firing profile usually achieved through four to eight heating zones. In the preheat or binder burnout portion

of the furnace, heat decomposes the ethylcellulose, and it combines with the oxygen in the air to form carbon dioxide and water vapor (both are properly ducted away). The organic binders and solvents are burned out in this first phase. The film then reaches a higher temperature on the order of 480–650°C to start melting the glass particles in the film. Thus, the glasses bond the film to the substrate, and the metal particles in the conductor films begin to sinter or join together. At peak firing temperatures on the order of 850°C for 10 min, the film achieves its desired electrical attributes. Cooling, following a certain rate, is necessary to avoid stresses and oxidation of the fired film.

1.5.7   Thick-Film Metallizations

The basic constituents of a thick-film conductor consist of four main ingredients. The first is a conductive metallic phase that typically consists of finely divided noble metal powders or alloy. Examples include gold (Au) for high-reliability circuits, silver (Ag), silver–palladium (Ag–Pd) with ratio ranging from 1:2 → 1:12, palladium–gold (Pd–Au) with ratio 1:2.5 by weight, platinum–gold (Pt–Au), with ration 1:3.5 by weight, and copper (Cu). Aluminum (Al) and nickel (Ni) may be also used. The particle sizes range from submicrometer to a few micrometers. The selection of the particle size, distribution, surface chemistry, and shape depends on the interfacing materials as well as the application. Resistivity varies from 3 to 5 mΩ/□ for Au, 12 to 16 mΩ/□ for 6 Ag-1 Pd, and 2 to 4 mΩ/□ for Cu, and 40 to 70 mΩ/□ for Ni, based on a fired thickness of 0.5 mil. The second part is a binder phase or bonding agent inorganic in nature that typically consists of a mixture of glass powders. The third component is an organic medium, or vehicle, that serves as the carrier agent for the inorganic constituents to properly provide the paste rheology for the screen-printing process. The final component is an organic suspension medium. A polymeric thick-film conductor may consist of a silver, carbon (C), or Ag and C mixture functional phase dispersed in a thermoplastic or thermosetting polymer and solvent.

Although noble metals are fired in air atmosphere, copper, nickel, and aluminum firing necessitates a pure nitrogen environment. The firing cycle for the conductor composition after deposition onto the substrate consists of a warm-up period during which the organic suspension medium and diluents are eliminated by burning off to form carbon dioxide, a period at peak firing temperature when the glass bonding constituent melts and sintering of the metallic particles takes place, followed by a cooling period to anneal the film. A uniform airflow is maintained through the furnace in a direction opposite to that of advancing substrates (for volatile organic materials to be removed).

Functions of a thick-film conductor include conductor interconnections, soldered lead and device attachment, thick-film resistor terminations, crossover connections, capacitor electrodes, chip and die bonding, wire bonding, low-value resistors, and packaging of thick-film circuits. The factors considered in

selecting a conductor composition include ultimate solderability, resistance to leaching, adhesion of the fired films, suitability for wire and chip bonding, compatibility with resistor and dielectric films, line definition attainable, and resistance to aging effects upon refiring.

1.5.8 Thick-Film Dielectrics

Functions of the dielectric paste include a crossover dielectric and high-K capacitors. A crossover dielectric is a low dielectric constant insulator capable of separating two conductor patterns through several firing steps with good isolation and minimum stray capacitance. The requirements of a crossover dielectric include control of resoftening with the top conductor firing, low dielectric constant to prevent AC capacitance coupling between insulator circuits, low electric loss to avoid dielectric heating, minimum tendency to form pinholes, high resistance to thermal shock, and low sensitivity to water vapor. High-dielectric-constant capacitors are based on barium titanate. The recommended procedure with high-dielectric-constant dielectrics is to fire the bottom electrode. Screen-printed thick-film capacitors are formed by screen printing a dielectric paste on top of a lower metal electrode, followed by a firing process. The dielectric should overlap the electrode pattern by at least 10 mil on all sides to eliminate surface leakage. Often, the dielectric is double printed to reduce the probability of pinholes formation. Then, screen printing a top electrode on top of the second dielectric layer is followed by cofiring. The top electrode should fall completely within the bottom electrode area. The dielectric constant depends on the electrode materials as well as the peak firing temperature.

Dielectric compositions for insulator fabrication include insulator dielectrics or glass filled with ceramic dielectrics (alumina and silica added to the glass), ceramic-filled glasses (glass and refractory oxides), and crystallizing dielectrics (crystallizable glass and crystallization agents).

The raw materials most commonly used in high-K dielectric powders for capacitor fabrication are barium titanate ($BaTiO_2$ or barium carbonate as the source for a BaO and anatase or rutile TiO_2), lead titanate ($PbTiO_3$), and lead zirconate titanate (formulated from its oxide constituents). Barium titanate may often contain additives of strontium, calcium, or lead. After the initial mixing, the dielectric formulations are calcined in powder form to initiate thermochemical reaction among the constituents for compound formation, to burn off volatile impurities, and to eliminate both carbon dioxide and water vapor. This is achieved at about 1000°C for about 2 h. Postcalcination grinding is followed by ball milling to small sizes 1–10 μm for screen printing in a carrying vehicle, such as deionized water, or alcohol, or tetrachloroethylene and then dried, reducing all compositional inhomogeneity. Raw material purity (99.7% and higher), stoichiometry (excess major cations can affect the temperature and time of film sintering, modifying the microstructure and dielectric properties), and particle size (larger particle sizes can

result in low-density fired films possessing large intergranular voids) are important factors to determine the dielectric electrical properties.

Commercially available dielectric materials for capacitor fabrication possess a typical dielectric constant value that varies between 20 and 1500. The firing cycle greatly controls the capacitance density and loss factor of the dielectric material and the adhesion of the metallic electrode composition. During the firing process, the nonvolatile portion of the organic vehicle decomposes. The firing process should proceed slowly to allow the organic material to burn out or completely decompose prior to the melting of the glass.

1.5.9   Thick-Film Resistors

Resistor formulation contains an insulating glass frit, an electrically conducting powder, an organic agent, and additives to enhance electrical attributes. Resistor materials are classified into organometallic or resinate systems and particles of metal in glass frit or cermet systems. Precious metal resinates are solutions of metal chlorides in organic solvents or organometallic compounds in which the metal atom is attached to an oxygen atom linked to a carbon atom. On the other hand, cermets are materials resulting from a fused structure of conductive or resistive materials in a vitreous nonconductive binder. These resistive elements may and can include oxides or oxide compounds of indium, thallium, ruthenium, palladium, tungsten, and other noble elements. The firing furnace should have good control over the setting of the various heat zones for good yield and reproducibility. Resistor properties are microstructurally and stoichiometrically dependent, affecting the sheet resistivity, the temperature coefficient of resistance, the electrical noise, and the stability of values with time under load [27,28].

The resistor compositions typically comprise of a resistive component, a glassy phase, an organic suspension medium, and an organic diluent. Compositions are available having fired sheet resistivities from 1 $\Omega/\square$ to 5 M$\Omega/\square$, with the resistive component being palladium–palladium oxide–silver compositions, mixtures of precious metals other than silver and palladium, ruthenium oxide, thallium oxide, indium oxide, tin oxide, tungsten–tungsten carbides, or tantalum–tantalum nitride. Electrical properties of thick-film resistors include temperature coefficient of resistance (TCR), voltage coefficient of resistance, long-term drift under temperature and load, and electrical noise. The conduction process in thick-film resistors is extremely complex. The active materials behave like metals to a certain extent. A metal typically has a positive TCR. The glass behaves basically like an insulator. In an insulator, TCR is slightly positive. However, in very thin layers, when some of the active material has been dissolved in the glass during the firing process, the glass behaves like a semiconductor with negative TCR. To a very large extent, the resistance of the pastes is controlled

by controlling the amount of active material. The more active material, the lower the sheet resistance value. Pastes with lower sheet resistivity tend to take on metallic characteristics and exhibit a positive TCR. Also, thin resistors tend to have a more negative TCR than thick resistors. Short and narrow resistors have a more positive TCR than long and wide resistors because of the diffusion of the conductor material.

1.6 Thin Films on Ceramics

1.6.1 Introduction and Background

Although thin-film technology has been widely used in the fabrication of semiconductor devices for decades, it was not common in electronic packaging until the mid-1980s, due to the limitations of some ceramics in wiring density (0.127-mm line width) and low signal speed (high dielectric constant). Thin film on ceramics has the highest interconnect density among the ceramic interconnect technologies, resulting from its small line-width/spacing (~25/50 μm) and via diameter (~20 μm). Converting the line and via data into interconnect density, one will expect 200 cm/cm^2/layer (500 in./in.^{2}/layer) and 4×10^4 vias/cm^2 (25×10^4 vias/in.^{2}) from thin-film technology, as opposed to 50 cm/cm^2/layer (125 in./in.^{2}/layer) and 2000 vias/cm^2 (1.27 $\times 10^4$ vias/in.^{2}) from conventional ceramics.

High interconnect density reduces the number of signal layers required to connect devices mounted on a substrate. For instance, a module consisting of 33 layers of cofired ceramic to interconnect 100 chips can also be implemented using 5 to 10 thin-film layers, depending upon the configuration of signal lines [29]. Short interconnect paths due to a lower number of interconnect layers decrease the cycle time of a high-performance system. In addition, reduction in size and weight is another advantage of high-density interconnects.

In the past, numerous thin-film techniques have been developed for various substrates and applications [29]. Regardless of process variation, thin-film interconnect technology typically consists of a dielectric substrate, such as ceramic, providing mechanical support and a heat dissipation path; dielectrics separating the interconnect conductors; conductors and vias forming interconnect; and resistors, inductors, as well as capacitors in some applications. Once a thin-film interconnect substrate is finished, devices are populated on top of it. At this point, a functional board or card has been accomplished. The following sections describe the key aspects of thin films on ceramics; the reader can consult Reference 30 and Reference 31 for more information about thin-film technology.
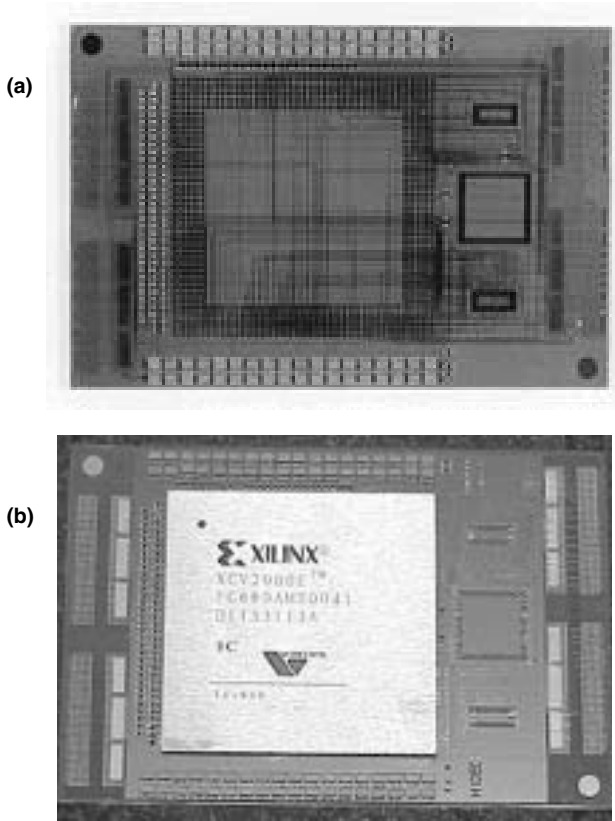
FIGURE 1.3
Photographs of a thin-film interconnect module on a 14-layer LTCC Substrate. (a) Partially assembled completed substrate and (b) with an assembled large BGA microprocessor on the substrate. Note the attached passive devices as well as sites for the FPGA, ASIC, and memory chips. Each end of the substrate is composed of ~1000 sites for *z*-axis interconnects.

1.6.2 Thin-Film Process Example

Figure 1.3 shows an example module with thin-film interconnects on a low-temperature cofired ceramic (LTCC) substrate [32]. This module measures $81 \times 55 \times 1.88$ mm and has a 14-layer cofired LTCC substrate with silver conductor and 6-layer thin-film interconnects (three on the top and three on the bottom) using Ti/Cu and benzocyclobutane (BCB) structure. A microprocessor is connected to 2 memory chips and over 140 passive components through about 4000 nets.

1.6.3 Preparation of Substrates

Because thin films range from hundreds of angstroms to several micrometers, roughness, flatness, and waviness of substrate surface are crucial to a

successful deposition of thin-film materials. Therefore, the first step of the thin-film process is to prepare an appropriate substrate surface suitable for the process. Normally, the prefired ceramic substrates for thin film have been polished or glazed. To start the thin-film process, a polymer layer such as polyimide or BCB is applied onto the surface of the substrate to provide a planar surface for deposition of the first metal layer.

Nevertheless, preparation of the multilayer substrate surface is more complex and is usually carried out by the users instead of manufacturers of ceramic substrates. Simply applying a polymer layer onto the as-fired ceramic surface cannot lead to successful thin-film layers. The solvent trapped in microporosities in the conductor for vias and/or at the interface between conductor and ceramics may outgas during the reflow soldering when populating components on the finished thin-film substrate, resulting in poor adhesion of thin-film metal and dielectric at the position of vias.

Therefore, before applying the polymer layer onto the multilayer ceramic substrate, lapping and polishing of the ceramic surface is necessary. Lapping and polishing is a technique used to flatten a surface through mechanical removal of surface materials. A lapping and polishing machine is employed for this purpose and can provide at least 250-Å surface roughness and 2-μm/mm camber.

Figure 1.4 shows the surface profiles of multilayer LTCC substrates under different conditions: as-fired, lapped, and polished, and in contrast to a Si wafer.

1.6.4 Application of Dielectrics

Two types of dielectrics are commonly used to separate the metal interconnects: silicon dioxide (SiO_2) for silicon substrate and polymer dielectric for most applications. The widely used polymer dielectrics are polyimide and BCB in either photoimageable or nonphotoimageable. Several techniques can be employed to deposit a uniform polymer dielectric film onto a substrate, including spin coating, spray coating, meniscus coating, extrusion coating, among other techniques [33–35]. Spin coating is the most commonly used process to deposit photoresist or polymer dielectric using a liquid source or fluid. This process has the capability of processing up to 300-mm substrates with resulting film thickness from a few to tens of microns that can be easily controlled by adjusting either spin speed (rpm) and/or viscosity of the fluid.

A spin-coating process involves dispensing, spreading, and thinning of a given fluid. Figure 1.5 shows a typical process profile and the change of fluid geometry in each process stage.

Spin coating also possesses some intrinsic disadvantages. Normally, the resulting polymer film uses no more than 10% of the fluid dispensed onto a substrate, with the remaining 90% being spun off into the coating bowl for disposal. This is because of the amount of liquid required to cover the overall
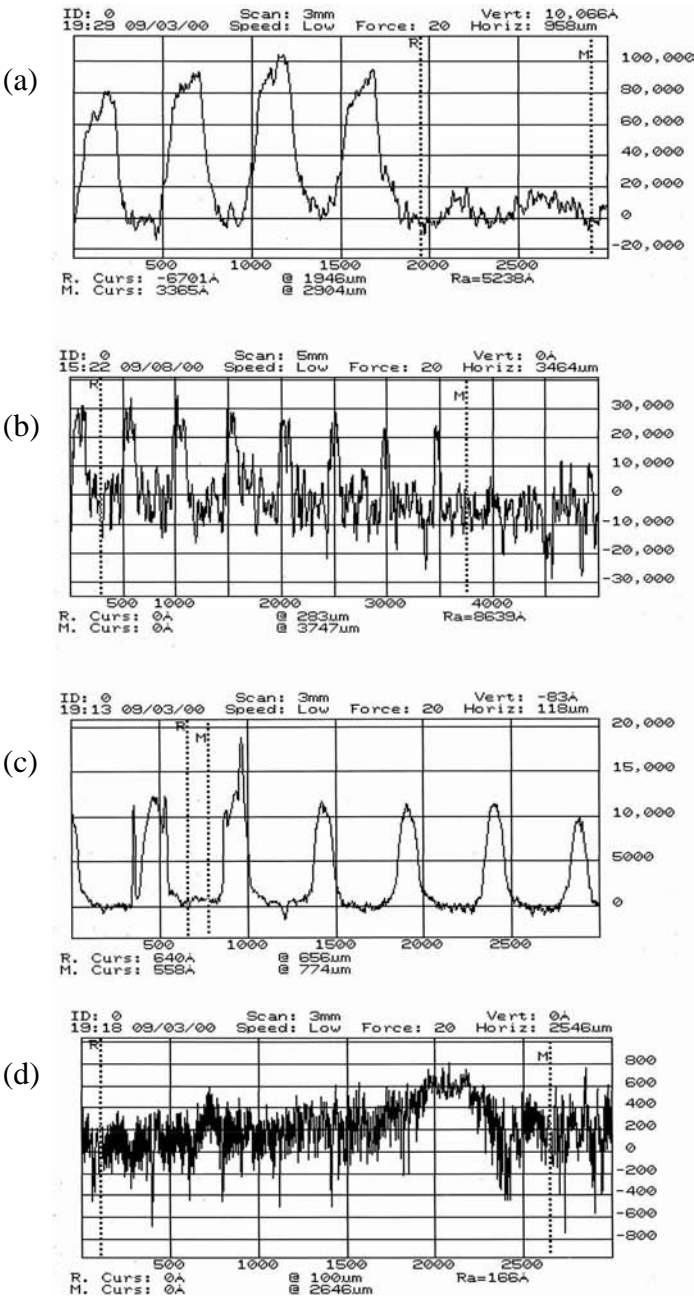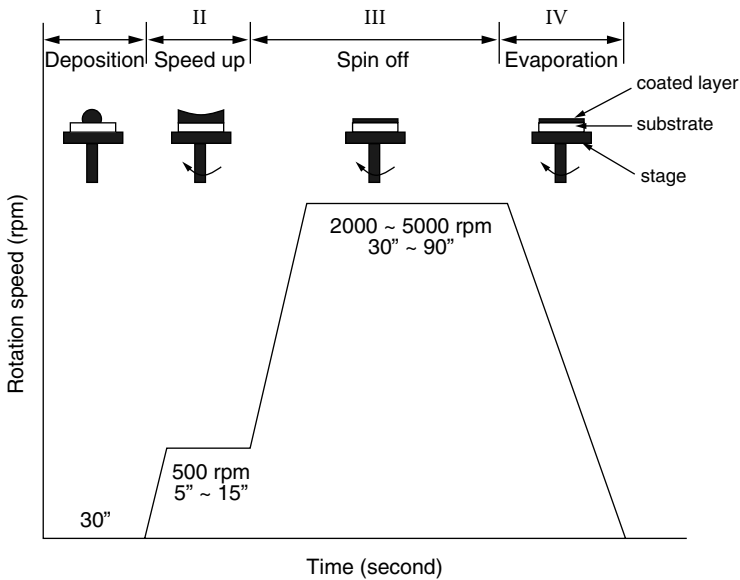
FIGURE 1.4
Surface profiles of LTCC substrates: (a) as-fired, (b) lapped, (c) polished, and (d) in contrast to
a Si wafer. All vertical scales are in angstroms.

FIGURE 1.5
An illustration of spin-coating process.

substrate surface to avoid a discontinuity of film and to ensure film uniformity. Throughput of spin coating is another concern regarding volume production. To obtain a thick dielectric film, multiple thin coatings as opposed to a single thick coating should be considered because the solvent in the fluid dries before the fluid is spread on the entire substrate surface. To overcome the disadvantages of the spin-coating process, the previously mentioned methods were developed. However, spin coating is still the process of choice today, and the reader can consult Reference 34 and Reference 35 for details on other coating processes.

1.6.5 Formation of Vias in Dielectrics

Vias in dielectrics for *z*-axis interconnect are commonly created using a reactive ion etching (RIE) process for nonphotosensitive dielectrics or a photolithography process for photosensitive dielectrics. Wet etching and laser ablation of polyimide have also been reported [36,37]. A typical RIE process is illustrated in Figure 1.6.

The RIE process involves the removal of unwanted dielectric material from the areas where vias are desired by means of reactive ion beam with etching rate of 0.5 ~1 µm/min, depending on etching conditions. The RIE process takes advantage of both a physical collision of high-kinetic-energy ions with a dielectric and a chemical reaction between a dielectric polymer and reactive gases such as oxygen or the mixture of oxygen and other gases. Etching of
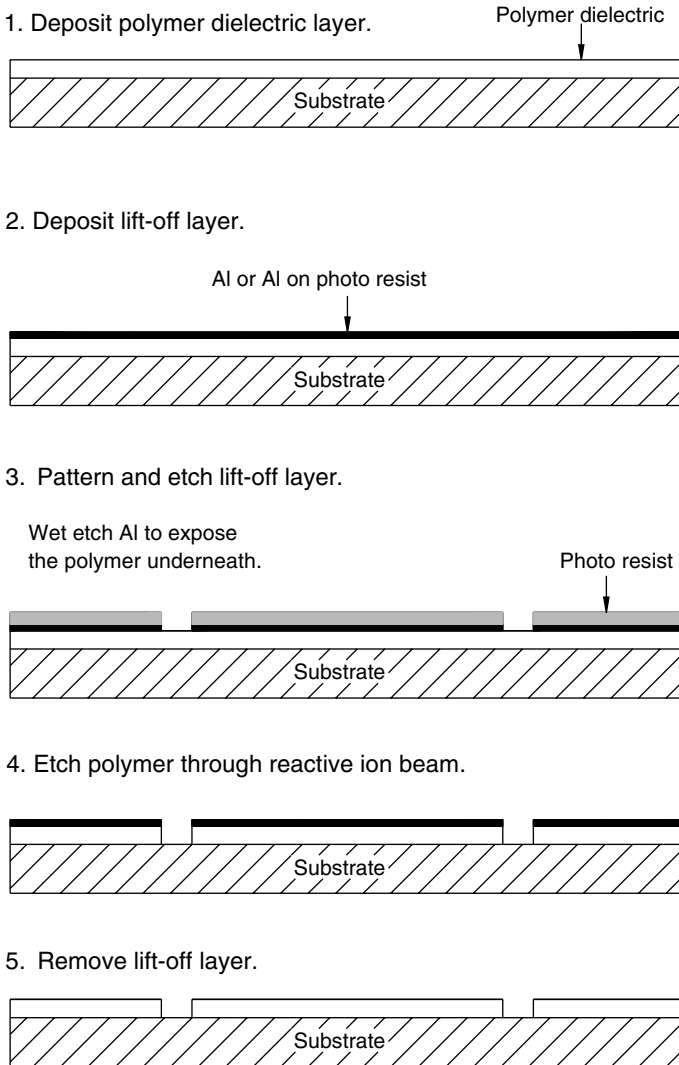
1. Deposit polymer dielectric layer.   Polymer dielectric

2. Deposit lift-off layer.

Al or Al on photo resist

3. Pattern and etch lift-off layer.

Wet etch Al to expose
the polymer underneath.   Photo resist

4. Etch polymer through reactive ion beam.

5. Remove lift-off layer.

FIGURE 1.6
Formation of vias in polymer dielectric through reactive ion etching.

a polyimide dielectric can be accomplished using oxygen alone, whereas a mixture of oxygen (O_2) and fluorine gas (SF_6) must be used to etch a BCB dielectric due to the formation of silicon dioxide on the surface of the BCB (BCB contains silicon). Although chemical reaction produces an isotropic etching of material, by changing the balance of chemical and physical etching, it is possible to influence the anisotropy of the etching characteristics and obtain vias with a straight wall.

The area of dielectric to be etched is exposed through an etch mask deposited on the dielectric. A photoresist mask is usually employed for etching of thin polyimide dielectrics, but it must be thicker than the polyimide as the reactive ion etches the photoresist mask as well. However, due to a cracking of the thick photoresist, coupled with a faster etching rate than BCB, an inorganic (SiO_2 or Si_3N_4) or metal (Al or Cr/Cu) etch mask must be used in cases involving thick polyimides or BCB dielectrics. To make an Al etch mask, a 1000–2000 Å thick metal layer is deposited and patterned on a dielectric through photoresist, and then wet-etched in a solution such as 79 phosphoric/10 acetic/0.6 nitric acid/10 water/0.03% Triton X-100 at a temperature around 40°C, giving an etching rate of 1000–2000 Å/min, depending on the age of the bath. Once vias are formed in the dielectric through dry etching, the etch mask is removed by wet-etching it. The alternative removal of an etch mask is a so-called "lift-off" process, in which a photoresist layer is applied between the etch mask and the dielectric and stripped off upon completion of the RIE process. Because the RIE process produces a straight wall, vias in adjacent layers can be stacked, resulting in a high interconnect density.

To reduce the number of process steps and, ultimately, cost involved in via formation through RIE process, photosensitive dielectrics may be used. This process necessitates just two fabrication steps — exposure and development — as contrasted with up to seven steps in the RIE process. The exposure of dielectric to UV light results in a different solubility for exposed and unexposed areas when placed in a developer solution. Following exposure, developer is sprayed onto the dielectric, and the exposed areas of dielectric dissolve in the solution, leaving vias in the dielectric. Usually, some dielectric residue remains on the metal pads under vias, and a short RIE cleaning process may be added to ensure direct contact of metal in the adjacent layers.

Because the developer also attacks the exposed dielectric laterally, sloped-wall vias are produced. Consequently, metallization of these vias entail a metal deposition technique that fully covers the sloped wall. In addition, vias in the adjacent layers must be staggered, which decreases the interconnect density. Besides being a simple process, ease of reworking is another advantage of the utilization of a photosensitive polymer dielectric. Being able to easily remove the unwanted dielectric layer before hard baking avoids the stripping process.

1.6.6   Metallization of Vias and Interconnect

The deposition methods of metal for vias and interconnect can be categorized into four groups: (1) sputtering, (2) evaporation, (3) electroplating, and (4) electroless plating. In some cases, metal interconnects are accomplished along with the metallization of vias.

1.6.6.1   Sputtering

Figure 1.7 depicts a typical sputtering metallization process. This metalliza-
tion technique is also called "conventional thin film," "wet-etching," or a
"subtractive" process. It is the most widely used technique for via metalli-
zation and interconnect formation because of the simplicity of the process.
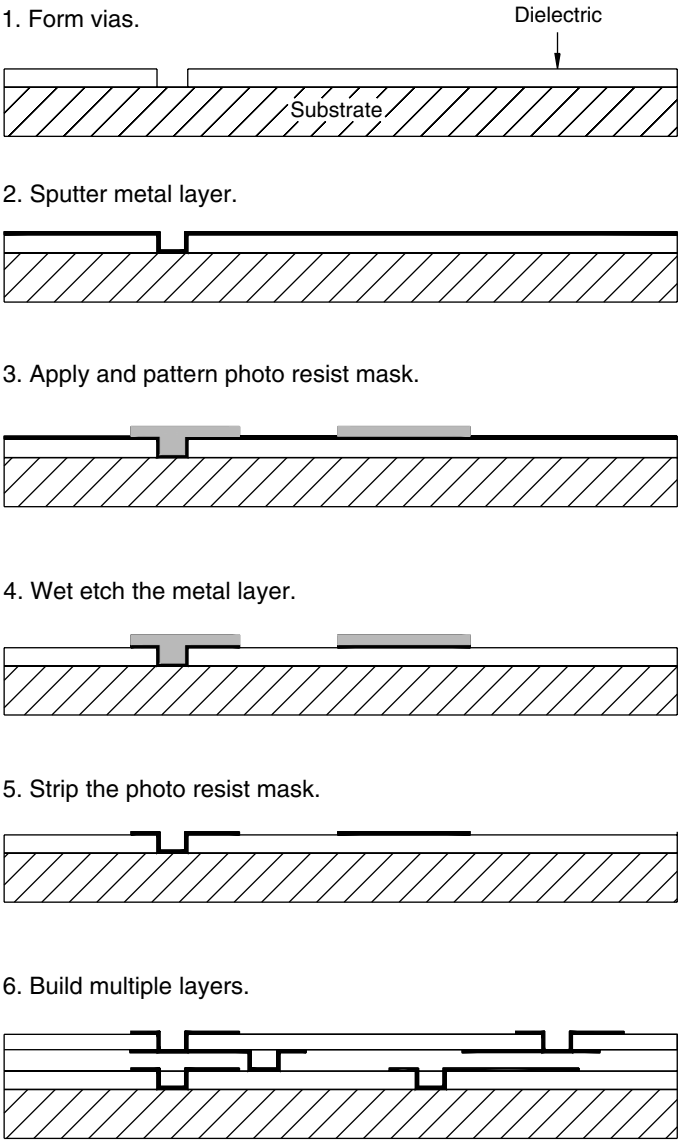
1. Form vias.

2. Sputter metal layer.

3. Apply and pattern photo resist mask.

4. Wet etch the metal layer.

5. Strip the photo resist mask.

6. Build multiple layers.

FIGURE 1.7
Sputtering metallization: wet-etch process.

Because sputtering deposition covers the sloped wall of vias, this technique is also suitable for the metallization of vias patterned in a photosensitive dielectric, vias formed through laser ablation, and wet-etched vias in polyimide. However, it is difficult to sputter a thick metal film, because stress in the deposited film leads to poor adhesion. The typical metal thickness is around 2 μm. Therefore, the vias are partially filled and a staircase or staggered via layout is normally used, which limits interconnect density. In addition, the interconnect lines have sloped sidewalls because both vertical and lateral etching occur in the wet-etching process.

1.6.6.2 Evaporation

Unlike sputtering, evaporation is a line-of-sight deposition technique, resulting in high deposition rates in the desired direction and low deposition rates in other directions. Taking advantage of this characteristic, a lift-off process illustrated in Figure 1.8 has been developed. In this process, evaporation is used to deposit metal onto the RIE etching mask, filling the vias and channels that have been etched through RIE. Next, the etching mask is lifted off in an aqueous solution with the metal on top of the etching mask being removed from the substrate, producing patterned metal for vias and lines.

Depending on the metal deposited, the lift-off process may vary. Copper is insoluble in an aqueous solution, therefore the etching mask needs to be removed by dipping the substrate in an appropriate stripping solution. However, because aluminum dissolves in both acid and alkaline solutions, following the evaporation of this metal, a photoresist layer is normally applied and patterned to protect the desired metal in vias/channels. This protection layer is stripped off after the lift-off mask is removed. Note that the photoresist layer in this process must withstand whatever solution is used to etch the RIE mask. This technique produces a truly planar surface for the next layer.
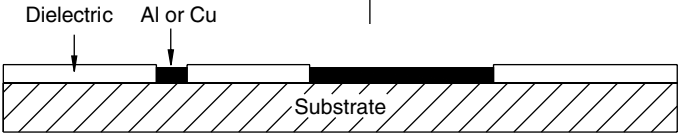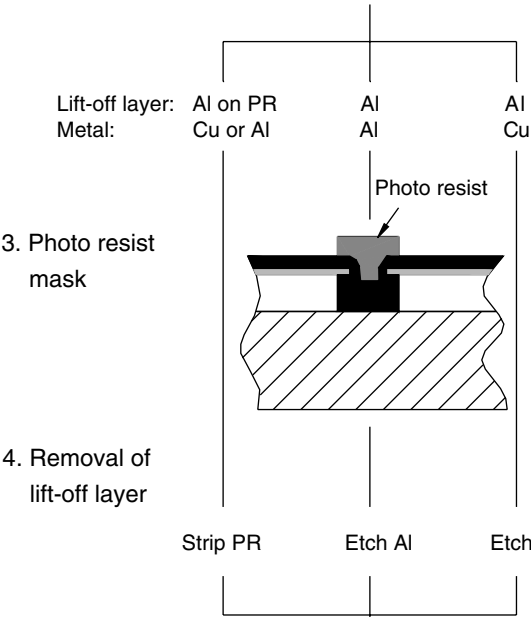
1.6.6.3 Electroplating

In this method, metal is selectively electroplated. Because aluminum cannot be electroplated in an aqueous solution, copper is the most commonly used metal. A typical process sequence is shown in Figure 1.9.

This process begins with sputtering a thin seed layer, e.g., Ti/Cu/Ti (500/ 1000/500 Å), providing adhesion/barrier between the dielectric and the metal, as well as an electrode for subsequent electroplating. Titanium on top of copper also protects the copper from oxidation during processes before electroplating. A photoresist layer is then applied onto the dielectric, patterned, and developed to expose areas where copper will be plated, i.e., vias and/or interconnects. Just before to electroplating the copper, the top titanium layer is wet-etched in a solution such as 2% hydrofluoric and 0.5% nitric solution with etching rate of 500–2000 Å/min, depending upon oxidation of the titanium. A 2~10 μm thick copper film is electroplated in

1. Formation of vias and channels

Dielectric   Via   Channel for   Lift-off layer:
                                signal line   Al or Al on PR

Substrate
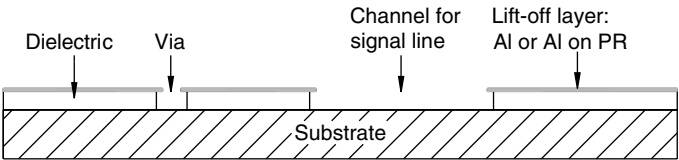
2. Evaporation of metal layer

Lift-off layer: Al on PR   Al   Al
Metal: Cu or Al   Al   Cu

                                 Photo resist

3. Photo resist
   mask

4. Removal of
   lift-off layer

              Strip PR   Etch Al   Etch Al

Dielectric   Al or Cu

Substrate

5. Fabrication of multiple layers
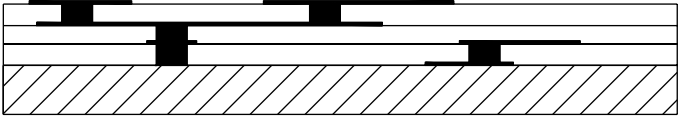
FIGURE 1.8
Evaporation metallization: lift-off techniques.

1. Form vias.

Metal   Via

Dielectric

Substrate
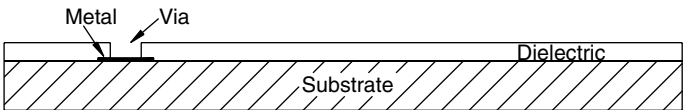
2. Sputter seed layer.   Ti / Cu / Ti (500 / 1000 / 500 Å)

3. Apply and pattern photo resist mask.
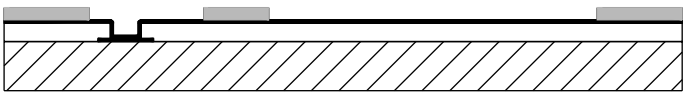
4. Electroplate metal on top of the seed layer.
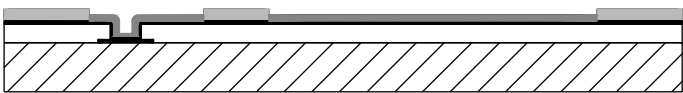
5. Strip the photo resist mask.

6. Wet etch the seed layer.
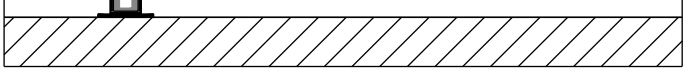
7. Construct multiple layers.
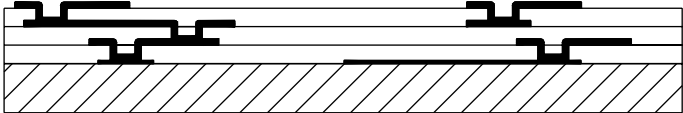
FIGURE 1.9
Electroplating metallization.

the openings for vias and interconnects that were formed in the photoresist layer. Afterward, the photoresist layer is stripped off and the Ti/Cu/Ti seed layer is etched away using the electroplated copper as a mask. Because the copper thickness in the seed layer is only 1000 Å, the etching of the thicker electroplated copper mask is negligible. Whereas titanium is etched in the aforementioned solution, the copper etching may be performed in a solution comprising 1% sulfuric acid and 0.5% hydrogen peroxide.

1.6.6.4   Electroless Plating

A method used to ensure the complete filling of vias is electroless plating of nickel. Electroless plating is a process to plate metal without electrical current involved. As a result, it eliminates the seed layer needed in electroplating. To plate nickel on copper, the copper surface must first be activated in a palladium chloride solution. This activation treatment allows palladium to bond to copper at certain sites so that the subsequent nickel plating can nucleate.

A typical electroless plating solution is composed of a cation provider such as nickel sulfate, a reducing agent such as ammonium hypophosphite, and additional additives that help prevent the bath from decomposition, i.e., plating spontaneously. When an activated substrate is immersed in the plating bath at a temperature of 80°C and a pH around 6, nickel cation in the bath are reduced by hypophosphorous acid, and the nucleation of nickel deposition starts at the activated locations. Because nickel readily plates to itself (self-catalysis), the deposition continues and eventually fills the via locations in the dielectric with nickel metal. The reduction reaction can be expressed by the following equations:

$$Ni^{2+} + H_2PO_2^- + H_2O \rightarrow Ni + H_2PO_3^- + 2H^+$$

$$2H^+ + H_2PO_2^- \rightarrow P + 2H_2O.$$
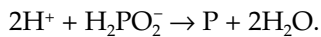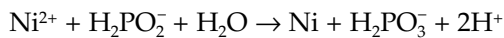
As one can see from the equations, phosphor is codeposited with nickel, resulting in 2–10% (by weight) phosphor in the deposited nickel, depending on the pH of the bath. The quantity of phosphor influences the physical and the electrical properties of the deposited nickel. Therefore, the pH of the plating bath and the concentration of metal ion in the bath must be well controlled. In addition, a uniform deposition requires a minimum temperature variation in the bath. This can be achieved through the heating of the plating solution to desired temperature in an agitated water bath.

Using electroless nickel-plating technique, nickel pillars are formed to connect conductor pads/lines/vias to next layer (see Figure 1.10). Interconnects between the nickel pillars and the next layer can be implemented through sputtering/wet etching, electroplating/etching, or evaporation/lift-off metallization methods. As the metal interconnects are built prior to the
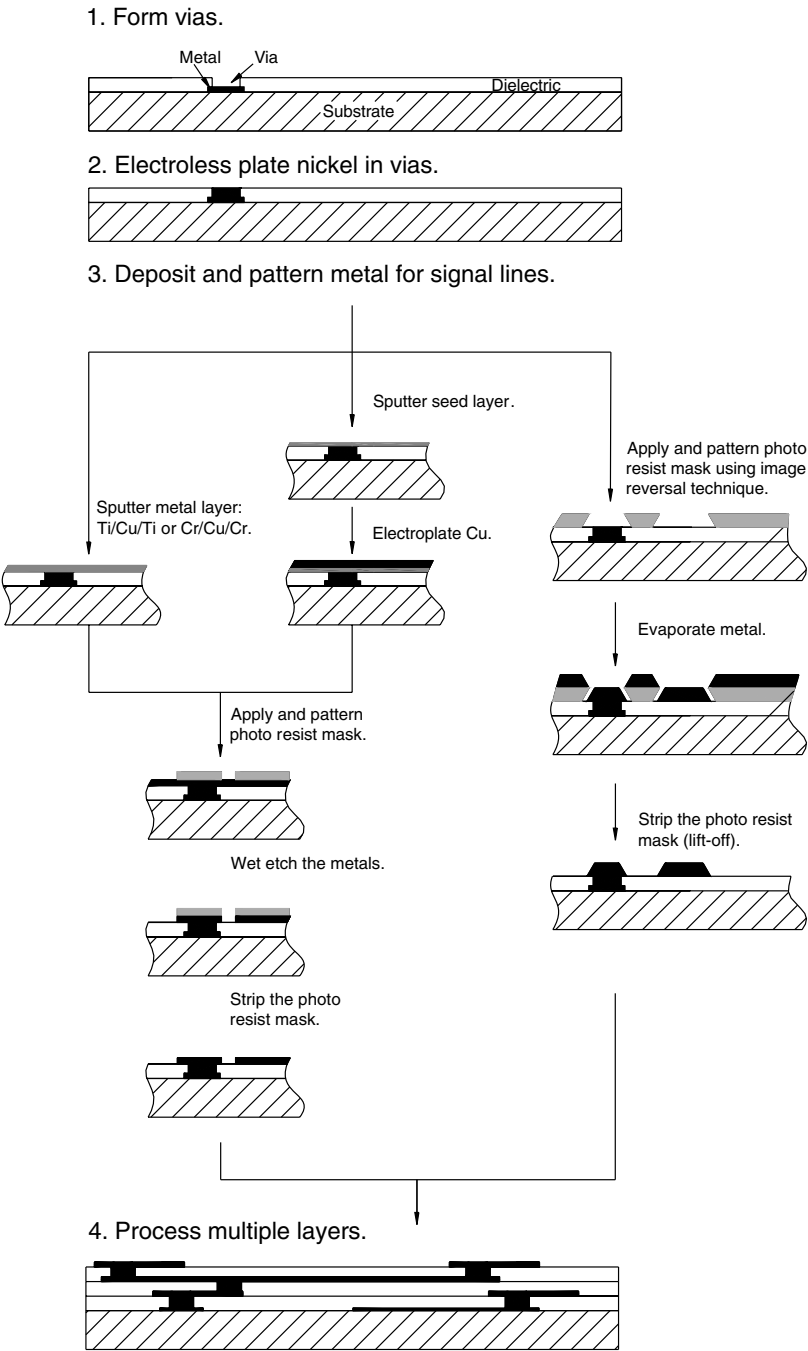
1. Form vias.

Metal   Via

Dielectric

Substrate

2. Electroless plate nickel in vias.

3. Deposit and pattern metal for signal lines.

Sputter seed layer.

Apply and pattern photo resist mask using image reversal technique.

Sputter metal layer: Ti/Cu/Ti or Cr/Cu/Cr.

Electroplate Cu.

Evaporate metal.

Apply and pattern photo resist mask.

Strip the photo resist mask (lift-off).

Wet etch the metals.

Strip the photo resist mask.

4. Process multiple layers.

FIGURE 1.10
Electroless plating metallization: nickel pillar.

application of a dielectric, a nonplanar surface is the consequence. Electroless plating is suitable for metallization of vias in dielectric as thick as 15 μm and also generates stacked vias.

1.6.7   Testing and Rework

Testing plays a crucial role in the fabrication of thin-film interconnects, because no matter how many measures are taken to increase yield, some defects occur during the process. These defects must be caught and corrected before the next process step can be conducted. Testing involves three major stages. The first testing is aimed at evaluating the integrity of the substrate, in the case of a cofired multilayer ceramic substrate. As failure in such a substrate cannot be reworked once the thin-film process starts, a known good substrate must be supplied. Once the metallization of vias and interconnects is finished on each thin-film layer, the second testing is performed to determine if the substrate has sufficient yield to continue in the process. The third testing is carried out on the completed substrate.

The main failures in the thin-film process are shorts and opens of interconnects. Through stringent quality control, 100% inspection, and multiple sets of testing, these problems can be identified. By removing metal between shortened traces, either mechanically or electrically, one can turn a short defect into an open one. An open defect may be repaired by adding another layer of thin film onto the existing layer using a custom mask that routes signal lines to the open nets. After all open defects are identified and repaired, the resulting interconnects should be as reliable as the original. In cases where excessive thin-film defects would make reworking the substrate unrealistic, the thin-film layers can be completely polished/removed so that the ceramic substrate can be reused, and the thin-film process can be restarted from the beginning.

1.7   High-Current Substrates

For power electronic and high-power RF systems, it is not at all unusual for very high currents and voltages to exist in a small substrate area. This creates two primary challenges for the packaging engineer: minimizing the electrical losses, and thermal management. Large currents demand low-resistivity materials because very large power losses and, therefore, heat will be generated in lossy conductors. Likewise, high-power systems are accompanied by high-power dissipation and high operating temperatures in most cases.

As a result, ceramics with thick high-conductivity metallizations are the norm for these types of applications. Ceramics make the most sense for these applications because of their high thermal conductivity and stability at high

operating temperatures. The following sections outline the common methods used to meet these challenges.

1.7.1 DBC Process

For many power systems, hundreds of amperes of current may be flowing through a substrate in a relatively small area. To prevent severe losses in the conductors, the metallization must be very thick and low in resistivity. One approach to this problem is direct bond copper (DBC), which was developed by General Electric in the mid-1970s. Unlike thick-film or thin-film conductors, DBC can be purchased with metal thicknesses up to 0.65 mm (25 mil). Combined with the low resistivity of copper (0.12 mΩ/$\square$) and a high thermal conductivity substrate such as AlN, this approach creates nearly the ideal substrate for this type of application.

The DBC process begins with either an alumina, beryllia, or AlN substrate on which a Cu foil of the desired thickness is placed. This assembly is then heated to ~1065°C in the presence of a controlled amount of oxygen. Under these conditions, a bond is formed between the copper foil and the substrate, which is very strong in nature and is stable up to 850–900°C. In the case of alumina, the bond is formed between the copper and the aluminum oxide as a eutectic alloy at a 1.6 atomic percentage of O_2 at 1065°C by the reaction,

$$CuO + Al_2O_3 = CuAl_2O_4.$$
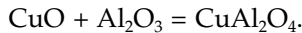
The required oxygen is provided by a copper oxide coating that normally is present on the metal surface. Notice that this reaction takes place just below the melting point of copper, which is 1083°C. For AlN, the substrate is first oxidized to form a thin coating of alumina on the surface of the part by the reaction,

$$4AlN + 6O_2 = 2Al_2O_3 + 2N_2,$$
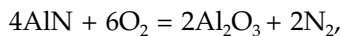
which is usually conducted at a temperature of 1200°C in the presence of oxygen. After the oxidation step, the process proceeds as if the substrate was composed of alumina rather than AlN. The strength of the bond between the AlN and alumina is similar because of the common bonding mechanism, with peel strengths greater than 50 N/cm.

Once the DBC metal is attached to the substrate, the copper metallization can be etched with processes similar to those used in the PCB industry. The key difference is that the metal is far thicker than is used by PCB vendors and requires special etching considerations. The principal method used to etch these conductors is spray etching with a caustic solution. Spray etching is necessary because the amount of material that must be removed is significant, and a standard dunk etch process is ineffective because of saturation of the solution at the copper interface. In contrast, the spray process presents

a fresh solution to the copper surface and flushes away the reacted solution. While etching DBC, care must be taken to consider the conductor widths and spaces that can be achieved. It is unrealistic to expect to etch a 0.65-mm (25-mil) thick conductor to a resolution of less than 0.65 mm (25 mil). The general guidelines are traces and spaces no smaller than 0.25 mm (10 mil) for even relatively thin DBC metals. Thicker metals may require even larger conductor geometries to ensure high substrate yields.

Applications that require precise etching of DBC conductors must be chosen considering the fact that the etching process is lateral as well as vertical. The result is that the etchant has a tendency to produce finer traces than the photomask used due to this lateral etching. An etch-back factor, which is often determined experimentally for a given etching system, is normally used to expand the artwork to account for this over-etch.

This DBC process is simple and offers a number of capabilities beyond plain metallized substrates, including metallizations that extend out beyond the edge of the substrate to form leads, as well as multilayer substrates and via connections. The leaded DBC substrates are formed by using a copper foil that is larger than the substrate desired. In most cases, this foil is stamped to size and may include a variety of prefabricated connections. Multilayer DBC is formed by simply stacking layers of metal foil and substrates, followed by the bonding process described in the previous paragraph. Via connections between these layers are created through holes drilled in the ceramic and the inclusion of rectangular or spherical copper inserts or the welding of the adjacent copper metallizations through the via hole.

1.7.2   Active Metal Brazing (AMB)

Although DBC offers an ideal solution for a number of applications, some applications are best suited to a metal thickness between thick-film printed conductors and the DBC. For these cases, active metal braze substrates are an option. In this process, a copper foil is bonded to a ceramic substrate using a braze alloy. This process is analogous to soldering; however, braze alloys are typically classified as alloys with melting points higher than 500°C. The majority of these alloys use titanium as a key component, which initiates a reaction between the substrate's surface and the braze alloy. In this manner, the braze material wets and forms a strong bond to both the foil and the substrate. The copper foil is often grooved on the side that is bonded to the substrate to facilitate the process. Common braze alloys include Ti–Cu–Ag (for example, 68.8%–26.7%–4.5%), as well as Ti–Al–Cu–N compositions.

The process flow for active metal braze substrates usually involves coating the braze alloy on the ceramic substrate of interest in a paste form, or as a metal foil. The copper foil is then placed on top of the braze alloy, and the whole assembly is heated in an inert atmosphere. The braze alloy melts and forms a strong bond with the copper and substrate. In many cases, the braze alloy and copper are patterned before bonding to eliminate the need for

etching of the braze alloy, which can be difficult. This approach also avoids the need to remove unwanted activated ceramic areas, which are conductive and can be difficult to etch.

Alternatively, a complete coating of braze alloy and copper foil can be placed on the ceramic. In this case, the copper is then etched much like a DBC substrate. However, in this case, an etching or abrasion process must be used to remove the unwanted braze alloy and activated substrate layer.

1.8   Applications

Ceramic chip capacitors, chip resistors, and networks such as RC filters, matching circuits, and terminations have been implemented in ceramics. These components are manufactured in hundreds of millions of pieces per year. Ceramic technology has a long history of use in automotive applications that demand high reliability, excellent thermal performance for high-temperature operation, electrical and dimensional property stability, and high thermal conductivity. Since the earliest use of ceramics in the military electronics during World War II, ceramic interconnect technology was driven by military applications that fully enjoyed the same benefits that ceramics offer for automotive industry. In addition, high interconnect and packaging density was achieved through fine-line patterning, integral passive functions, and bare chip multichip modules.

From its introduction in the early 1980s, LTCC was primarily used in military and medical applications. The advent and explosion of wireless technology in the mid-1990s brought LTCC into the forefront for many commercial wireless products such as cellular phones and wireless local area network (WLAN). The adoption of LTCC was a result of excellent high-frequency performance in terms of dielectric loss (up to 70 GHz) and property stability over a broad frequency range and environmental conditions (–40 to 70°C), coupled with the capability of embedded passives offering very high packaging density. Fine-line patterning and thermal performance was also important for the high-density packaging and miniaturization needed for personal and mobile communications products. The production volumes of modules such as the Bluetooth™ circuits were such that costs were equal or better than organic equivalents.

Table 1.4 summarizes the major application/market segment and the technical attributes that influence the selection of ceramic interconnect technology in that segment. As shown in this table, thermal management — thermal performance, thermal stability, and high-temperature operation as it relates to both operating environment and lead-free assembly — is common to most applications. High-performance electrical property, and the related interconnect density, direct die attach, and embedded passives or embedded functions also span many applications. This comparison demonstrates that many

TABLE 1.4

Technology and Market Comparison

	Automotive	Avionics	Biomedical	Wireless	Communication	Components	Consumer	Digital	Displays	IC Packages	Instrumentation	Military	Optoelectronics	Power Control	Space/Satellite	Telecom
Thermal performance	X	X								X		X	X	X	X	X
High electrical performance	X	X								X		X	X		X	X
Surface resistors																
Embedded passives and functions	X	X		X	X	X				X	X	X	X		X	X
Interconnection density	X	X		X	X			X	X	X	X	X	X		X	
High reliability	X	X	X		X	X	X	X			X	X	X		X	
Manufacturing infrastructure — high volume	X					X	X									
Rework tolerance	X			X				X	X	X			X	X		X
Halogen free	X		X	X			X	X	X	X						
Lead-free solder assembly	X		X	X			X	X	X	X						
Thermal stability	X	X		X				X	X	X	X	X	X	X	X	X

Note: X Indicates ceramic offers significant advantage to the market/application.

application areas find a large number of ceramic properties or attributes to their advantage. It is this combination of many advantageous properties that continue to result in the selection of ceramic in new packaging approaches and markets. This section briefly describes the example ceramic products and applications.

1.8.1   Ceramic Products

Ceramic interconnect technologies are commonly used in four major product formats: component, integrated circuit package, functional module, and system-in-package. Ceramic products are involved in nearly all electronic applications, such as automotive industry, consumer electronics, wireless/telecommunication, military/avionics, and medical science, among other applications. Figure 1.11 to Figure 1.16 show some examples of each product category.

1.8.1.1   *Component*

A surface-mounted LTCC RF band-pass filter (bottom half of Figure 1.11) operates at 942 MHz and, by embedding inductors and capacitors in the 17-layer structure, replaces 9 individual passive components (top half of Figure 1.11). Some layers in the stackup are 50 µm (2 mil) thick for use as the capacitor dielectrics. This filter was designed for cellular phone applications and significantly reduced board space over its discrete equivalent. In addition, assembly time was reduced and, with fewer solder joints for this function, reliability was improved.
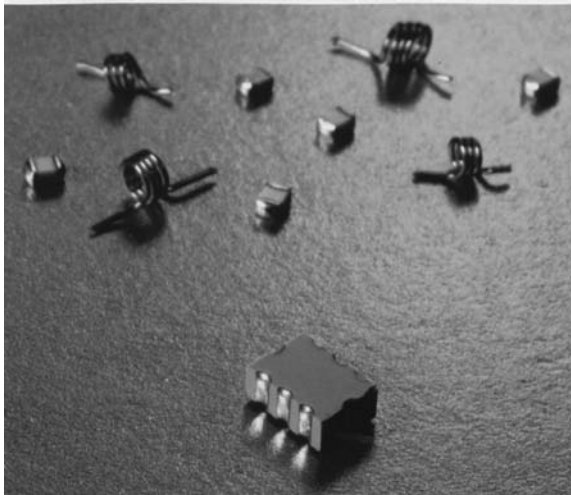
FIGURE 1.11
LTCC band-pass filter. (Courtesy of CTS Microelectronics. DuPont Application Note Reference H-84339.)
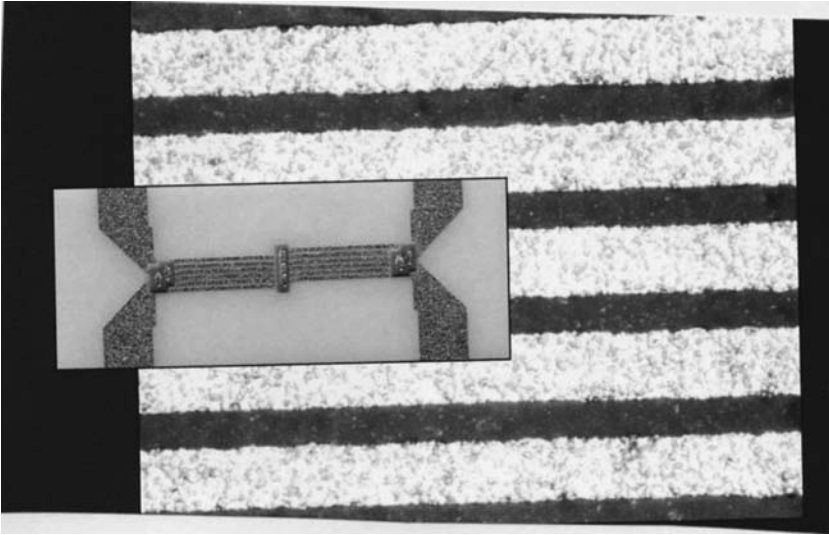
FIGURE 1.12
High-frequency coupler. (Courtesy of Circuits Processing Technology Inc. DuPont Application
Note Reference H-84338.)

Couplers are widely used four-terminal passive devices functioning as
power dividers or combiners in RF and microwave circuits. Typical appli-
cations using couplers include RF amplifiers, power amplifiers, and trans-
mitting/receiving modules for phased-array antenna systems. One type of
coupler is shown in Figure 1.12, a Lange coupler, which has four closely
spaced edge-coupled parallel transmission lines. The line width and spacing
determine the coupling, and the coupled line length, the operating frequency.
Typically, wire bonds are used as crossovers or jumpers to interconnect the
appropriate lines. Thick-film crossovers to replace the wire bonds and etched
conductor lines capable of 25-μm (1-mil) line widths and spaces were used
in this design, resulting in improved coupling, reduced inductance,
improved repeatability from circuit to circuit and lower overall cost. Cou-
plers such as this can be integrated into a module design with thick-film
resistors or be designed as stand-alone components.

1.8.1.2 *Integrated Circuit Package*

In the early stages of semiconductor integrated circuit packaging, ceramic was
the material of choice for its dimensional stability, thermal performance, and
hermeticity. Ceramic dual-in-line (DIP), ceramic quad flat package (QFP), and
ceramic leadless chip carriers (LCC) were all implemented in high-temperature
cofired ceramic (HTCC) packages. As a better understanding of the semicon-
ductor technology and the failure mechanisms became understood, ceramics
packages gave way to plastic packages. However, ceramics are still used in the
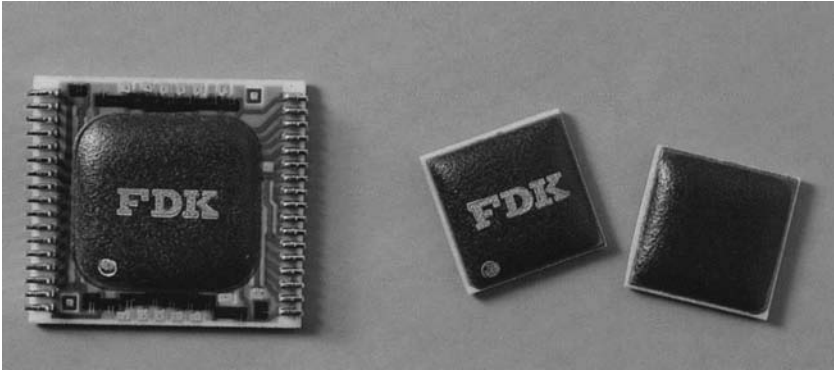
FIGURE 1.13
LCD driver CSP. (Courtesy of Iwaki Electronics Co. DuPont Application Note Reference H-67770.)
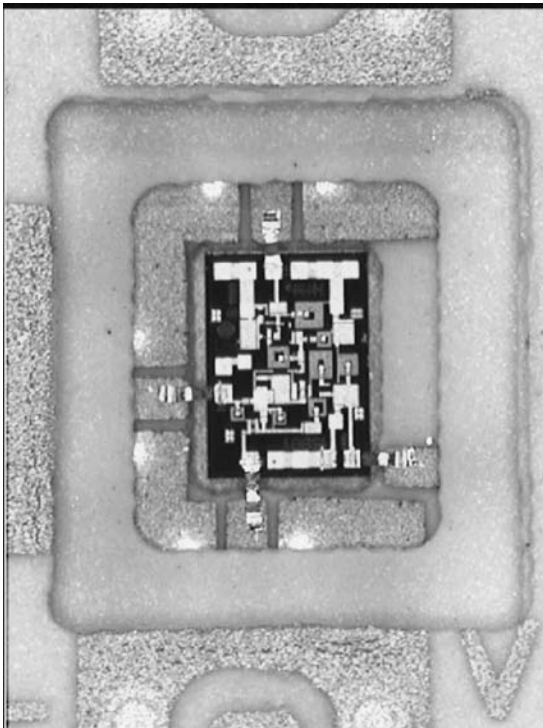
FIGURE 1.14
High-frequency mixer package. (Courtesy of Merrimac Industries Inc.)

most demanding single-chip package applications where high thermal and electrical performance, reliability, and hermeticity are needed.

The chip scale package (CSP) shown in Figure 1.13 was designed for use in LCD driver circuits for laptop computers where there was a need to reduce size and weight. The previous leaded hybrid design was replaced by this 8.9×8.9 mm (0.35×0.35 in.) square ceramic ball grid array (BGA) package, resulting in a circuit area reduction of nearly 70% and a corresponding reduction in the display driver board area of 50%. The thick-film substrate had 32 through holes, 4 metal layers with 200-µm (8-mil) lines on 400-µm (16-mil) pitch with a BGA ball pitch of 1.143 mm (45 mil). The chip scale package facilitated IC test and eliminated the problems associated with the known good die (KGD).

Figure 1.14 depicts a multilayer LTCC package that was designed for a 28 to 31 GHz GaAs MMIC mixer with an integrated local oscillator (LO) amplifier intended for local multipoint distribution service (LMDS) applications [38]. A "cavity down" leadless chip carrier construction with surface-mounted coplanar waveguide (CPW) terminals was chosen to minimize signal lead lengths. The die has a nominal size of $1.32 \times 0.97 \times 0.1$ mm ($52 \times 38 \times 4$ mil) with four 0.1×0.1 mm (4×4 mil) I/O pads. The CPW configuration is used for three of the cavity bond pads and are interconnected with a 75 µm (3 mil) wide ribbon bond for the RF, LO, and IF sections. The fourth pad is bonded with a 50-µm (2-mil) wire bond for DC bias. The die is bonded to the package using a Au–Sn eutectic solder preform. A plastic lid sealed with an epoxy preform encloses the die in the package. The leadless chip carrier was designed using the low loss Green Tape™ LTCC system. The package consists of 14 layers of 125 µm (5 mil) and 50 µm (2 mil) thick Green Tape™ with an overall size of 6×6 mm (236×236 mil). A 100-pF capacitor for the DC bias is integral to the package. Seven layers of 50 µm (2 mil) thick tape with conductors in an interleaved multilayer capacitor format are incorporated in the package base resulting in minimal inductance for the bias interconnection. A plastic lid is recessed so that the module will mount in the cavity down configuration. Minimum line width and spaces are 125 µm (5 mil) and 150 µm (6 mil), respectively, and 125-µm (5 mil) vias are used for signal interconnects. The signal traces use a Ag–Pt composition for wire bondability. Vias are Pt–Pd and the ground conductors Ag for the MMIC epoxy die attach. Packaging the MMIC using LTCC allows for complete electrical characterization in a format suitable for high-volume production, while not compromising performance, and ultimately reducing cost for the end user.

1.8.1.3   *Functional Module*

Ceramic interconnect technologies are capable of integrating various components, such as passive components, RF/microwave devices, ICs, and transmission lines on and/or in a ceramic substrate, forming electronic modules that provide certain functions. Recently, millions of such functional modules have been commercialized in the automotive industry, consumer
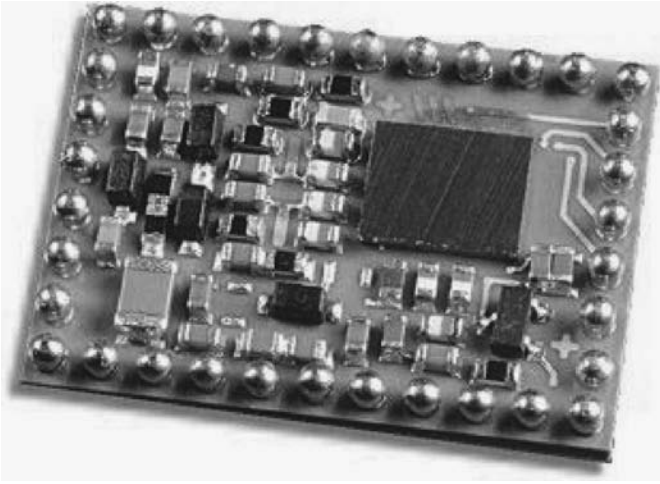
FIGURE 1.15
Bluetooth® module. (Courtesy of Ericsson. DuPont Application Note Reference H-84340.)

electronics, wireless products, military applications, and so on. Figure 1.15 illustrates a widely used Bluetooth® module. An early application of LTCC technology was chosen by Ericsson, originators of the Bluetooth concept and wireless technology, for its high packaging density, electrical properties at 2.45 GHz, robust mechanical properties, and small size through flip-chip compatibility, and BGA form factor for PWB attachment. The maturity of ceramic interconnect technology and the potential for future higher-density integration were also factors in the choice of LTCC. The multilayer technology allowed the integration of the antenna filter and transmitting/receiving baluns into the transceiver substrate.

1.8.1.4 System-in-Package

Ceramic interconnect technology also allows the implementation of electronic products at system levels, producing a system-in-package. Figure 1.16 illustrates such a system for avionics displays through thick-film interconnect technology. The metal package measures 31.75×50.8 mm (1.25×2 in.) with 78 surface mount leads on 1.27-mm (50 mil) pitch. Six conductor layers carry power, analog, and digital signals interconnected with more than 8000 125-μm (5 mil) vias. Minimum line widths and spaces are 125-μm (5 mil). This system-in-package module uses top surface thick-film printed resistors, surface-mounted passives, and wire bonded ICs achieving a component density of over 60 components per square inch. Precision electrical tolerances are maintained over a –55 to 125°C operating temperature range.
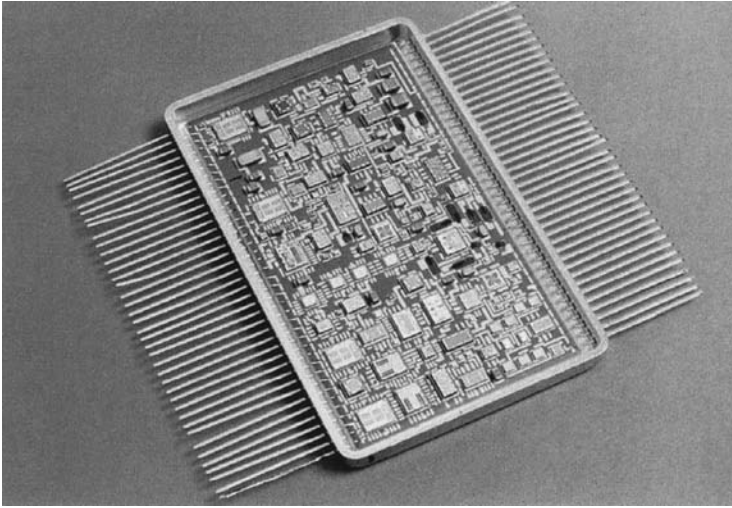
FIGURE 1.16
Avionic display system. (Courtesy of CMAC Microcircuits Ltd. DuPont Application Note Reference H-73159.)

1.8.2   Automotive Industry

Early applications in the 1970s in the automotive industry used thick-film substrates in engine-compartment-mounted silicon-gel-filled, nonhermetic plastic, voltage regulator modules. Thick-film circuits were also used in the passenger compartment for radio audio amplifier modules. Thick-film and LTCC ceramic circuits are now pervasive in automotive applications in engine control modules, antilock brake systems, airbag control modules, entertainment systems, navigation systems, pressure sensors, and transmission-mounted control units. All these applications enjoy high volumes, are cost effective, and proven for very harsh environments, demanding applications in automotive, and even motorcycle and marine systems. Figure 1.17 through Figure 1.19 show some recent examples of automotive ceramic circuits.

1.8.2.1   Engine Control Unit

To achieve lower fabrication cost for automotive under-the-hood engine control unit (ECU), thick-film via and conductor materials capable of cofiring with the dielectric were used in this design. This eliminated two printing and four firing steps for this two-metal-layer circuit. The system had very good reliability, withstanding a temperature cycling environment of –40 to 125°C with solderable conductors on 200-μm (8-mil) pitch for flip chip die attachment and surface-mounted components.
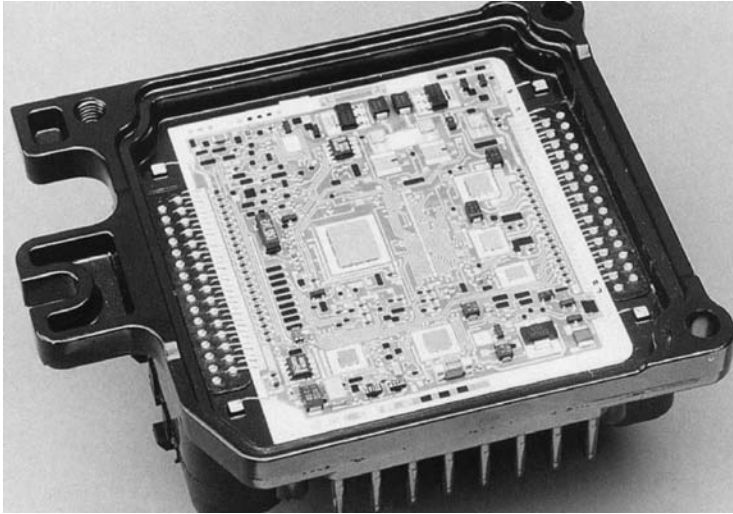
FIGURE 1.17
Engine control unit. (Courtesy of Delphi Delco Electronics. DuPont Application Note Reference H-73162.)
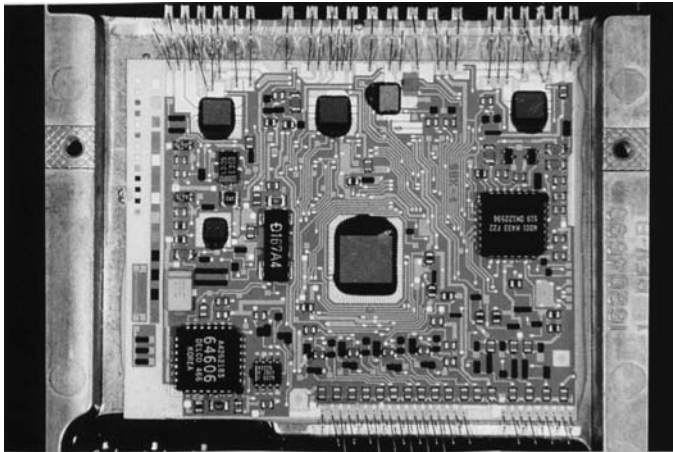
FIGURE 1.18
Antilock brake system module. (Courtesy of Delphi Delco Electronics. DuPont Application Note Reference H-65358.)

1.8.2.2 Antilock Brake System Module

This thick-film hybrid circuit module is part of an anti-lock brake system. It was designed to mount directly on the brake master cylinder where it had to withstand extreme environmental conditions. The module was successfully qualified after being subjected to vibration, brake fluid exposure,
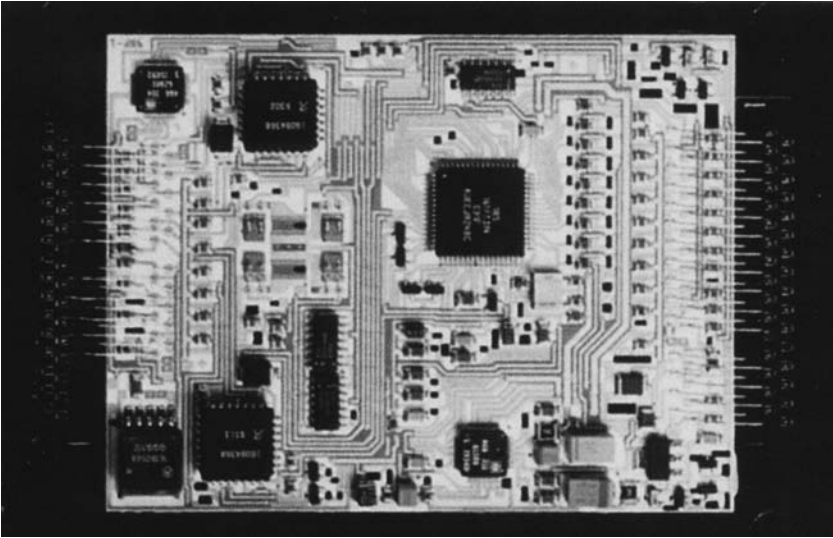
FIGURE 1.19
Electronic fuel injection module. (Courtesy of Delphi Delco Electronics. DuPont Application
Note Reference H-65355.)

ice-water immersion, water jet spray, electrostatic discharge, electromagnetic
radiation, biased humidity, biased thermal shock, and biased thermal
cycling. The thick film on alumina circuit has flip-chip, wire bond, and
surface-mounted soldered ICs. The circuit also packages surface mount tech-
nology (SMT) passives and screen-printed thick-film surface resistors that
are laser trimmed to a 1% tolerance with a TCR of ±100 ppm. The three-
conductor-layer circuit has conductor widths and spaces of 125 μm (5 mil)
and was manufactured in high volumes typical of automotive applications.

1.8.2.3 Electronic Fuel Injection Module

Thick-film ceramic multilayer technology was chosen for this marine engine
control module for its ability to handle high power dissipation and perform
reliably in harsh environments cycling between temperature extremes. Pack-
aging density was also important to reduce the module size for direct mount-
ing on the engine.

1.8.3 Military/Avionics Applications

1.8.3.1 Military Airborne Communications Multichip Module

This multichip module was designed for military airborne communications
applications where small size, high density, and low weight were critical to
system performance. The module shown in Figure 1.20 is a 25.4-mm (1-in.)
square package with a multilayer thick-film substrate with 125-μm (5-mil)
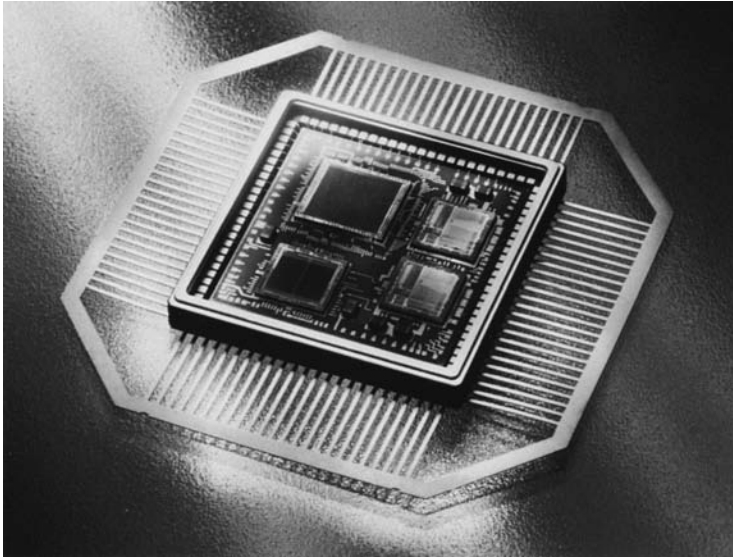
FIGURE 1.20
Military airborne communications multichip module. (Courtesy of CMAC America. DuPont Application Note Reference H-65352.)

chemically formed vias and screen-printed 125-μm (5-mil) lines and spaces. Using direct-chip-attach and gold-wire-bond interconnects resulted in a high packaging efficiency with a 0.42 silicon-to-substrate area ratio.

1.8.3.2 Avionic Multichip Module

The module shown in Figure 1.21 is 36.8-mm (1.45-in.) square in a land grid array (LGA) format with 480 I/O in a package that is 3.18 mm (125 mil) thick, including the lid. Line widths and spaces are 50 μm (2 mil) and vias are 50 μm (2 mil) in diameter. This multichip module met the needs for a rugged, low-profile design for avionics application. The choice of thick film on alumina technology using chemically formed vias and photo-patterned interconnects provided rapid prototyping, reducing the time from design to production to weeks rather than months, with costs lower than MCM-D technology.

1.8.3.3 Cockpit Display Module

This thick-film multichip module substrate (Figure 1.22) packaged the row and column driver circuits for an electroluminescent avionics flat panel cockpit display. The three-conductor-layer substrate is 86.4 × 111.8 mm (3.4 × 4.4 in.) in size with 43 metallized through vias in the alumina substrate for interconnections on both sides of the substrate. On the component side, the 14 row and column driver ICs are aluminum-wire-bonded with a total
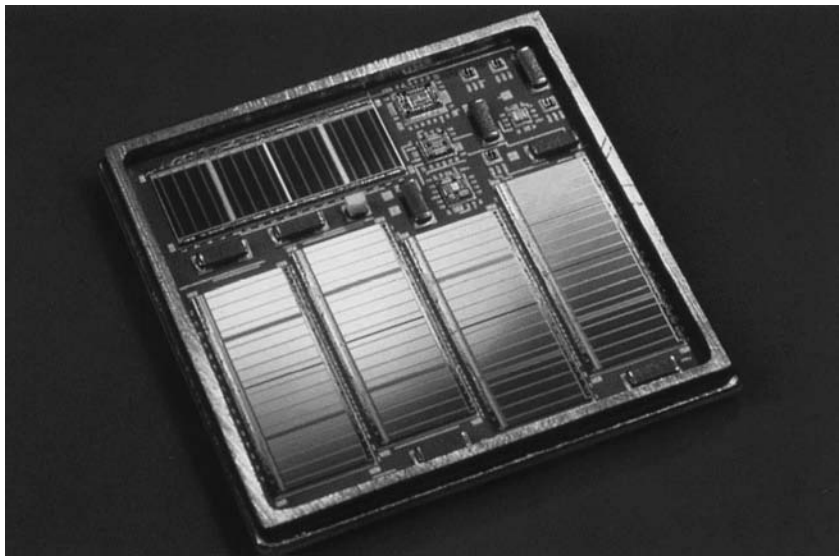
FIGURE 1.21
Avionic multichip module. (Courtesy of Teledyne Electronic Technologies. DuPont Application Note Reference H-65353.)
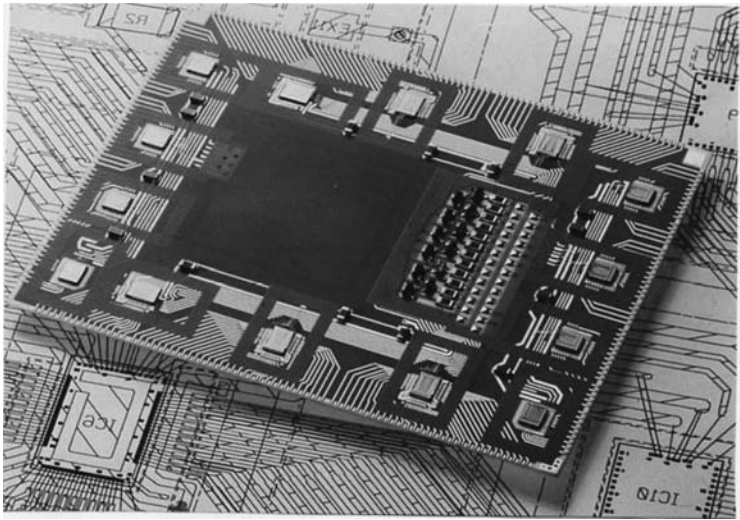
FIGURE 1.22
Cockpit display module. (Courtesy of Barco Microelectronics. DuPont Application Note Reference H-65356.)

of 860 wire bonds. Ceramic lids are sealed over each die on the substrate for hermetic enclosure. The module is mounted on the backside of the EL panel and wire bonded to the panel with over 1100 wire bonds for a total of almost two thousand 30-μm (1.2-mil) wires interconnected to the ceramic substrate.

1.8.4 Commercial Wireless

Figure 1.23 and Figure 1.24 are examples of modules designed for use in the 900-MHz to 2.4-GHz range. New commercial wireless applications of ceramic technology continue to emerge for RF front-end modules, filters, antenna switches, and radio modules.

1.8.4.1 VCO/Synthesizer

This module (Figure 1.23) was an early application of LTCC for wireless products and demonstrated the cost-effectiveness of LTCC in commercial production volumes. The module is a VCO/synthesizer with surface-mounted components, an embedded resonator, and embedded inductors and capacitors. The substrate is about $^1/_2$-in. square and has eight conductor
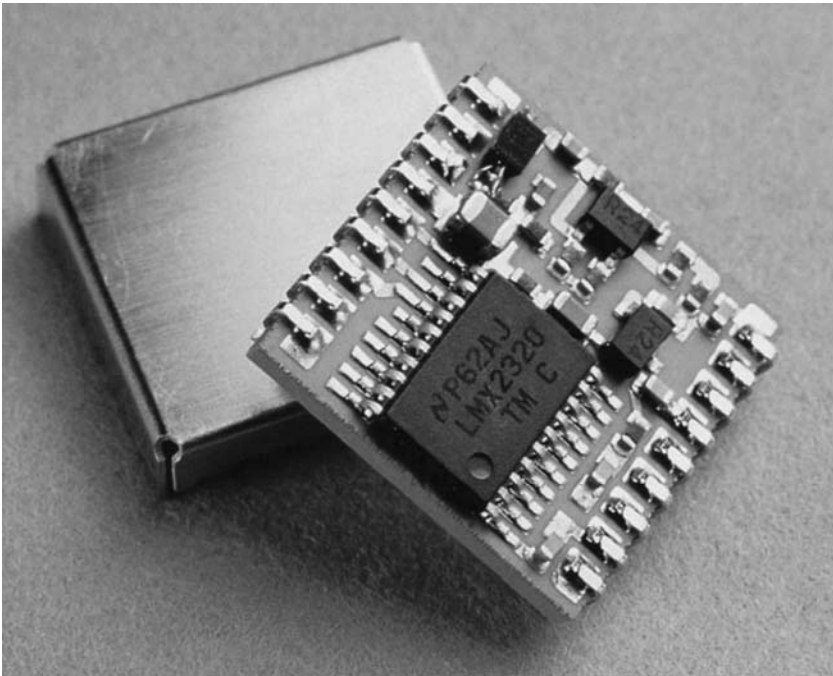
FIGURE 1.23
VCO/synthesizer. (Courtesy of National Semiconductor. DuPont Application Note Reference H-67767.)
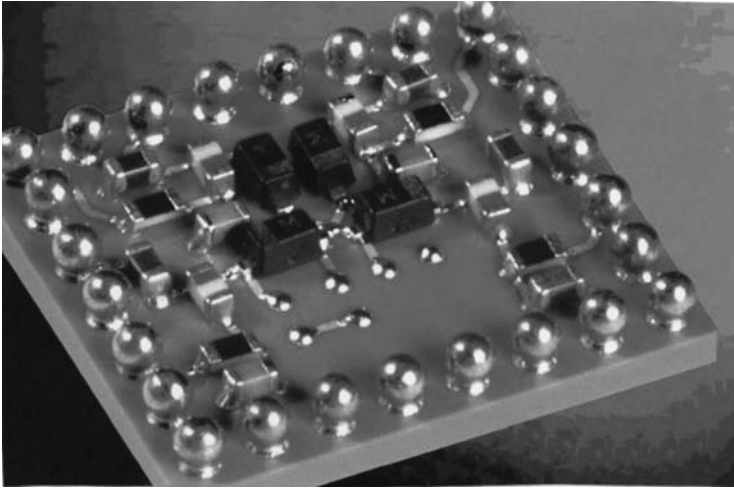
FIGURE 1.24
Antenna switch. (Courtesy of Sorep-Erulec. DuPont Application Note Reference H-84342.)

layers with 8-mil lines and spaces and 6-mil vias. The use of the embedded function and passives reduced circuit size by a factor of four and reduced cost by half.

1.8.4.2 Antenna Switch

This module (Figure 1.24) is an antenna switch/filter module designed for dual-band portable wireless telephones. It combines GSM/DCS/PCS diplexing and receiving/transmitting antenna functions. The 8.9 × 9.9 mm (0.35 × 0.39 in.) LTCC module uses a 26-pad BGA format. In addition to the surface-mounted passive components, the six-conductor-layer structure incorporates 13 embedded capacitors and inductors to form the diplexer and 2 low-pass filters.

1.8.4.3 RF Analog Front End

This LTCC package (Figure 1.25) was designed for a highly integrated RF analog front end for wireless communications using micro ball grid array (μBGA) technology. The package shown is 9 × 9 mm in size with 81 I/O in a 9 × 9 array. The die is wire bonded to pads that interconnect through the substrate to the array terminals on the board-mounting side of the package. Embedded within the substrate are 14 RF bypass capacitors using both high-K and low-K dielectrics. The embedded components and the high I/O capability providing multiple ground connections resulted in improved RF performance and high package density.
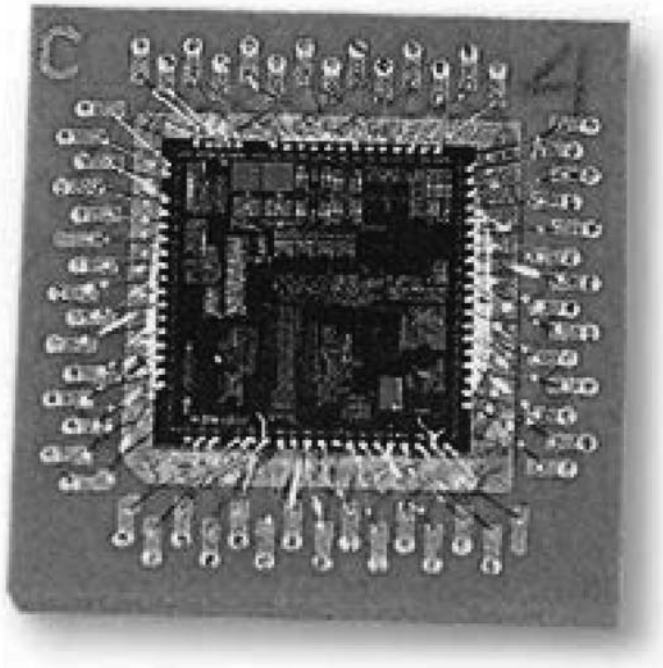
FIGURE 1.25
RF analog front end. (Courtesy of National Semiconductor. DuPont Application Note Reference H-84341.)

1.8.5 Consumer Electronics

The versatility and cost-effectiveness of thick-film techniques is demonstrated in consumer applications, as well. Printed thick film (PTF) materials are used in circuitry in games, membrane touch switches, electroluminescent lighting and signage. Thick-film circuitry is used in personal digital products and specialty applications such as those shown in Figure 1.26 and Figure 1.27.

1.8.5.1 *Digital Camera Circuit*

This credit-card-sized digital camera (Figure 1.26) uses multilayer LTCC materials to reduce the size of the printed wiring board by 50%. The 10-layer circuit used fine-line silver conductors and integrated thick-film resistors having one half the volume of the equivalent chip resistor volume to achieve this significant reduction in size, as well as cost savings.

1.8.5.2 *Hearing-Aid Circuit*

Ceramic technology offers advantages for consumer applications requiring proven high reliability, property stability, and very-high-density packaging

FIGURE 1.26
Digital camera circuit. (Courtesy of Matsushita Electronics Corporation. DuPont Application Note Reference H-84334.)
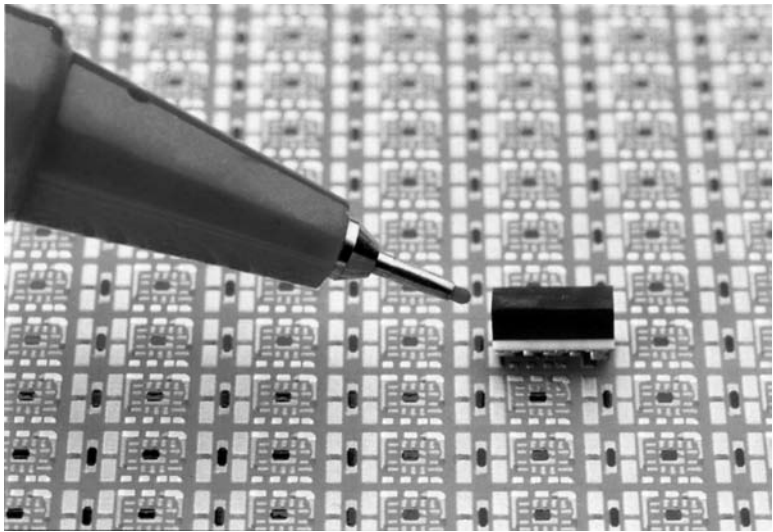
FIGURE 1.27
Hearing-aid circuit. (Courtesy of HEI Inc. DuPont Application Note Reference H-67773.)

capabilities. Miniaturization is a key capability, and good examples are in hearing aids and pacemaker circuitry, applications that have long used thick film, and LTCC. Figure 1.27 shows a thick-film hearing-aid circuit where thick-film technology was used to meet the small size and unique packaging required for this in-ear hearing-aid circuit. The module packaged a flip-chip amplifier IC and a wire-bonded filter IC, and discrete surface-mounted passives on a three-conductor-layer 5 × 2.8 mm (0.198 × 0.110 in.) substrate. The substrate had over three thousand 125-μm (5-mil) vias interconnecting the circuitry.

1.8.6 Space and Satellite Applications

Space and satellite applications are an excellent example of the proven high reliability, thermal performance, and thermal stability of ceramic interconnect technologies, in addition to the high density, functional integration advantages required for these applications. Figure 1.28 and Figure 1.29 are examples of thick-film and LTCC satellite circuitry.

1.8.6.1 *Satellite Control Circuit*

This multilayer LTCC (Figure 1.28) circuit regulates the power for satellite microwave modules. LTCC was chosen for its high density, enabling weight
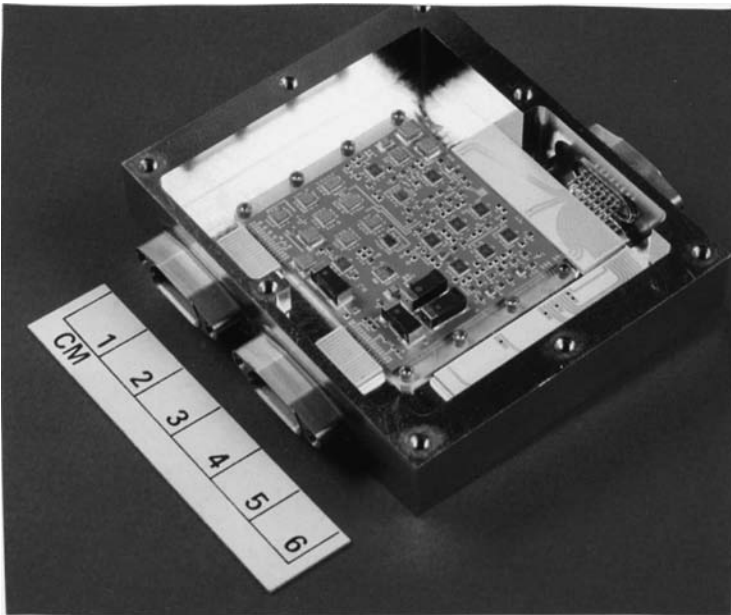
FIGURE 1.28
Satellite control circuit. (Courtesy of Space Systems Loral Inc. DuPont Application Note Reference H-78276.)
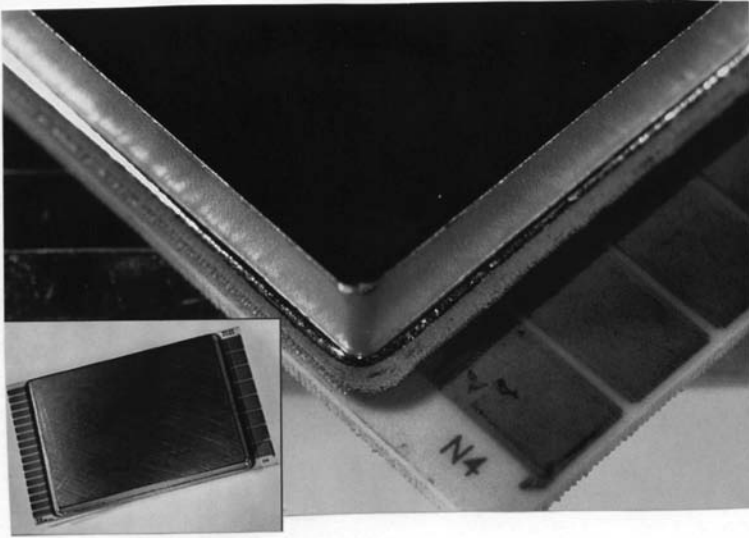
FIGURE 1.29
Satellite power control module. (Courtesy of Space Systems Loral Inc. DuPont Application Note Reference H-78298.)

reduction through the integration of multiple functions into one module and also higher reliability through the reduction of interconnects. RF stripline and microstrip circuits are used in this eight-layer multilayer circuit. Two layers were added to allow the use of 250-μm (10-mil) lines and spaces to minimize line loss. The circuit successfully passed rigorous aerospace performance standards including temperature cycling of –55 to 125°C.

1.8.6.2   *Satellite Power Control Module*

This communications satellite power control module is designed to regulate power between the solar-array panels and the spacecraft. The module has to withstand severe environment extremes and perform reliably for up to 15 years. Hermeticity is a requirement for this application, and thick-film technology with low-temperature brazing alloy was used to seal the module. The thick-film braze material applied to the multilayer substrate produces a uniform concave solder fillet between the cover and thick-film dielectric seal ring, absorbing much of the stress due to thermal expansion mismatch of the metal cover and the substrate. Seal integrity was demonstrated by environmental testing, including thermal cycling for 100 cycles from –65 to +150°C followed by mechanical shock of 1500 g and successfully passing fine and gross leak tests. The units also withstood temperature extremes as low as –100°C. This design using the substrate as the package reduced costs

over the conventional approach of placing a substrate into a hermetic metal package and avoided problems associated with glass to metal feed-throughs.

1.8.7   Telecommunications

Telecommunication line cards and switching circuits were early applications of thick-film circuitry employing its high reliability and interconnection-density capabilities. The Telecom Central Office power control and power supply circuits were also implemented in ceramic technology for the capability to dissipate high heat and maintain dimensional stability. This is important where backup power is required to maintain operation during primary power outages when cooling is restricted. Perhaps one of the best examples of integral component application is in a Motorola satellite handset circuit for voice communications. This circuit, designed in the mid-1990s, had 26 embedded components and 16 surface-mounted components in a 10-mm square 10-layer LTCC circuit. The component density is unmatched by any organic interconnection technology, and far greater density than the estimated 2007 capability of some of the new embedded component technologies are now being developed for printed wiring boards.

1.8.7.1   Digital Switch Line Card

Line cards used in telecommunication system digital switches are the interfaces between the analog phone lines and the digital switch, and provide A/D conversion, power to the phone line, over-voltage protection, ringing current, and control functions. This line-card module (Figure 1.30) packages surface-mounted ICs and discrete active component packages, chip capacitors, and 33 thick-film resistors on the substrate with soldered substrate clip terminals. The ability to functionally laser-trim resistors to tight tolerances is also a key factor in this application. The resistors are trimmed to absolute tolerances as tight as ±0.5% and some with ratio matching of multiple resistors to ±0.25%. Millions of thick-film hybrid circuits have been used in this application where ceramic technology was chosen for proven high reliability and high-density packaging enabled by fine features and integral surface resistors.

1.8.7.2   High-Speed Switch

This module (Figure 1.31) functions as a high-capacity and high-data-rate telecommunications switching circuit. An IC was designed that was capable of operating at 10 Gbps with 24 I/O channels; however, the circuit speed, overall size, and feature size were such that printed wiring board technology could not meet the IC pad size, controlled impedance, and dimensional control or cross-talk requirements, and still be cost-effective. Photopatterned thick-film technology was chosen that was capable of 50-µm (2-mil) features for IC pad fan-out and precise line definition and spacing for the 50-Ω microstrip
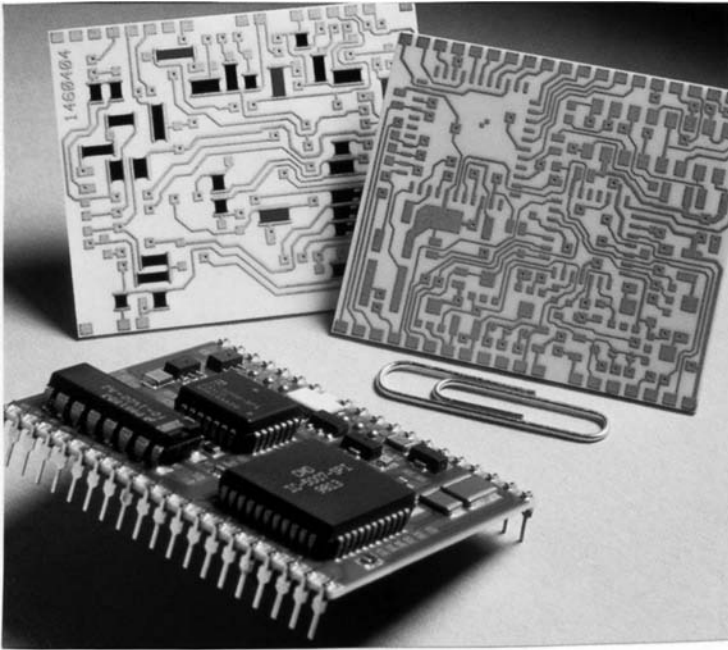
FIGURE 1.30
Digital switch line card. (Courtesy of AG Communication Systems. DuPont Application Note Reference H-84330.)

lines, enabling the full capability of the switching IC to be realized in the available space.

1.8.8   Instrumentation

Test instruments have long used ceramic interconnect technologies for the capabilities of high-frequency performance and dimensional and environmental stability. Component and interconnection density is also important in those applications where parasitics must be minimized, such as in oscilloscope front ends and probes. Figure 1.32 and Figure 1.33 present some high-performance instrumentation applications of ceramics.

1.8.8.1   *Oscilloscope Data Acquisition Circuit*

Thick-film technology was used in this high-speed data acquisition system in a high-performance digital oscilloscope. Circuit size reduction and performance improvements were needed to achieve a 2-Gbps sampling rate. High circuit density was obtained using etched gold conductors to form 50-μm (2-mil) lines and spaces and integral resistors, capacitors, and inductors in this 7.62×88.9 mm (3×3.5 in.) substrate. The use of ceramic interconnect
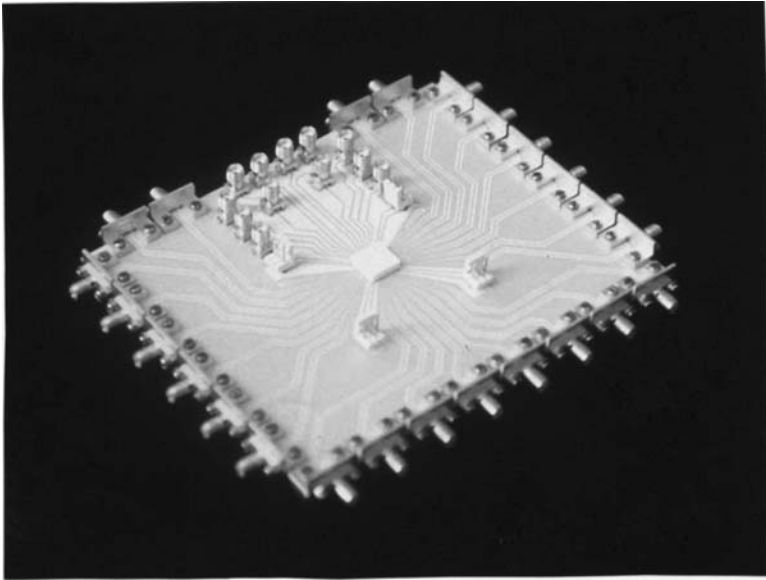
FIGURE 1.31
A 10-Gbps switching module. (Courtesy of Nortel. DuPont Application Note Reference H-67772.)
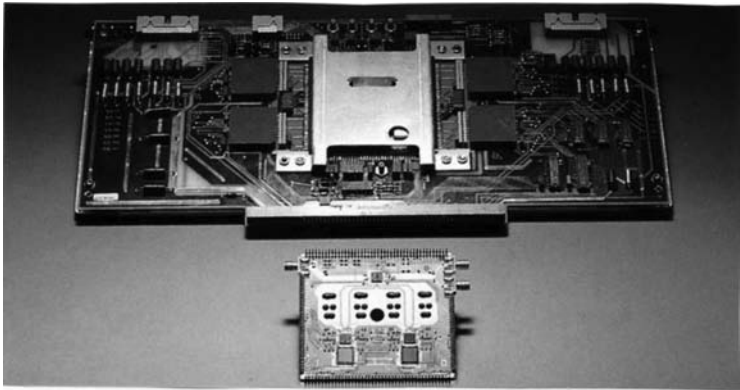
FIGURE 1.32
Oscilloscope data acquisition circuit. (Courtesy of Hewlett-Packard Corporation. DuPont Application Note Reference H-78284.)

technology allowed the circuit size to be reduced to one eighth that of the prior printed wiring board design (Figure 1.32). In addition, a 4X performance increase and improved power dissipation for the 20 W of heat generated by the circuitry was realized.
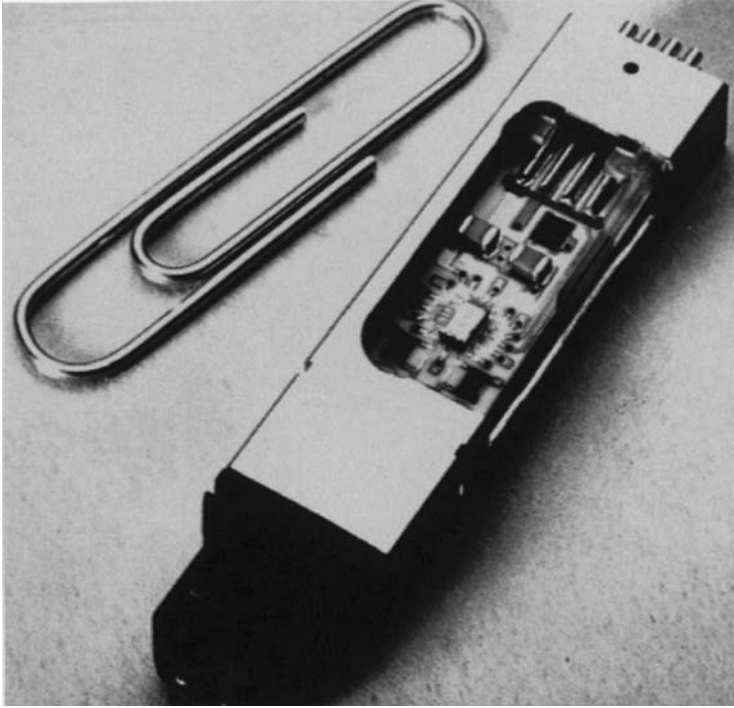
FIGURE 1.33
Differential probe. (Courtesy of Tetronix Inc. DuPont Application Note Reference H-67771.)

1.8.8.2 Differential Probe

Thick-film materials were used to create this ceramic multichip module (MCM-C) circuit (Figure 1.33) for a high-frequency, low-input capacitance active differential probe. The choice of ceramic was based on the need for high-density packaging, high-frequency material properties, the ability for active laser trimming of resistors and capacitors, and high thermal conductivity. The probe operates with a bandwidth of more than 1 GHz. Passive components are screen printed on both sides of the substrate dissipating 0.8 W.

1.8.9 Power Supply and Control

1.8.9.1 DC-to-DC Converter

DC-to-DC converters provide high-efficiency conversion of high voltage used for power distribution to lower voltages used by individual circuits. Figure 1.34 demonstrates such a converter. This series of converters were designed for thermal performance to meet the stringent requirements of aircraft and space vehicles. Thick-film materials on both alumina and beryllia substrates were used with both 25-μm (1-mil) diameter wire bonds for IC signal connections and large-diameter (up to 20 mil) wire bonds for high-current interconnections.
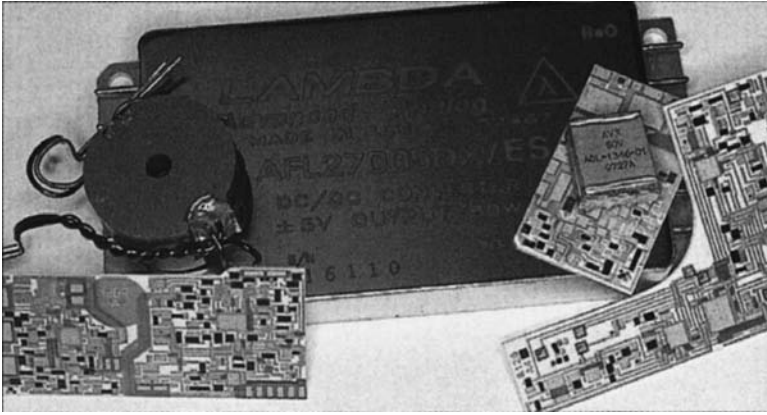
FIGURE 1.34
DC-to-DC converter. (Courtesy of Lambda. DuPont Application Note Reference H-84331.)

Actively trimmed integral surface resistors enabled circuit optimization. The converters successfully pass centrifugal force tests up to 10,000 g, thermal cycling from –65°C to +150°C, and a 1500-g mechanical shock test following thermal cycling. The use of thick-film ceramic technology helped reduce the size, weight, and cost of these aerospace modules.

1.8.9.2 Switching Power Supply

This switching power supply (Figure 1.35) was designed for high-reliability telecom applications where there was a requirement for a light-weight,
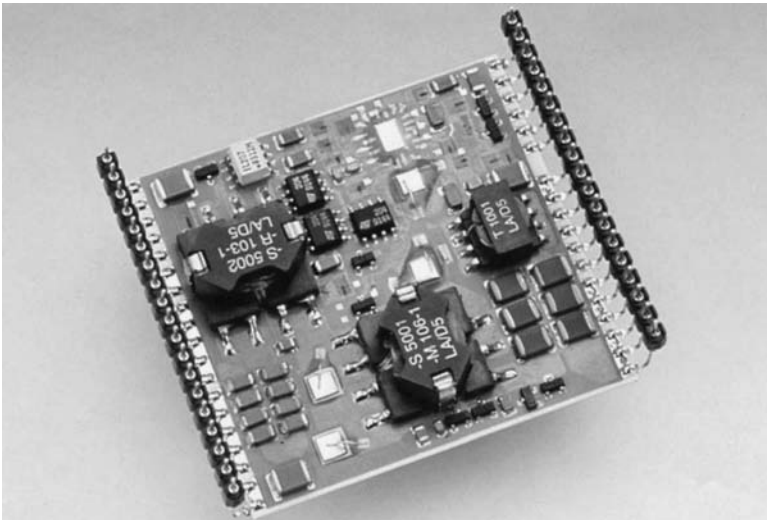
FIGURE 1.35
Switching power supply. (Courtesy of Siemens. DuPont Application Note Reference H-65354.)

low-profile package in a plug-in, board-mounted, in-line format. The two-and three-metallization-layer hybrid circuit designs of this type used bare-die and surface-soldered components, and met the thermal and electrical performance requirements with a service life of more than 15 years at a 40°C operating temperature.

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2

Electrical Design, Simulation, and Testing

Daniel I. Amey and Kuldeep Saxena

CONTENTS

2.1   Introduction

Ceramic thick-film hybrid technology is a mature technology. There are a number of books, texts, short courses and workshops, and design tools that deal with the design of substrates and thick-film hybrid modules [1]. Multilayer printed wiring board materials, processes, and design tools are similarly well defined [2]. Low-temperature cofired ceramic (LTCC) technology is relatively new for broad-based applications, and design tools tailored to LTCC are emerging. However, many of the characteristics that are unique to, and influence the design of, LTCC ceramic substrates and packages are not well understood. This chapter discusses some of the basics of multilayer design, and the key material and process considerations unique to multilayer LTCC design.

The material in this chapter is based on analytical formulas for the various multilayer structures, using the parameters defined later, which are representative of most LTCC material systems. Interconnection impedance is influenced or affected by the material properties, conductor and dielectric dimensional variations, ground or reference plane configuration, as well as the proximity of other interconnects and components to the circuit, which are unique and specific to each design. This section provides a first-order estimate based on nominal values of impedance-determining properties, and describes design and worst-case tolerance for single-conductor interconnections. More exact data would result from field solver simulations. The intent is to provide a starting point to understand the design approach, possible

structures, and basic design trade-offs, which would then be supplemented by simulation tools to finalize design parameters.

2.2   Electrical Properties

To be able to integrate and use ceramics as substrates for the electrical circuits, the reader should be aware of the properties of these materials that make them useful for such applications. Ceramics are electrical insulators, but they do conduct electricity above the dielectric breakdown voltages that are of the order of 1000 V/mil of dielectric thickness. The electrical properties of the ceramics are very important parameters of high-frequency designs; the dielectric constant, for example, will determine the device size, and other properties such as the loss tangent will give a fairly good idea about device behavior at higher frequencies of interest. So in this section, a brief overview of the electrical properties has been provided.

2.2.1   Conductor Properties

2.2.1.1   *Conductivity*

Ceramic technology offers a wide choice of conductor metallizations, and various conductor technologies are used with ceramics. Screen-printed and photo-defined, thick-film, thin-film, electroplating [3], electroplating over thick film, and direct bond copper (DBC) [4] are the most prevalent metallizations.

It is common to refer to thick-film metallizations as "gold," or "silver," or "copper" — the conducting metal component in the paste. It is important to keep in mind that the typical conductors for ceramics are compositions of glasses, ceramic powders, and conducting metal particles. As a result, the conductivity of typical gold conductors is 30–50% that of bulk copper and that of typical silver conductors, 70–90% that of bulk copper. The conductivity of plated thick-film and DBC approach that of bulk copper. Table 2.1 summarizes the properties of typical conductors for ceramic application.

2.2.1.2   *Skin Depth*

The skin depth is the distance over which electrical conduction will take place in a conductor; it could be a thin-film, thick-film, or bulk material. Precisely stated, the skin depth is the distance into the conductor at which the electric field drops off to $1/e$. In practice, very little conduction occurs in the portion of the conductor that is greater than a few skin depths. This distance is always from the surface of the conductor carrying the radio-frequency (RF) current, which is always the surface nearest to the media in

TABLE 2.1

Properties of Common Conductors Used in Ceramic Substrates

Composition	Primary Function	Typical Fired Thickness µm	Resistivity mΩ
Ag	Cofired signal-lines and electrodes	9	3.3
Ag	High-conductivity cofired signal lines	18	<3
Ag	Large-area cofired planes	9	8
Ag	Via fill	250 dia/100 thick	<3
Ag	Cofired photo-defined signal lines	10	<3
Ag/Pd	Mixed metal via fill	10	<10
Ag/Pd	Cofired solderable conductor	13	<60
Au	Cofired signal lines wire-bondable	9	<5
Au	Large-area cofired planes wire-bondable	9	<5
Au	Au and Al wire bondable	9	<5
Au	Via fill	—	—
Au/Pt	Cofired solderable conductor	12	<35

which the electromagnetic (EM) wave propagates. Skin depth is a strong function of the frequency and decreases with increasing frequency. So, in the microstrip-type configuration, the RF currents reach a maximum value at the lower part of the top conductor line and the upper part of the ground plane.

The other two parameters on which the skin depth depends are the resistivity of the conductor and the relative permeability of the material:

$$SkinDepth = \delta_s = \sqrt{\frac{2\rho}{2\pi f \mu_0 \mu_r}}$$

where
ρ = bulk resistivity (ohm-meters)
f = frequency (hertz)
μ_0 = permeability constant (henries/meter)
μ_r = relative permeability

The relative permeability is a measure of how a magnetic field interacts with a material and can often be considered a constant for a given material. The net result of this skin effect is that conduction is limited to a thinner region of a metallization at higher frequencies. Consequently, the net conductor loss may appear lower if the skin effect is taken into account. In practice, conductor thickness of more than a few skin depths is of little value. However, the reader should note that at low frequencies, the skin depth becomes very large.

2.2.1.3 Effect of Surface Roughness

Roughness of the conductor and dielectric is an important property for high-frequency performance. The increase in attenuation due to roughness is a complex function of roughness and skin depth [5].

$$\alpha_c^1 = \alpha_c \left\{ \text{Roughness Correction Factor} \right\}$$

$$\alpha_c^1 = \alpha_c \left\{ 1 + \frac{1}{90} \text{ ARCTAN} \left[1.4 \left(\frac{\text{rgh}}{\delta_s} \right)^2 \right] \right\}$$

where "rgh" is the average root-mean-square (RMS) roughness, and "δ_s" is the skin depth.

This correction factor is plotted in Figure 2.1. In a perfectly smooth surface (no roughness), there is no increase in conductor attenuation as a result of roughness. If the roughness is 50% of the skin depth, there is a conductor attenuation increase of 1.21, or 21% increase in conductor loss over a perfectly smooth conductor, due to roughness. If the roughness equals the skin depth, the increase in conductor attenuation is 1.61, or 61%.

The typical roughness of LTCC material is 13 µin., which falls between 96% alumina, which has a typical roughness of 17 µin., and the more expensive unpolished 99% alumina, which has a typical roughness of 4 µin. In a
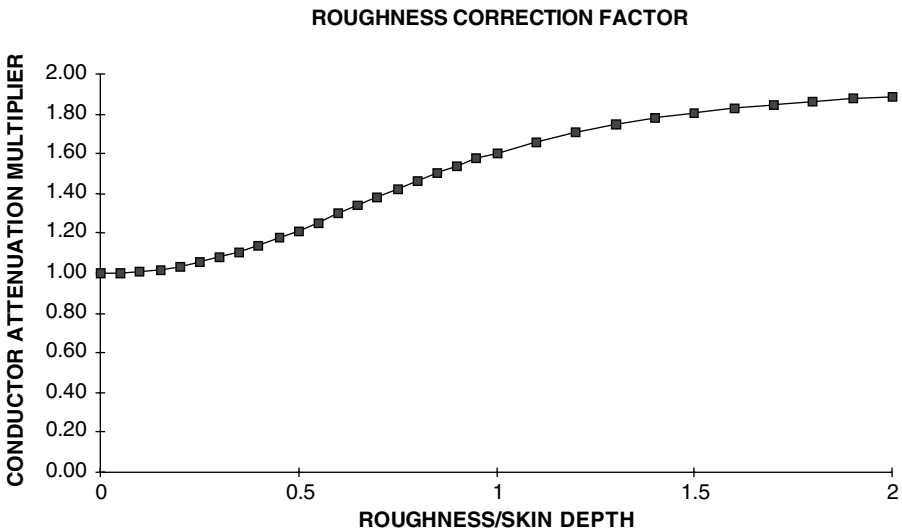
FIGURE 2.1
Conductor attenuation correction factor for roughness.

thick-film silver conductor with a conductivity of 0.71 that of copper, the skin depth is on the order of 1.75 μm or 69 μin. at 2 GHz, 1.1 μm or 44 μin. at 5 GHz, and 0.78 μm or 30.9 μin. at 10 Ghz. Table 2.2 tabulates the values of the increase in conductor attenuation (with all other properties remaining the same) for typical substrate roughness values under these conditions.

2.2.1.4   *Conductor Geometry*

Conductor geometry in ceramic technology varies with the patterning method and processing. This is similar to printed wiring boards where, for example, etch factors result in trapezoidal conductor cross sections. In ceramic multilayer technology, screen-printed conductors have an oval cross section. Conductor thickness will vary based on the paste material, screen properties, e.g., emulsion thickness and mesh and, of course, the number of prints. Photo-patterned technology produces conductors with a near-rectangular cross section and very straightedge features. Figure 2.2a shows typical screen-printed and photo-patterned conductors, and Figure 2.2b demonstrates the fine line (50-μm lines with 50-μm spaces) and excellent line definition of the photo-patterned Fodel® process. This feature results in improved high-frequency performance over screen-printed conductors [6]. The conductor geometry within an LTCC substrate is also influenced by the lamination process. Conductors patterned in the green state on tape layers are slightly compressed when laminated. In many applications this effect is negligible, but it may be necessary to take this into account if, for example, conductor to ground plane spacing or dielectric thickness separation to other conductors is critical. If necessary, the lamination process can be adjusted to control this effect.

2.2.2   Dielectric Properties

Considerable research has been done to find and predict the microscopic basis of the useful dielectric properties of ceramics, especially for LTCC applications, that would lead to the design of next-generation ceramics for advanced electronic applications. This kind of research suggests the importance of the dielectric properties of ceramic materials. Candidate technologies for RF and microwave devices should have low dielectric losses and offer a range of permittivity values. Also, as the operating temperature range of the devices increases, an important factor to consider is the temperature stability of the resonant frequency. The development of LTCC materials with lower loss tangent values and better control of dielectric properties is on the rise.

The dielectric constant, which determines how the dielectric material interacts with an electric field, is a characteristic property of dielectrics. It is a measure of the charge retention capacity of a medium. In general, low dielectric constants result in faster substrates, whereas large dielectric constants

TABLE 2.2

Substrate Material Comparison, Roughness Effects

Substrate	Typical Roughness μin.	rgh/δ_s 2 GHz	Attenuation Increase 2 GHz	rgh/δ_s 5 GHz	Attenuation Increase 5 GHz	rgh/δ_s 10 GHz	Attenuation Increase 10 GHz
99.6% ALUMINA	4	0.058	1.003	0.092	1.01	0.13	1.02
951 GREEN TAPE™	13	0.188	1.03	0.298	1.08	0.421	1.16
96% ALUMINA	17	0.246	1.05	0.39	1.13	0.551	1.26
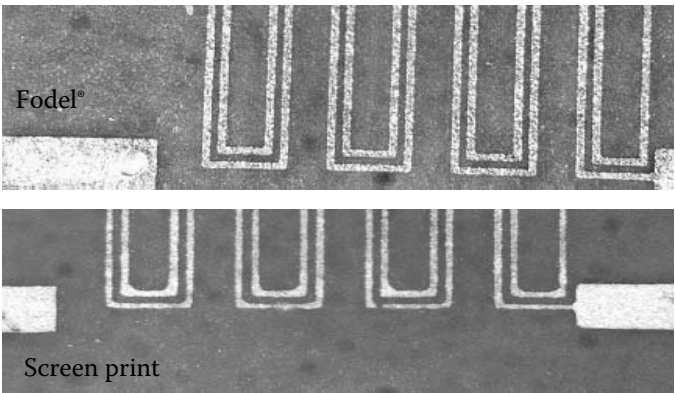
FIGURE 2.2A
Fodel Ag vs Printed Ag (50 µm lines).
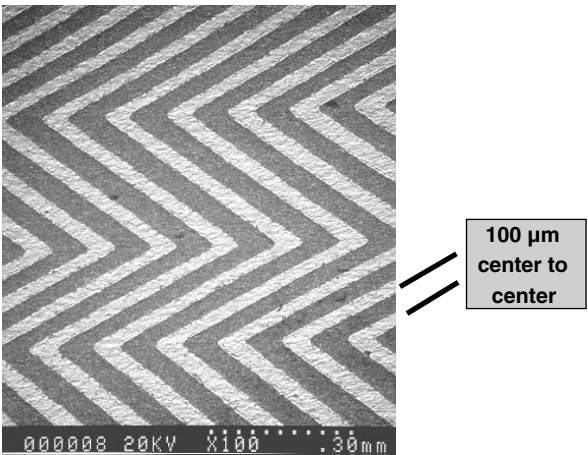
FIGURE 2.2B
Fine line pattern cofired Fodel® 6453 on 951 Green Tape™.

result in slower substrates. The terms *slow* and *fast* relate to the charge retention of these substrates. It is also called the *relative permittivity* (ε_r). The dielectric constant is the real part of the complex permittivity, whereas the imaginary part is related to the loss of the material. The loss is generally expressed in terms of the loss tangent, tan δ:

$$\tan \delta = -\frac{\varepsilon''}{\varepsilon'} = \frac{\sigma}{\omega\varepsilon}$$

TABLE 2.3

Properties of Selected LTCC Materials

Parameter	Value	Minimum	Maximum
Dielectric constant (E_r)	7.8 ± 0.1	7.7	7.9
Conductor thickness (mil)	0.35 ± 0.08	0.27	0.43
x–y Shrinkage (%)	12.7 ± 0.3	12.4	13
z-Axis shrinkage (%)	15 ± 0.5	14.5	15.5
Fired thickness (mil)	3.8 ± 0.3	3.5	4.1
Fired thickness (mil)	5.5 ± 0.4	5.1	5.9
Fired thickness (mil)	8.5 ± 0.7	7.8	9.2
Screened line-width tolerance (mil)	± 1	—	—
Photo-defined line-width tolerance (mil)	± 0.2	—	—

where σ is the material conductivity, ω is the radian frequency ($2\pi f$), ε' is the real part of the complex permittivity, and ε'' is the imaginary part of the complex permittivity. The dielectric constant and other key parameters for several LTCC materials are summarized in Table 2.3.

2.2.3 Impedance Control

Impedance is the electrical property defined as the total opposition a device or circuit offers to the flow of an alternating current (AC) at a given frequency. It comprises resistance, conductance, inductive reactance, and capacitive reactance. Close control of circuit impedance is important to maintain signal integrity. In general, when the electrical length of a signal path exceeds one-third the signal rise or fall time, a controlled impedance interconnect should be used. High-frequency applications necessitate the maintenance of closely matched interconnection impedance, both within a structure and at the various interfaces in an interconnection system. The primary impedance-determining parameters in a planar interconnection system are:

- Circuit configuration
- Substrate material dielectric constant
- Conductor width
- Conductor thickness
- Dielectric thicknesses

The circuit configuration (microstrip, stripline, etc.) is the basic structure of the interconnect. The general relationship of the physical parameters to impedance is such that impedance is an inverse function of conductor width, dielectric constant, and conductor thickness, and a direct function of the dielectric thickness or spacing between the signal conductor and the impedance reference planes.

The impedance reference plane is preferably a signal ground plane. In practice, the reference plane should be the system signal ground. In digital applications, both voltage and ground planes can serve as impedance reference planes, as there is, typically, a large amount of capacitance between the power planes, which closely couples the voltage plane to ground for a good AC reference for the high-frequency signals. If both digital and analog signals are in the system, the sharing of voltage or ground planes must be carefully analyzed to ensure that unwanted coupling does not result. Also, high-current-carrying planes may not be suitable signal reference planes, and separate power distribution and signal reference planes may be needed.

2.2.3.1   Gridded Ground

Typical LTCC design guidelines recommend that ground/power plane coverage not exceed 70% (for example, a grid with 0.010-in. line and space). Although this is important for mechanical integrity, processing, and manufacturability, the use of a solid plane is preferred for electrical performance, and solid planes may be used in selective areas. Many studies have been performed for meshed or gridded planes. These studies examine the effect on high-frequency properties of the ratio of conductor to the opening beneath the conductor, optimal orientation (angle) of the mesh to the signal conductor, impedance, impedance discontinuities, etc. [7].

A design methodology for gridded or meshed planes that provides the manufacturability advantages with minimal degradation of high-frequency signal performance was developed for LTCC [7]. This method provides for a meshed reference (power or ground) plane while maintaining a solid conductor path beneath the signal conductor. It can be thought of as an image of the signal conductor layer that is projected onto the reference layer and then interconnected to form a grid. It can also be thought of as the image of the signal layer interconnections superimposed on a grid. This method of ground or reference plane design preserves a solid return path for the signal conductor, and allows a reference grid or mesh without discontinuities along the signal path. It is desirable to have the reference plane conductor wider than the corresponding signal conductor. If there are a number of parallel lines, a solid area beneath all lines is preferable if it is within the 70% limit, taking care to avoid unbalanced metal coverage without compensating layers. Of course, if full solid planes can be incorporated within the limits of the manufacturing guidelines, they should be used, and if the reference planes are used as primary power planes, direct current (DC) distribution or voltage drops must also be considered. Figure 2.3 illustrates the concept: Figure 2.3a depicts a signal conductor layer, Figure 2.3b depicts the reference plane for that layer with the connecting grid paths, and Figure 2.3c depicts the finished reference plane resulting from this method. The reference plane layout may be further optimized for a specific design [8].

(a) SIGNAL LAYER

(b) SIGNAL LAYER IMAGE SUPER IMPOSED ON GRID

(c) FINISHED REFERENCE LAYER
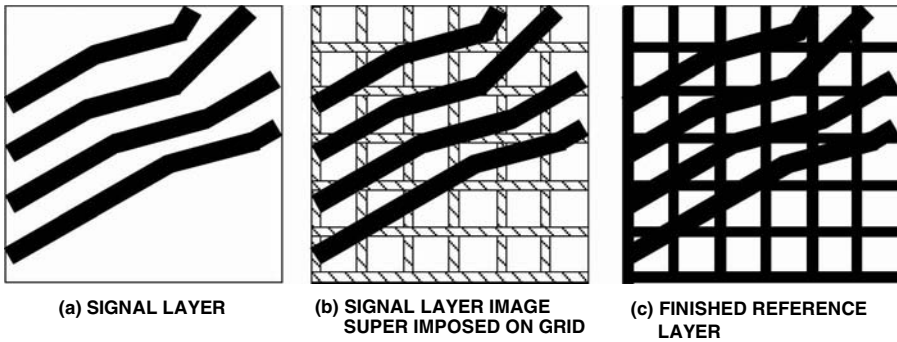
FIGURE 2.3
(a) An example of a set of signal lines in a ceramic substrate. (b) The signal lines superimposed onto a mesh ground plane. (c) The final combination of the improved mesh ground plane.

2.2.3.2 Dielectric Thickness

LTCC tapes are offered in multiple thicknesses. In one LTCC material system, fired thicknesses of 1.7, 3.8, 5.5, and 8.5 mil are available. Combinations of any of these thicknesses may be used in a structure; however, it is recommended that a symmetrical stackup be used to minimize potential process or mechanical problems such as warp and bow.

Table 2.4 tabulates some variations of overall thicknesses that can be configured with the previously stated four increments of tape thicknesses. This gradation of overall thickness coupled with line width variation results in the ability to meet a wide variety of impedance values.

2.2.4 Propagation delay

Propagation delay is the time between the input and output of a signal expressed in nanoseconds per foot (nsec/ft) or picoseconds per inch (psec/in.), of conductor length [9]. Transmission line signal propagation delay, or "tpd," is a function of the effective dielectric constant of the material in the signal path. The propagation delay will vary with the circuit configuration and the dielectric material. For the microstrip configuration, the delay equation is:

$$\text{tpd} = 1.017\sqrt{0.475\,\varepsilon_r + 0.67}\ \text{ns/ft.}$$

For stripline, the equation is:

$$\text{tpd} = 1.017\sqrt{\varepsilon_r}\ \text{ns/ft.}$$

TABLE 2.4

LTCC Substrate Thickness vs. Layer Count

Overall Fired Thickness (mil)	Number of Layers			
	1.7-mil Tape	3.8-mil Tape	5.5-mil Tape	8.5-mil Tape
1.7	1	—	—	—
3.4	2	—	—	—
3.8	—	1	—	—
5.1	3	—	—	—
5.5	1	1	—	—
5.5	—	—	1	—
6.8	4	—	—	—
7.2	1	—	1	—
7.6	—	2	—	—
8.5	5	—	—	—
8.5	—	—	—	1
9.3	1	2	—	—
9.3	—	1	1	—
10.2	6	—	—	—
11	—	—	2	—
11.4	—	3	—	—
11.9	7	—	—	—
12.3	—	1	—	1
13.6	8	—	—	—
14	—	—	1	1
15.2	—	4	—	—
15.3	9	—	—	—
16.5	—	—	3	—
17	—	—	—	2
17	10	—	—	—
19	—	5	—	—
22	—	—	4	—
22.8	—	6	—	—
25.5	—	—	—	3
26.6	—	7	—	—
Minimum Via (mil)	2.5	4	6	10

Figure 2.4a shows the difference in propagation delay between the microstrip and stripline configurations for a nominal LTCC dielectric constant of 7.8 vs. conductor length. A typical tolerance of dielectric constant is ±0.1. Figure 2.4b shows the minimal variation in propagation delay with this variation. Stripline delay is a function of material dielectric constant, whereas the microstrip delay is a function of the material dielectric constant and air, resulting in a lower effective dielectric constant and greater speed. Other configurations also exhibit minimal variation in delay.
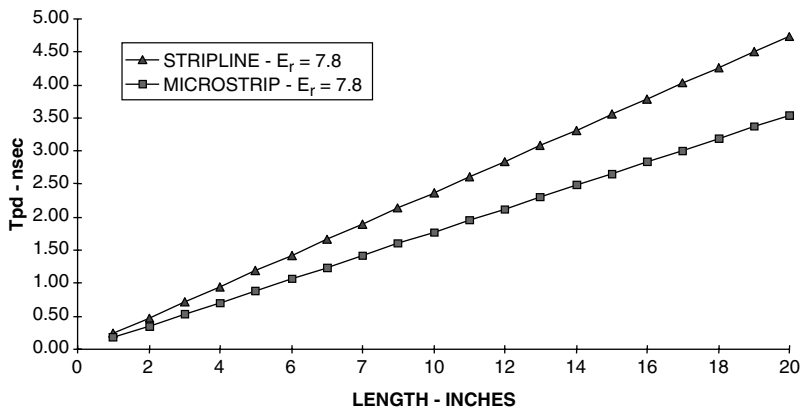
FIGURE 2.4A
Propagation delay vs. configuration.
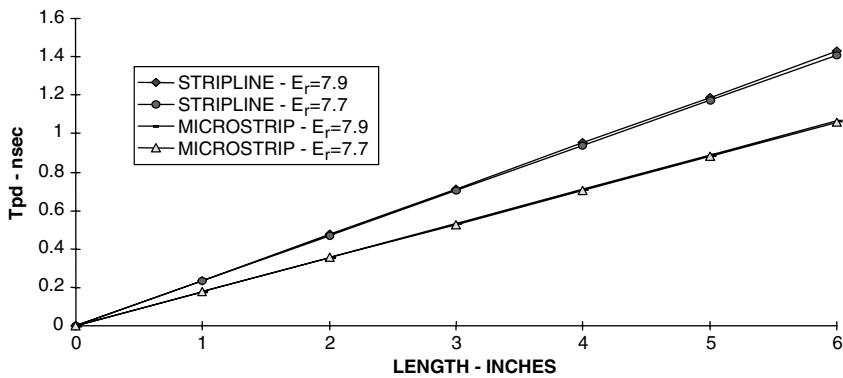
FIGURE 2.4B
Propagation delay, E_r = 7.7 to 7.9.

2.3 Electrical Design Considerations

2.3.1 Controlled Impedance Lines

2.3.1.1 Microstrip

The microstrip transmission line configuration is defined as a signal conductor opposite a parallel reference plane separated by a dielectric. A microstrip cross section is shown in Figure 2.5. The equation defining the impedance of this configuration is:
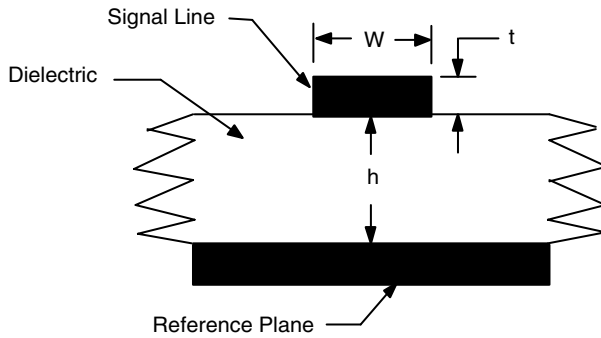
FIGURE 2.5
A cross section of a microstrip transmission line.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \, \mathrm{Ln}\left(\frac{5.98h}{0.8w + t} \right)$$

where
  h = dielectric thickness
  w = conductor width
  t = conductor thickness
  ε_r = effective dielectric constant [10]

This configuration is used in RF and microwave circuitry, and is typical of external layers in a multilayer structure.

2.3.1.1.1 Embedded or Coated Microstrip

In the microstrip configuration, the signal conductor is surrounded by air (except on the dielectric surface). If the conductor is coated by another dielectric, such as a glaze or encapsulant, it is referred to as *embedded* or *coated microstrip*. If the dielectric constant of the coating is close to that of the supporting dielectric, the impedance of the line will be lowered by 10–20%, and the signal propagation delay will be increased by about 20%.

In an LTCC structure, the reference plane conductor may be printed on the opposite side of the tape dielectric upon which the signal conductor is printed, or it may be printed on the tape layer beneath the signal conductor tape layer. The end result in the fired structure will be the same. From a manufacturing perspective, printing on only one surface of a tape layer is preferred.

2.3.1.2 Stripline

The stripline transmission line configuration is defined as a signal conductor surrounded by dielectric material between two reference planes. It may also
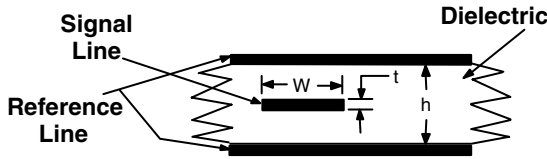
FIGURE 2.6
A cross section of a stripline transmission line.

be referred to as *balanced stripline* when the signal conductor is located equidistant from the reference planes. A stripline cross section is shown in Figure 2.6. The equation defining the impedance of this configuration is:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \, \text{Ln}\left(\frac{4h}{0.7\pi \, W \left(0.8 + \frac{t}{w}\right)} \right)$$

where
h = dielectric thickness
w = conductor width
t = conductor thickness
ε_r = material dielectric constant [10]

As described in Section 2.3.1.1, the microstrip configuration is an inherently faster interconnection (shorter propagation delay), as in a microstrip, the signal conductors are on an external surface exposed to air, resulting in a lower effective dielectric constant. However, there is only limited external area on a substrate and microstrip structures require more surface area. This could be a problem, particularly in digital applications with a large number of interconnects; so other configurations are typically used. The stripline construction with its multiple reference planes is well suited for multilayer interconnection. The two reference planes and homogeneous dielectric offer the benefits of dielectric uniformity and electrical isolation, but capacitive loading on the signal line is increased, increasing propagation delay over that of a comparable microstrip line. Also, a thicker dielectric is needed with stripline interconnections for the same impedance such that overall substrate thickness is increased. However, for multiple layers, impedance reference planes may be shared (noise or interaction in sensitive signal lines as a result of ground noise or coupling through the common plane is not of concern). Shared reference planes in stripline would use five conductor layers for two signal layers, seven conductor layers for three signal layers, etc. A top pad or component attachment layer would result in a total of six conductor layers for a two signal layer structure; eight conductor layers for a three signal layer structure, etc., for pure stripline construction.
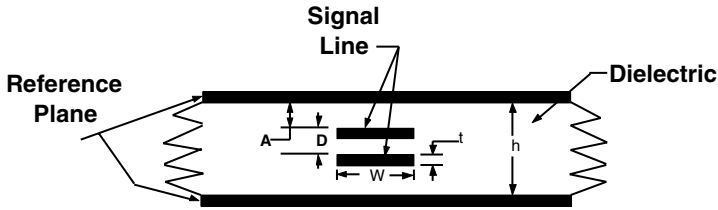
FIGURE 2.7
A cross section of a dual stripline transmission line.

2.3.1.2.1 Dual Stripline

The dual stripline transmission line configuration is defined as two signal conductors surrounded by dielectric between two reference planes. The signal conductors are predominately routed orthogonally on an "x" layer and a "y" layer to minimize z-axis coupling, and are symmetrically located between the reference planes. A cross section of a dual stripline configuration is shown in Figure 2.7. The equation defining the impedance of this configuration is:

$$Z_0 = \frac{2 F_1 F_2}{F_1 + F_2}$$

$$F_1 = \frac{60}{\sqrt{\varepsilon_r}} \, \text{Ln} \left(\frac{8A}{0.67\pi \, W \left(0.8 + \frac{t}{w}\right)} \right)$$

$$F_2 = \frac{60}{\sqrt{\varepsilon_r}} \, \text{Ln} \left(\frac{8(A+D)}{0.67\pi \, W \left(0.8 + \frac{t}{w}\right)} \right)$$

where
  h = dielectric thickness
  w = conductor width
  t = conductor thickness
  ε_r = material dielectric constant
  A = signal line to reference plane spacing
  D = signal line spacing [10]

This configuration is commonly used in digital applications. A single signal layer, four conductor layer stripline construction is shown in Figure 2.8. If multiple signal layers are needed (and shared reference planes are electrically acceptable), the dual-stripline configuration is more effective. With shared reference planes, a dual-stripline construction would use eight conductor layers for four signal layers (two signal layer pairs). Similarly, ten conductor layers would be needed for six signal layers, etc. (Note that in
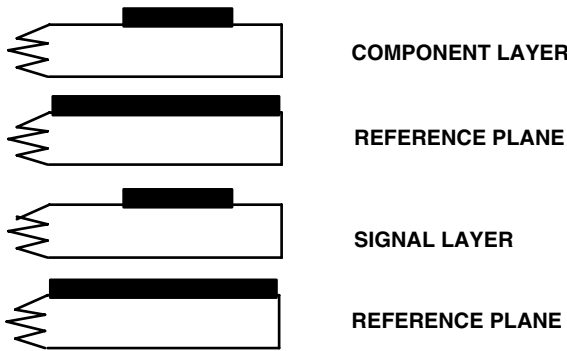
FIGURE 2.8
Basic stripline construction.

these examples, in addition to the signal and reference plane layers, an additional layer is used for component attachment and surface interconnection.) A four-signal-layer dual-stripline construction with shared reference planes is shown in Figure 2.9 whereas Figure 2.10 compares two signal layer constructions using stripline, stripline with shared reference planes, and dual stripline, demonstrating the reduced number of layers if shared planes are used.

2.3.1.3 Coplanar Waveguide

In many high-frequency applications, coplanar waveguide (CPW) has emerged as an alternative topology to traditional microstrip in ceramic circuits, utilizing microwave integrated circuits (MICs) and monolithic microwave integrated circuits (MMICs).

CPW implementations offer design advantages of nearly constant effective dielectric constant values for a wide range of characteristic impedance values, and low-substrate thickness dependence on impedance. CPW impedance is a function of the signal and ground conductor widths, spacing of the ground conductors from the signal conductor, and the width of the ground conductors as depicted in Figure 2.11. The analytical expressions for this configuration are more complex and beyond the scope of this section [11–13]. A sample geometry for a 50-Ohm finite ground CPW interconnect, established using a field solver, could use the following parameters: a gap of 3 mil, line width of 8.3 mil, and a ground width of 15 mil for an LTCC dielectric with a dielectric constant of 7.4, and a dielectric thickness of 23 mil.

2.3.1.4 Differential Interconnections

Differential signaling is becoming more popular as the circuit speed increases and integrated circuit (IC) voltages become lower. Differential transmission minimizes the effect of common mode noise; however, each signal path
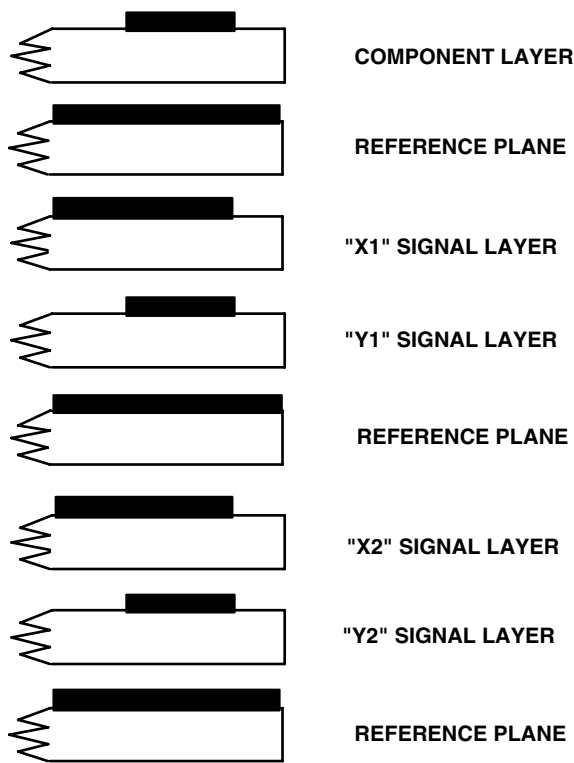
FIGURE 2.9
Four signal layer dual stripline construction with shared reference plane.
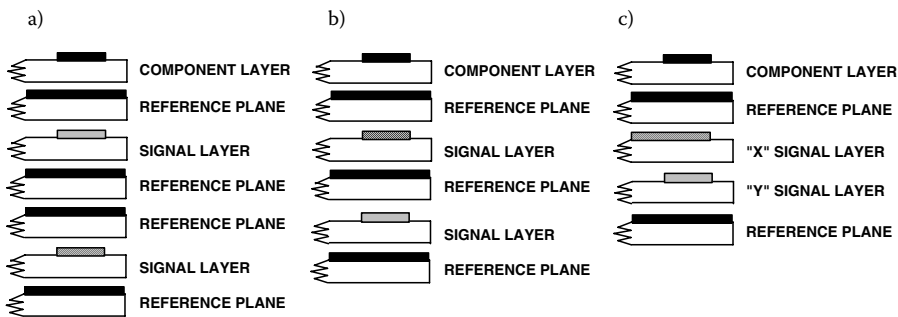
FIGURE 2.10
(a) Two signal layer stripline construction. (b) Two signal layer stripline construction with shared reference plane. (c) Two signal layer dual stripline construction.
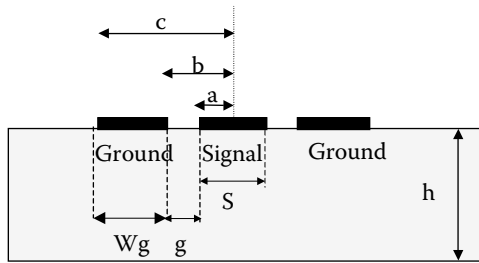
FIGURE 2.11
A cross section of a coplanar transmission line.

requires two conductors instead of one, resulting in lower-density interconnections. LTCC offers an advantage for this class of interconnections in that it is practical and cost-effective to have a large number of layers in a structure such that x–y density is not sacrificed. Useful analytical equations for edge-coupled differential pairs in the microstrip or stripline configuration are found in the literature [14]. The impedance of the individual conductor must be calculated first; then the differential impedance is computed based on the conductor spacing and the dielectric thickness. For these equations, both conductors in the differential pair must have the same cross-sectional dimensions. The relationships were determined empirically, and the practical ranges of impedance are 20–150 Ohms with an accuracy of up to ±10%.

For microstrip, the differential impedance is:

$$Z_{\text{diff}} \cong 2Z_0 \left(1 - 0.48 e^{-0.96\frac{s}{h}} \right) \text{Ohms}$$

and for stripline, the differential impedance is:

$$Z_{\text{diff}} \cong 2Z_0 \left(1 - 0.374 e^{-2.9\frac{s}{h}} \right) \text{Ohms}.$$

2.3.2 The Choice of Impedance

The choice of interconnection impedance involves many complex system design trade-offs and is driven by the semiconductor circuit requirements. Circuit rise time, propagation delay, and noise immunity are the primary parameters that must be balanced within the system along with noise budget, operating-performance requirements, power limitations, and physical/process capabilities and, of course, minimizing cost in the selection of the system impedance level. An excellent description of the choice of system impedance can be found in [15]. Impedance values in the range of 50–100 Ohms are

typical with, 50, 75, 80, and 100 Ω being most prevalent in both digital and
analog applications.

   As previously discussed, the primary variables that influence impedance
are the substrate material dielectric constant, signal-conductor thickness,
signal-conductor width, and the dielectric thickness surrounding or separat-
ing the signal conductor from the return or reference planes. There are other
"knobs to turn," and other physical elements influence impedance, which is
a function of specific designs. Proximity to other features or components,
the number and placement of vias, adjacent conductors, meshed or gridded
power planes, etc., can all affect circuit impedance. It is not practical in an
overview chapter such as this to address these effects. The literature should
be consulted for further information [10–15]. The dielectric constant is an
inherent material property and is essentially fixed (within a tolerance range)
for design. Important factors are the uniformity of dielectric constant over
a broad frequency range for analog and digital applications and close toler-
ance control. A change in dielectric constant causes a significant change in
impedance. LTCC materials have excellent uniformity of dielectric constant
over a broad frequency range, resulting in improved signal integrity or the
ability to relax specifications on other parameters to achieve improved yield
and to reduce cost.

2.3.3   Guide Wavelength

High-frequency RF designs can use the higher dielectric constant of ceramic
materials to reduce the feature size of resonant or wavelength-dependent
features, as signal wavelength is an inverse function of the square root of
the dielectric constant. Guide wavelength is defined as:

$$\lambda_g = c / \left(f \times \sqrt{\varepsilon_r} \right)$$

where
   λ_g = guide wavelength (meters)
   f = frequency (hertz)
   c = speed of light (meters/second)
   ε_r = dielectric constant [2]

   Guide wavelength may also be used to compare different material systems
with different feature sizes, to plot attenuation vs. guide wavelength. This
is shown in Figure 2.12, based on measured data comparing the 50- micros-
trip attenuation of various material systems. Comparing materials with vari-
ations in dielectric constant using 50-Ohm microstrip transmission lines on
constant thickness substrates requires different conductor widths. These
width differences result in differences in conductor attenuation, making
direct comparison unrealistic. Using guide wavelength, in effect, normalizes
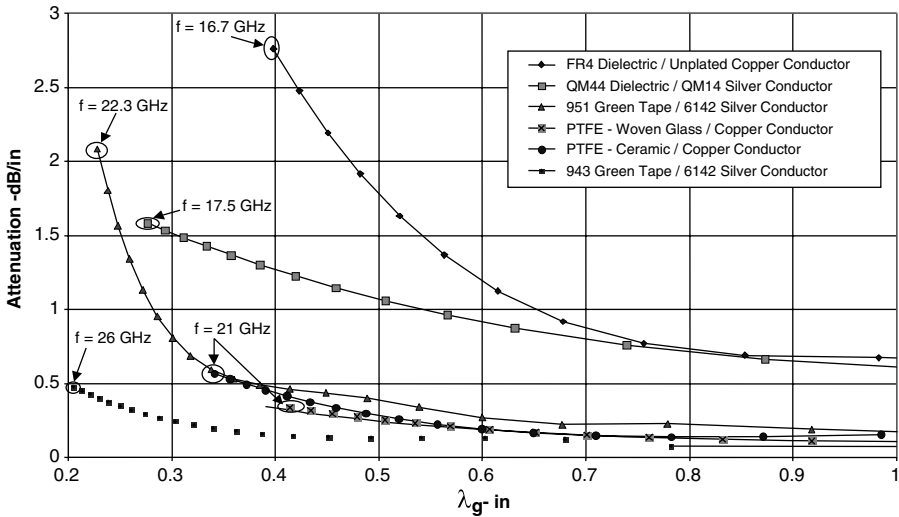
FIGURE 2.12

Attenuation vs. guide wavelength for several different material systems with different feature sizes.

the data for the dielectric constant and conductor width differences. It can be seen from these comparisons that the low-loss LTCC system has attenuation comparable to, or lower than, the organic-based material systems used in many high-frequency applications [2,16].

2.3.4 Embedded Passives

2.3.4.1 *Integral, Buried, Embedded Components*

There is a wealth of information in the literature describing the benefits of embedded or buried passive components. Embedded components provide high density by allowing passive components to be located beneath the active devices mounted on the surface of an interconnecting substrate, higher reliability through the reduction of solder joints, and higher performance through the reduction of both interconnection and power system impedance.

Ceramic technology has offered integral components (resistors and capacitors) in thick-film hybrid circuitry for over 30 years [1]. Capacitors have been implemented in multilayer hybrid circuits using high dielectric constant (high-K) pastes, and surface resistors have been implemented with pastes having resistivities from 100 to 100,000 Ohms/□ [17]. These surface resistors can be trimmed to precision values. A significant advantage of LTCC ceramic technology is the ability to fully embed resistors, capacitors, and inductors in the inner layers of multilayer structures, resulting in high-density packaging and enabling functions not currently achievable with organic technology.
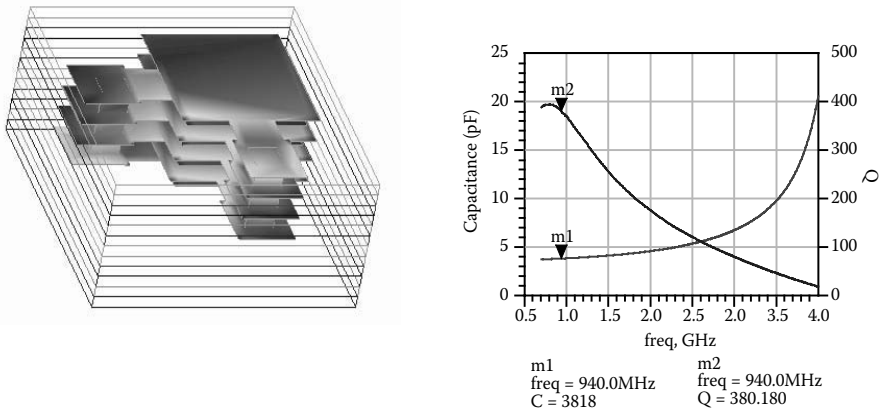
FIGURE 2.13

(left) A 3D model of multilayer integrated capacitor, along with the electrical performance of this device as a function of frequency (right).

2.3.4.2   *Capacitors*

In LTCC technology, capacitors and resistors can be buried (embedded) in a multilayer structure resulting in high density (more functions per unit area or a smaller size for the same function), improved electrical performance (shorter interconnection paths to active devices and reduced parasitics), and improved reliability over surface mount technology (SMT) components (reduction of solder joint interconnections). Capacitors in LTCC can be constructed using high-K tapes or pastes. Thin LTCC dielectric tapes with K = 20–100 and thick-film cofireable pastes with dielectric constants up to 2000 have been developed. These materials are suitable for decoupling, filtering, and DC blocking applications. Typical worst-case tolerances for buried capacitors are 7 to 10%. Figure 2.13 depicts a multilayer embedded capacitor designed for LTCC. This component was designed for a 2.4-GHz application using 1.7 mil thick LTCC with a dielectric constant of 7.8 [2].

2.3.4.3   *Resistors*

Cofiring and burying resistors in LTCC results in the same functional and performance advantages as buried capacitors. The values of screen-printed, untrimmed buried resistors can range from ±20 to 30% of nominal values, which is suitable for many applications. Some foundries specify a tolerance as tight as ±10%. If tighter resistor tolerances are needed, openings may be left in layers above the resistor to permit trimming. Of course, this obviates some of the density advantage, but burying may still offer the performance and reliability improvements of embedded components. The resistor size, termination metallurgy, number of refirings, and location of the resistor in the stackup will affect the resistance value. For example, using the same

50
45
40
35
30
25
20
15
10
5
0

Inductance (nH)

100
90
80
70
60
50 Q
40
30
20
10
0

m6

0.5   1.0   1.5   1.8
freq, GHz

m6
freq = 940.0MHz
L1 = 15.729

m7
freq = 940.0MHz
Q3 = 30.689
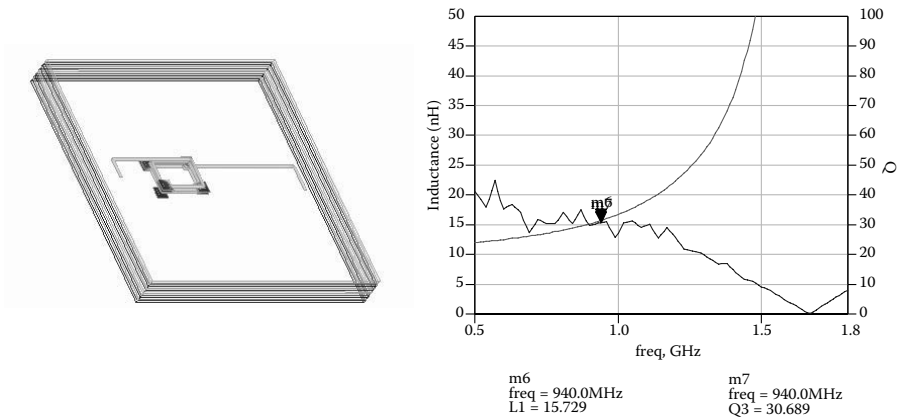
FIGURE 2.14

(left) A 3D model of a multilayer integrated inductor, along with the electrical performance of this device as a function of frequency (right).

paste value on different layers in a multilayer structure may produce different resistor values owing to location of the resistor with respect to the furnace belt, where poorer airflow exists. As with other materials and functions, there are process effects and geometry considerations in the application of buried resistor pastes that require close interactions with foundries [18–22].

Surface, postfired resistors that can be laser-trimmed can be used with LTCC, where tighter tolerances for precision analog applications and ratio-matched differential networks are used.

2.3.4.4 Inductors

Inductors can be implemented and buried in multilayer ceramic structures in single conductor or single layer or multilayer spiral configurations using well-known relationships [2]. Ferrite pastes are available to concentrate magnetic fields, thereby enhancing inductor performance. High-conductivity conductor materials are available that will improve inductor Qs. Figure 2.14 depicts a multilayer embedded inductor designed for LTCC. This component was designed for a 2.4-GHz application using a photo-patterned silver conductor.

2.3.5 Substrate Size

It has not been unusual for LTCC substrate manufacturers to be presented with designs in which the overall part size cannot be changed. The cost of LTCC multilayer circuits is very dependent on overall part dimensions and the relationship to the foundry panel size, panel tooling, and the usable area within the panel. It is important to maximize the total number of parts within the usable area to achieve the lowest possible unit cost. A small dimensional increase could eliminate a row or column of parts or produce excess waste

with a corresponding cost per part increase. The various elements affecting overall part size should be reviewed with potential foundries and a trade-off analysis of the tooling/process/design options performed. Factors that impact the final part size are overall sheet size, tooling border, edge-to-circuit clearance, shrinkage, shrinkage tolerance, registration tolerance, and saw or laser kerf, or hot knife width. These factors determine usable circuit area and the final individual part size. Of the many elements influencing the overall cost of a part, the optimization of the parameters impacting the overall part size to achieve the most parts per panel will have the most significant effect on cost

2.4   Electrical and Thermal Design Considerations

2.4.1   Electrical Design Tools

The ability to integrate passive components between LTCC layers enables a significant reduction in circuit size, weight, and cost. Over the past decade, LTCC has been used in multiple generations of RF and multichip modules. These applications have demonstrated the size, weight, and cost savings that can be realized by using LTCC. Much of the development of these modules was accomplished by trial and error: work-around methods and the use of proprietary design tools. The design flow resulted in multiple design–build–test iterations. There was not a strong push for development of a design infrastructure for LTCC circuits.

The 2002 National Electronics Manufacturing Initiative (NEMI) roadmap cited design infrastructure — education, tools, and standard practices — as a major gap that hinders broad adoption of LTCC in volume applications. Without this necessary design infrastructure, the design cycle relies on multiple design–build–test iterations, a highly inefficient process.

The need to improve design infrastructure of LTCC has been recognized by the industry, and major design tool suppliers now include LTCC in their suite of materials and have tailored products for LTCC design. However, even though there has been much progress in recent years, many designers are still unfamiliar with the technology.

Design libraries that reduce design cycles to days instead of weeks, with the goal of producing a prototype that meets specifications on the first prototype build, are emerging. Figure 2.15 illustrates a typical design flow for multilayer circuits with embedded passive components. This simplified diagram highlights some of the tasks or details a designer must consider at each step [23]. Perhaps the most challenging element is the need to perform EM simulation. This requires some of the most powerful commercially available computer hardware and software. EM simulation is necessary because functions are

Front End Design Decisions

Substrate Materials
Interconnect Materials
Test Requirements
Size/Weight Envelope
System Interface Issues
Lumped or Distributed?
Cost (price point)

Plan the Design

Research Available IP
Inventory Design Tool Needs
Determine Design Approach
Draft Initial Schematic
Draft Initial Layout
Initial Design Review

Develop Detailed Design

Reuse "Building Block" Models
Develop New Models
EM Simulate New Models
Optimize New and Reused Models
Cascade Models Together
EM Simulate Full Circuit
Optimize Full Circuit

YES   NO

Successful Prototype

Cataloh New Verified Models
Add to "Building Block" Library

Does it Meet Spec? (Test Verification)

Test Methods and Equipment
Reliability Testing
Functional Testing

LTCC Manufacture & Assembly

Fabricat In-House or Send Out?
Test Fixtures?
Resistor Trimming
Post-Processing or Rework

FIGURE 2.15

A typical design cycle for multilayer circuits with embedded passives.

complex, and coupling between closely integrated embedded passive components cannot be easily predicted, especially at high frequencies.

Designers are becoming more familiar with substrate and interconnect materials, and many software tools now have LTCC data libraries. As applications increase, materials data and models, or templates for verification, or electronic design automation (EDA) design reuse are becoming available. Basic geometries and structures that will be common to many different circuits are also becoming available. As frequencies increase, these structures become more dependent on the material properties and the application. Most design organizations maintain libraries of component models or "building blocks." These models are generally valid over a range of frequencies, so a building block developed for one application can be used for another circuit. Where appropriate, fabricators and materials suppliers can provide expertise, and also serve as repositories for these models to assist designers in getting the most out of LTCC materials.

To make the LTCC design process more efficient for designers, one organization took the step of developing a library of passive circuit components [16]. This library is formatted as a "design kit" for use with a widely used EDA design platform currently used for RF and microwave designs [32]. The library was developed for a low-loss LTCC materials system, which lent itself to emerging high-frequency applications owing to its low loss tangent at high frequencies ($\tan \delta = 0.002$ at 40 GHz). Components included in the design kit include inductors, capacitors, couplers, filters, resonators, transmission lines, transitions, and a balun. Details on these components are summarized in Table 2.5.

In this library, each component design is based on a simulated model developed using commercially available electromagnetic simulation tools. Mechanical layouts were generated based on these models, and parts were manufactured. S-parameter files included in the design kit reflect verified

TABLE 2.5

A Summary of Simulated Components Included in a Commercially Available LTCC Design Kit

Component Type	Palette Symbol(s)	Number of Elements	Verified? (Yes/No)	Frequency Range (GHz)	Notes
Microstrip Capacitors with lumped element values		5	Yes	20 – 40	0.2 pF – 1 pF
Microstrip Capacitors for broadband coupling		5	Yes	20 – 40	Interdigital (3) Gap (2)
Microstrip Inductors with lumped element values		6	Yes	20 – 38	0.2 nH – 1.2 nH
Microstrip Inductors chokes		3	Yes	22 – 40	Circular Spiral (1) Rectangular Spiral (2)
CPWG Transmission Lines		6	Yes	20 – 35	Six Different Lengths
CPWG to Microstrip to CPWG Transmission Lines		4	Yes	20 – 36	Four Different Lengths
CPWG to Stripline to CPWG Transmission Line		1	Yes	20 – 39	$L_{stripline} \approx 2(L_{CPWG})$
Transition Model		1	No	20 – 39	CPWG to Stripline
CPWG Discontinuities		5	Yes	20 – 38	Open End Effects (2) Center Cond. Gaps (2) Microstrip Open Circuited Stub (1)
Stripline Coupler Models		4	No	20 – 40	Branch (3 dB), Ring (3 dB), Offset (19 dB), Edge (20 dB)
Verified Stripline Coupler		1	Yes	21 – 26	Offset Design (12 dB)
Stripline Filter Models		2	No	20 – 55	Highpass (34 GHz cutoff) Lowpass (43 GHz cutoff)
Stripline Bandpass Filter		1	Yes	20 – 40	f_c = 33.75 GHz, BW = 770 MHz
Stripline Resonators		2	Yes	20 – 40	End Coupled (f_r = 30.5 GHz) Tee (f_r = 34.9 GHz)
50 Ohm Balun Model		1	No	29 – 37	Open Circuit Marchand Design

test data from the manufactured parts. These models reflect specific, measured components in a specific layer stackup. Also, for the most part they include ground–signal–ground (GSG) probe pads as part of the model; that is, most components are not de-embedded, but include probe pad ports as part of the component. These library elements have fixed values and feature sizes; that is, component scaling or parameterization was not incorporated. However, this design kit provides a starting point for application of LTCC.

An approach to successfully designing complex multilayer LTCC modules is not easily defined. It requires some of the elements from both semiconductor circuit and printed wiring board designs. Generally, in semiconductor design, processes become highly standardized based on the minimum feature size attainable by a given process. This results in well-developed process design kits that closely integrate complex EDA design tools and fabrication processes. In the design of many printed wiring boards, complex EM simulations are generally not needed. Most designs can be done using 50-Ohm calculations of printed structures. Design of complex LTCC multilayer circuits requires designers to be flexible in their choice of structures, similar to a printed wiring board (PWB) designer, but must take into account high levels of complexity, similar to a semiconductor designer.

A design infrastructure must provide flexibility in the choice of materials and structures. For instance, circuit models based on fixed features or stackups will not be as useful to designers as models that allow a designer to choose different variable parameters. Another major point to keep in mind is that different software tools are typically used to realize a successful design. One software tool can rarely effectively simulate and analyze both the individual building blocks and the total circuit. Finally, any design infrastructure must involve materials and fabrication experts to support design expertise.

2.4.2 Thermal Performance

Thermal performance has always been a significant factor in the choice of materials for electronic packaging; however, new demands are being placed on packages and interconnecting substrates. In wireless communication applications, the stability and uniformity of electrical properties over broad frequency and operating temperature ranges are critical. Until the advent of wireless communications, there were few high-volume applications of ceramic materials; ceramic was primarily used for its proven high reliability, high density, semiconductor process compatibility, environmental performance (hermeticity), and thermal properties. High-volume wireless module designs, such as Bluetooth, have been implemented in LTCC for the excellent combination of properties offered by LTCC, and the overall cost has been shown to be lower than FR4 PWB equivalents.

Similar performance requirements are arising in high-speed digital systems to maintain signal integrity. With clock rates exceeding 1 GHz, material

property stability and uniformity in the 7–10 GHz range, and higher thermal conductivity due to a significant increase in power dissipation of packages and modules is also needed. In wireless, digital, and photonic applications, these materials properties are required, along with higher component and increased interconnection densities. Ceramic materials are able to meet these increasingly stringent thermal requirements. Design techniques are available to provide thermal enhancement to thick film and packages and interconnecting substrates, in the form of integral heat spreaders and directly attached heat sinks, using brazing technology and thermal via configurations [24].

2.4.2.1 LTCC

Thermal vias have been used to improve thermal conductivity of packages and modules, as well as to provide a design approach to balancing junction temperatures in multichip modules [25,26]. Testing has shown the thermal conductivity of new low-loss LTCC materials to be 20 times that of printed wiring materials [27].

In Reference 27, test results for the thru-plane thermal conductivity for unmetallized FR4, PTFE–Ceramic, and 951 and 943 Green Tape™ with double-sided metallization were described. It was shown that the LTCC materials have a thermal conductivity of about 1/5th that of alumina but about 20 times that of the FR4 and ceramic-filled PTFE materials (Figure 2.16.) There was little improvement in thru-plane thermal conductivity with added metallization. Measurement of in-plane thermal conductivity was not
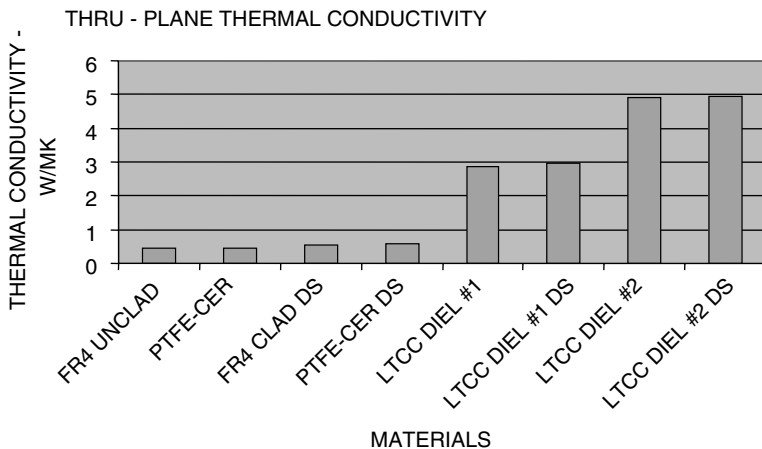
FIGURE 2.16
Thermal conductivity of several LTCC and polymer materials.

performed, as it required a different fixture and different test sample dimensions. An in-plane fixture was obtained, LTCC test samples redefined with solid and gridded metallization, and via variations and testing of the in-plane and thru-plane thermal conductivities were performed.

As expected, the highest thru-plane thermal conductivity was obtained in the samples with the greatest number of thermal vias. The addition of gridded and solid planes did not significantly improve the lower via density thru-plane conductivities, but the presence of metal planes significantly improved the higher via density thru-plane conductivities. In the configurations without vias, the solid or gridded planes offered little improvement in thru-plane conductivities. For the lower-density vias, a solid plane offered no improvement in thru-plane thermal conductivity over the gridded plane.

Little improvement was seen in the in-plane thermal conductivity when a solid plane was used instead of a gridded plane. The addition of an internal gridded plane improved the in-plane thermal conductivity by about 20%. Gridded planes connecting thru thermal vias improve the in-plane thermal conductivity by about twice that of the configurations without metal planes.

2.4.2.2 Thermal Coefficient of Expansion

Ceramic technology has thermal coefficients of expansion (TCEs) well matched to silicon, gallium arsenide, and indium phosphide semiconductor technologies for reliable direct attachment of large die. Figure 2.17 charts the TCEs of popular substrate and semiconductor materials. LTCC is being used for ball grid array (BGA) modules for direct attachment to PWBs [28]. LTCC
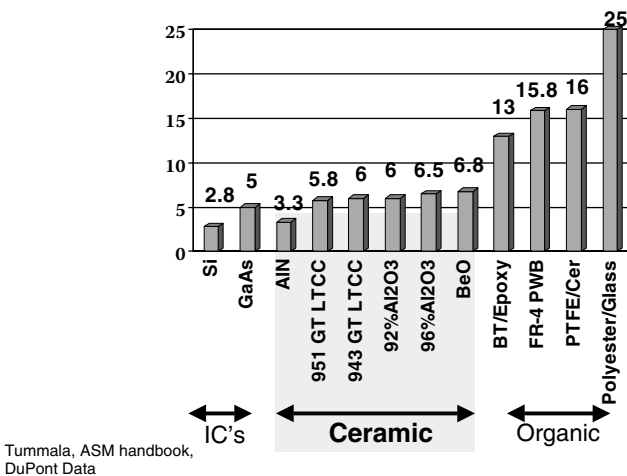
FIGURE 2.17
CTE of selected materials.

material is also available with a TCE of 12, a value midway between the semiconductor and PWB materials to minimize the stress on attachment materials.

2.4.2.3   AlN Thick-Film Technology

In thick-film technology, new materials and unique process techniques have been developed to fill thermal vias in alumina ceramic substrates, as a lower-cost alternative to high-thermal-conductivity ceramics [26]. Also, new materials are now available that expand the use of aluminum nitride (AlN) thick-film ceramic for high-power-dissipation applications.

Thick-film materials for AlN substrates have been in use for over a decade. Earlier, considerable effort was made on treating the surface of AlN to make it more bondable to thick-film materials. Recently, more attention has concentrated on making conductor materials more compatible with AlN substrates and overcoming difficulties with conventional thick-film materials that work well on alumina substrates but either blister or adhere poorly to AlN substrates. This development was also driven by environmental concern for the use of high-thermal-conductivity beryllium oxide (BeO) ceramic, where many manufacturers felt compelled to switch to alternative substrates. Typical data for popular substrates used in high-dissipation applications are tabulated in Table 2.6.

Conductors exhibit performance at the same level as on alumina substrates. Test results demonstrated that none of the conductors showed any particular sensitivity to substrates from four sources. This is important as the substrate variability and conductor incompatibility experienced in the past have been remedied.

In addition to the conductors, compatible crossover dielectric, resistor series, and brazing materials are available. The dielectric composition matches the TCE of AlN substrates, and resistance values of resistors range from 100 mΩ to 1 KΩ/sq. Typical properties of the resistors include TCR

TABLE 2.6

Properties of Common High-Thermal-Conductivity Substrates

Property	AlN	BeO	Al$_2$O$_3$
Dielectric constant	8.9	6.7	9.8
Dielectric loss	0.0001	0.0003	0.0002
Resistivity (Ω·cm)	>10^{14}	>10^{14}	>10^{14}
Thermal conductivity (W/m·K)	170–200	260	36
CTE (ppm/°C)	4.6	8.5	8.2
Density (g/cm^3)	3.3	3.85	2.89
Bending strength (MPa)	290	230	380
Hardness (GPa)	11.8	9.8	14.1
Young's modulus (GPa)	331	345	372

TABLE 2.7

Thick-Film Materials for Aluminum Nitride (AlN) Resistors

Thick-Film Materials for AlN Resistors						
Product	AN592	AN599	AN610	AN615	AN620	AN630
Chemistry	Pd/Ag	Pd/Ag	RuO_2	RuO_2	RuO_2	RuO_2
Resistance	200 mΩ	1 Ω	10 Ω	50 Ω	100 Ω	1 KΩ
TCR (ppm/°C)	+300 – +400	±100	±150	±150	±150	±150

AlN Conductors and Dielectrics						
Product	AIN44	AIN11	AIN21	AIN23	AIN33	AIN71
Chemistry	Diel	Ag	Ag/Pt 100:1	Ag/Pt 3:1	Ag/Pd 10:1	Au
Solderable						
62/36/2	N/A	X	X	X	X	N/A
10/88/2	N/A	X	X	X	X	N/A
Platable	N/A	X	X	NT	X	N/A
Brazable	N/A	X	X	NT	X	No
Wire-Bondable						
Au	N/A	X	X	N/A	NT	X
Al	N/A	NR	NR	NR	NT	X

(±150 ppm), low noise, blendability, refiring, and trimming stability. Table 2.7 summarizes the properties of this material system.

Ceramic technology has excellent thermal performance and offers a combination of properties satisfying the many complex trade-offs of high-performance packaging with a demonstrated capability to do so cost-effectively.

2.5   Testing and Characterization

2.5.1   Material Characterization

Electrical testing and the characterization of materials is required in parallel with material development. Complete property data is needed for design and simulation to proceed, and for product specification as well. Data and complete application information are also expected to be available with the initial release of a new materials system. This can be very challenging, particularly for materials suppliers who are expected to provide electrical property data over a wide range of frequencies, temperatures, and humidities for all combinations of the material's processing conditions. This requires extensive testing. The days of the fully integrated company manufacturing ceramic circuits are over, except for some advanced military organizations, and even they use outside services. This has placed more demands on the
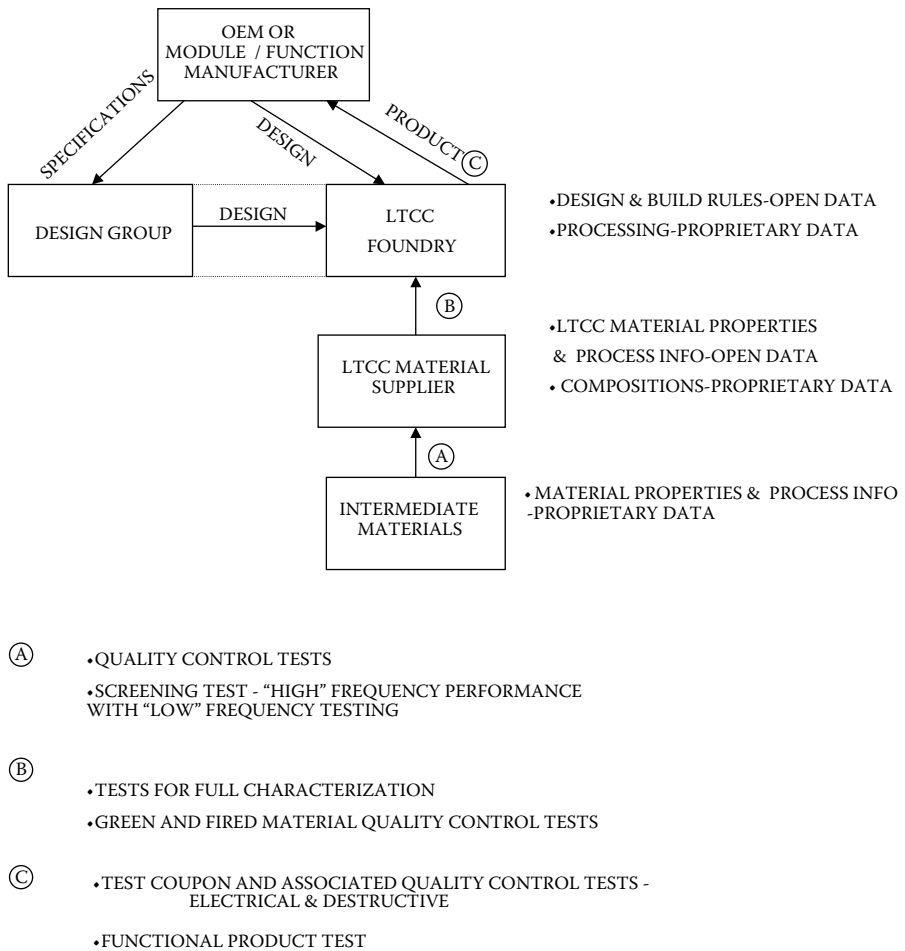
FIGURE 2.18
A typical supply chain.

supplier base for process and end-use characterization data. Ceramic technology employs the same basic test requirements used in other interconnection technologies; however, there are some unique considerations and practices owing to the nature of the technology and the supply chain.

Figure 2.18 depicts a supply chain typical of merchant market LTCC products. Testing at each of these levels has different requirements.

The supplier of intermediate chemical materials must provide basic chemical property data. Manufacturing process data are often proprietary, and correlation of materials properties to performance at the higher levels is typically not known. Also, owing to volume usage and economics, only single grades of material may be available where an electronic-grade material will require additional processing and higher cost. Therefore, testing at this

level is usually limited to basic specifications for quality control purposes. More comprehensive screening tests may be performed at the next level of manufacture.

At the next level, intermediate materials are further processed and developed into "engineered materials" or materials systems. These developments are extensive, lengthy, and complex to ensure conformance with specifications and market needs, and to ensure the compatibility of the broad range of materials in a typical ceramic system (dielectrics, conductors, via fill, resistors, encapsulants, etc.). Another difficult task at this level is the need to ensure compatibility and performance with the assembly processes that are performed at the next or higher levels in the supply chain, processes that are often different at each foundry or end user and can significantly impact material properties and performance. Complete electrical, mechanical, and environmental characterization is required at this level. In addition, quality control testing is performed at this level on both the green or unfired materials supplied to the customer, as well as the testing of processed materials from each lot to ensure conformance with specifications.

At the foundry level, quality control tests may be performed during incoming inspection of the ceramic materials. Finished-product inspection may range from limited testing (e.g., shorts and opens to ensure that the product was built to print) to additional functional performance testing on each substrate. Test coupons on each panel may be used for electrical performance checks (e.g., impedance, resistance), and destructive mechanical tests for feature size conformance. The extent of testing at this level is determined by the functional complexity of the circuits, final assembly testing, and economics.

The original equipment manufacturer (OEM) or module or component manufacturer may perform testing of the ceramic substrate, the assembly using the substrate, or depending on the test requirements at the lower levels, may not perform any further testing until the end item goes to final test.

As one moves up the supply chain, the test methods, equipment, and overall specifications become more unique and specialized to an application.

2.5.1.1 Material Characterization Tests

At the material supplier level, the testing to provide characterization data for design has the potential for some degree of standardization. A number of test methods have been developed that can be used for electrical characterization of ceramic materials, and no single method satisfies the broad range of application of ceramic materials. Each method has its own advantages and disadvantages. The National Institute of Standards and Technology (NIST) Technical Note 1520 "Dielectric & Conductor Loss Characterization and Measurements on Electronic Packaging Materials" is an excellent reference for general descriptions of test methods [29].

As the commercial wireless market began to emerge, it was recognized that standard high-frequency test methods for material characterization were

limited. What was desired was a methodology that had the following attributes:

1. Has simple sample fabrication
2. Uses simple test fixtures and launchers
3. Uses an electrically well-defined structure
4. Allows easy verification of critical dimensions
5. Has the capability to extract materials data (dielectric constant, loss tangent, attenuation) at numerous data points over a broad frequency range using one setup
6. Uses test samples typical of actual circuit use

Of the different possibilities, resonator structures were found to be well suited for materials characterization. Although dielectrics and conductors can be characterized independently, it is of key importance in a ceramic material system to characterize the conductor and dielectric together, as they will be in actual use. There can be interactions or influences at the conductor–dielectric interface that can significantly affect performance, particularly at higher frequencies. As frequencies increase, methods for materials characterization become fewer, more sensitive, and complex. All the possible methods cannot be fully treated in this chapter, and the reader is referred to the references for further information. Table 2.8a summarizes some of the test methods and considerations in their use for material characterization, whereas Table 2.8b charts the attributes of the general test methods [30].

TABLE 2.8A

A Comparison of Common Material Characterization Techniques

Type	Form	Characterization	Frequency Range	Comments
T resonator	Microstrip	Conductor and dielectric	1–25 GHz	Multiple data points, computational corrections
Ring resonator	Microstrip	Conductor and dielectric	1–40+ GHz	Gap sensitive
Stripline resonator	Stripline	Conductor and dielectric	> 20 GHz	Gap sensitive
Open resonator	Dielectric (large)	Dielectric	15–100 GHz	Position sensitive
Cavity methods	Dielectric (small)	Dielectric	0.1–60 GHz	High Q, limited data points, and very accurate
Meander line	Microstrip	Conductor and dielectric	40+ GHz	Simple testing
Waveguide substitution	Dielectric	Dielectric	100 GHz	Dimensionally sensitive

TABLE 2.8B

Key Attributes of Materials Characterization Techniques

Type	Well-Defined	Simple Sample Fab	Simple Fixturing	Easy Dimension Measurement	Broad Frequency Range	Numerous Data Points	Typical of Circuits
T resonator	X	X	X	X	X	X	X
Ring resonator	X	X	X	X	X	X	X
Stripline	X	—	X	—	—	X	X
Open resonator	—	X	—	X	X	X	—
Cavity	X	X	—	X	—	—	—
Meander	—	X	X	X	X	X	X
Waveguide	—	X	—	X	—	X	—

2.5.2 Design for Test

Rework or repair is not permitted in many high-density applications; however, if one is faced with the possibility of change or repair in a packaging system that uses multilayer interconnections, it is essential that repair and change methods be considered in the initial design.

The use of multilayer interconnection structures for high-density and high-performance interconnection and packaging complicates the routing, change, and repair of circuit interconnections. The need to consider change of techniques occurs primarily in applications of digital random logic circuits. Change and repair considerations are typically not necessary with logic structures that are low cost, use very few circuits, have an easily testable and predictable logic configuration, or for memories or similar applications that have very regular interconnections with little possibility of future changes.

The trade-offs in the decision to accommodate change or allow repair are complex; development and production hardware costs, electrical performance, packaging density, quality, reliability, and the need for quick turnaround times (time to market) to implement changes will vary with each application.

Even with extensive modeling and simulation, because of the complexity of multilayer structures, such as in multichip modules (MCMs) with hundreds of thousands of gates or modules with a large number of die or packages, it is difficult to fully model or test all the conditions that may occur. In addition, change typically occurs in the initial system test and prototype debugging development stages, as well as in early production. For complicated interconnect systems, a means to change or repair circuitry without having to replot and fabricate a module with updated circuit interconnections every time a change occurs should be considered. The repair technique should have electrical and mechanical reliability and quality comparable to the initial interconnections.

There is a perception that ceramic circuitry is not changeable; however, there are techniques that have been used for successful repair and change of multilayer ceramic circuits [31].

One method suitable for multilayer thick-film chip and wire prototype circuits uses small ceramic "change bars" and wire bonds to externally reconfigure nets. Wire bonds are removed from the die and substrate, isolating the die from the substrate interconnections. Small metallized alumina change bars are used to reconstruct the signal path and wire bonds are used to interconnect the change bars and die. Another approach uses surface repair links. This technique is suitable for solder bump and surface mount terminations. Inner layer nets are connected to the substrate surface with a via to a pad that connects through a narrow link to another pad used for IC solder bump or lead attachment. The die terminal is isolated from the internal net by cutting the link, and the net reconfigured with wiring. Note that the repair links can serve as thermal links for more uniform surface soldering. The link minimizes the effects of heat being drawn off by via holes and internal connections that are typically nonuniform, resulting in inconsistent solder joints. Yes, repair links reduce packaging density, can degrade performance, and can increase cost, but these factors must be weighed against the time and cost of redesign, multiple re-layouts, and fabrication iterations.

Ultimately, the system designer or packaging engineer must determine if change provisions must be accommodated in the design, and then through careful analysis of the trade-offs, choose the techniques best suited for each application.

2.5.3 High-Frequency Measurements

> When you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meager and unsatisfactory kind.

These golden words of Lord Kelvin [32] are very much applicable in any field of knowledge. In the context of microwaves and RF measurements, these words appear to have more meaning, as the things we cannot see are hard to visualize, and visualizing them correctly is a tough task.

For any measurement to be taken we need a device, the physical parameter we are trying to measure, and a standard or reference against which we want to measure the device. We should have the equipment or the means to measure the physical quantity. We should also know how accurately and how precisely we can measure the quantity. Precision and accuracy are two different things. Precision puts a limit on the measurement device whereas accuracy has a probabilistic nature.

Already RF and microwaves are a part of the EM spectrum. They are made up of time- and space-varying rotating electric field and magnetic field vectors in planes perpendicular to each other whereas the wave propagates in a plane perpendicular to both these vectors. The area of interest as regards the RF/microwave measurements is to be able to measure the physical properties associated with these high-frequency EM waves.

Before we get into the RF or microwave measurements, we should be first clear as to what we want to measure, or what could be important to have a better understanding about these kinds of EM waves; not only about the wave but also about the interaction of the microwaves with the devices through which they propagate.

We should list the physical quantities that interest us. They could be the frequency, wavelength, phase, amplitude, etc. Apart from these physical quantities, we should also have knowledge of other quantities that are measurable, which would enhance our understanding of the behavior of devices through which the microwaves propagate. In theory, microwaves need no medium to propagate, but surely could be reflected, scattered, or absorbed like any other EM wave, depending on the materials they interact with.

Microwave technology, just like the microelectronic technology, is moving towards smaller, faster, and cheaper devices and systems. It has been made possible because of the development of MICs. With the continuing advancements in fabrication facilities, computer aided design (CAD) tools, etc., the older, bulkies, and costly microwave components and devices are making way for smaller, planar, inexpensive devices that could be fabricated on monolithic or hybrid substrates. MICs have been there for 45 years, where the active and/or passive components are bonded to the substrate, whereas the MMICs are pretty recent technologies, where the active and passive devices, along with the transmission lines are grown on the semiconductor substrates, and there could be multiple layers of metallizations and insulations just like in IC fabrication technology.

After the design and fabrication of the MICs, there is a need to test the devices and to measure the device characteristics. The high-frequency measurements make a very useful field of study on hybrid, ceramic, or semiconductor substrates. As most measurements involve planar devices, there is a need of on-wafer measurements.

There are scores of microwave devices that need to be measured. The most common measurements that are done are the frequency measurements, but we are also interested in phase measurements depending on the device under test (DUT). We can use various equipments like spectrum analyzer, vector network analyzer, etc. [33]. Most of the devices that we measure will be two-port devices; that is, the input is applied at one port and the output is taken at the other port. So we will basically be measuring devices, a group of devices that form a part of the system, and microwave circuits.

The need for faster electronics has made MMICs, high-speed devices/interfaces, and or modules, etc., very common. The electrical engineers should also be well versed with the RF/microwave counterpart in today's

changing markets, where speed is money, and "faster, smaller, and cheaper" are the keywords. This section gives an idea in understanding the basic RF /microwave measurements.

2.5.3.1   Device Parameters

To simplify the study of the microwave devices and circuits, microwave engineers devised certain parameters that could give considerable amount of information about the device, a complete system, or a part of it. The most commonly used parameters are S-parameters. There could be two types of measurements in the microwave devices: reflection and transmission. The S-parameters give a fairly good estimate of these wave properties; hence, an insight into the device characteristics.

2.5.3.2   Calibration

Before we measure any of these parameters, the measurement device needs to be calibrated, which is the technique to get rid of the errors that could be inherent due to the measurement setup, most commonly the cables and/or the probes that are in physical contact with the device. Also, the calibration sets the reference planes for the measurements. The most important consideration here is that the calibrations cannot be done on an infinite bandwidth, and they are a strong function of system noise, vibrations.

   The goal of calibration methods is to provide the DUT with an electrically pure connection to the test system terminals. This means that the signal at the test ports should have zero magnitude, no phase shift, and a characteristic impedance of Z_0. Mathematically, it means to place an error model between the test setup and the DUT, so that it can account for any errors due to the testing device. Calibration is a procedure that basically quantifies these errors [33–36].

2.5.3.3   Calibration Standards

All the physical quantities are measured with respect to a reference, which is called a *standard*; for example, a meter for length, gram for mass, etc. Similarly, the device calibration at high frequency is done by measuring various known physical devices called *standards*. The frequency response of these devices is known. In most of the calibration techniques, commonly used standards are the short circuit, open circuit, load, and a thru line. Together, these standards calibrate the RF path between the measurement device and the DUT. But no standard is ideal and has losses as the EM energy travels only in a part of the device owing to skin effect. So we have correction factors which, in turn, make up for the nonideal behavior of the calibration standards. It is very important to note that the correction factors, commonly known as *calibration coefficients* are only valid for a combination of test system

probe and the calibration standard; if any of these is changed in the test setup, it will affect the calibration coefficients.

2.5.3.4   CPW Probes

Coplanar waveguide has an advantage over microstrip because of the fact that CPW line width is independent of the line impedance. The CPW probe is a microwave transition from coaxial to coplanar wave probe pad [37]. Care must be taken to design transitions that have minimum loss.

2.5.3.5   On-Wafer Characterization

Owing to the complexity of die behavior at the wafer, the knowledge of the CPW probes, calibration, and characterization was not only time consuming but also nearly impractical for high-volume purposes. So there was a need to measure the RF behavior of devices on-wafer, as multiple dies could be characterized simultaneously with ease.

The wafer may have both active and passive devices. The electrical models for the devices are developed by making measurements on these devices at RF; the circuits are designed using these models. If the models are not accurate, then the circuit performance will not be optimum. So it is not only essential to calibrate the DUT but also on the wafer to eliminate the parasitics associated with the wafer.

Therefore, to characterize DUT on a wafer basically involves two steps: (1) vector network analyzer (VNA) calibration and (2) calibration substrate.

The first step sets the reference planes at the probe tip, whereas the second step moves the electrical reference plane from the probe tip to the DUT plane. It is important to have the calibration structures placed near the DUT because the substrate resistivity and oxide thickness vary across the wafer.

2.5.3.6   De-Embedding

De-embedding parasitics can be efficiently implemented with the following factors taken into consideration:

1. The probe pads should be as small as possible. Smaller the probe size, smaller would be the capacitance to the ground and to the surrounding interconnects.
2. Having low-inductance ground paths are important to help in de-embedding the parasitics efficiently.
3. The parasitics would be different than that of the dummy test structures, for any device. So it is required that the DUT should be at the same substrate.
4. The design of the pads and the interconnects should be done for high isolation, which would account for the substrate differences,

when it is not possible to have the DUT and the dummy test structures on the same substrate.

For the active devices, the pad parasitics can have a considerable effect on the transistor cutoff frequency. For field effect transistors (FET), the cutoff frequency is defined as:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \cong |h_{21}| - f$$

where g_m is the transconductance, C_{gs} is the gate-source capacitance, C_{gd} is gate-drain capacitance, h_{21} is the gain, f is frequency. Making the pads as small as possible could minimize the previously stated effect.

2.5.3.7   Noise

The noise figure measurement of an on-wafer device could be strongly affected by the probe pads and the interconnects. Eventually, with an increase in the pad size and decrease in the DUT size, the noise performance of the active device is dominated by the probe-pad impedance. Also, the probe pad contributes to the noise, especially on conductive substrates; this is due to the fact that the pads capacitively couple to the substrate through the oxide layer.

2.6   Summary

This chapter has concentrated on LTCC and the major differences in properties and processes that are unique to multilayer ceramic design. The values used in the chapter typically describe the concepts and examples. It should be recognized that there are continuing material property and process improvements. It should also be noted that there are differences between material supplier and foundry design guidelines, and differences between the various foundry design guidelines even when the same material system is used. Most LTCC foundries publish different levels of values and tolerances for their design guidelines. Preferred or standard specifications based on the most cost-effective/volume-production considerations for their processing are stated along with premium or high-density specifications. As with most features or guidelines, more stringent values or tolerances can be achieved, but at an increased cost. It is essential that prior to proceeding with an LTCC design that the design guide published by the foundries of choice be consulted, and direct interaction with the foundry-manufacturing engineers take place to define the design. There is a wealth of information

available from the LTCC foundries with excellent engineering data and is in much more detail than is practicable to treat in this chapter [32,38,39].

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3

ThermoMechanical Design

Al Krum

CONTENTS

3.1   Introduction

All electronic components, both active and passive, dissipate heat. In most
cases, this heat is unwanted and affects both the electrical performance and
the reliability of both the component and system.

When the temperature is increased because of self-heating or an environ-
mental change, active devices will see parametric changes, such as forward
drop, gain, leakage, and offset that may affect the electrical performance.

The value of a passive device also changes with temperature. For example, resistors have temperature coefficients that range from several parts per million per degree Celsius to several hundred. Capacitor values, depending upon the dielectric material, change from several parts per million per degree Celsius to tens-of-percents. These parameter variations are well documented and are usually included in circuit simulations. The electrical designer may compensate for these temperature changes using various circuit design techniques. A failure caused by a parametric change as a result of increased temperature is usually considered a "soft" failure — one in which the system may still operate, but not within specifications.

It is well known that component reliability decreases with increasing temperature. Some components have a threshold temperature above which their failure rate increases dramatically. Other components follow the Arrhenius equation [1–3]:

$$F = Ae^{-E_A/KT} \tag{3.1}$$

where
F = failure rate
A = constant
E_A = activation energy in electron volts (eV)
K = Boltzmann's constant (8.63×10^{-5} eV/K)
T = junction temperature in Kelvins

The activation energies E_A for various failure mechanisms are listed in Table 3.1.

Device failure rates at different temperatures can be compared, using an extension of Equation 3.1.

$$\frac{F_1}{F_2} = \frac{Ae^{E_A/KT_1}}{Ae^{E_A/KT_2}} \tag{3.2}$$

where
F_1 = failure rate at temperature T_1
F_2 = failure rate at temperature T_2

If a device with an activation energy of $E_A = 1.0$ eV were operating at 20°C and the temperature raised to 30°C, then the failure rate would increase by a factor of 3.7. If the same device were operating at 75°C and its temperature raised to 85°C, the failure rate would see an increase by a factor of 2.5 [5].

Electronic packaging usually consists of dissimilar materials that expand at different rates on heating. Most materials expand when their temperature is raised and contract when cooled.

TABLE 3.1

Activation Energies for Failure Mechanisms

Failure Mechanism	Activation Energy (eV)
Corrosion	0.53–0.70
Electromigration	0.68–0.95
Gate oxide	0.3–0.7
Contamination	1.0
Charge injection	1.3
Gold–aluminum films	1.0
Gold wire–aluminum film	0.55
Hillock	0.68–0.95
Aluminum wire–gold film	0.73
Gold–aluminum wire couples	0.69–1.0

Sources: From JEDEC Solid State Technology Association, JEP122-A, Arlington, VA, December, 2001; Epstein, D., Application and Use of Acceleration Factors in Microelectronic Testing, in *Solid State Technology*, November 1982; Harmon, G.G., *Wire Bonding in Microelectronics, Materials, Processes, Reliability, and Yield*, McGraw-Hill, New York, 1997.

When two dissimilar packaging materials are joined and subsequently heated, a differential expansion, or mismatch, occurs and introduces stress in the materials and joints. The temperature variations from ambient temperature occur during the manufacturing process and during normal operation. Manufacturing processes that raise the temperature include epoxy cures and solder reflow. In normal operation, the unit will see its temperature rise due to self-heating and due to a variation in the operating environment. If the differential expansion is not accommodated, then a fracture will occur in one or more of the materials. This fracturing during operation is called *thermal fatigue*. Subsection 3.5.1 will discuss mechanical stress [6].

Thermomechanical design is a vital part of the design process and needs to be addressed early in the design of the chip and its packaging. Packaging trade-offs need to be evaluated early enough so that an optimal design is achieved.

As discussed in other chapters of this book, there are three basic purposes for ceramic packages:

1. They provide an interconnect medium from the semiconductor devices and the passive devices to the next level of assembly — the circuit card.

2. They provide environmental and mechanical protection.

3. They provide a method of transferring the heat from the junction to the ambient.

Ceramic substrates also have three basic purposes: electrical interconnection, mechanical mounting of components, and heat transfer. In this chapter,
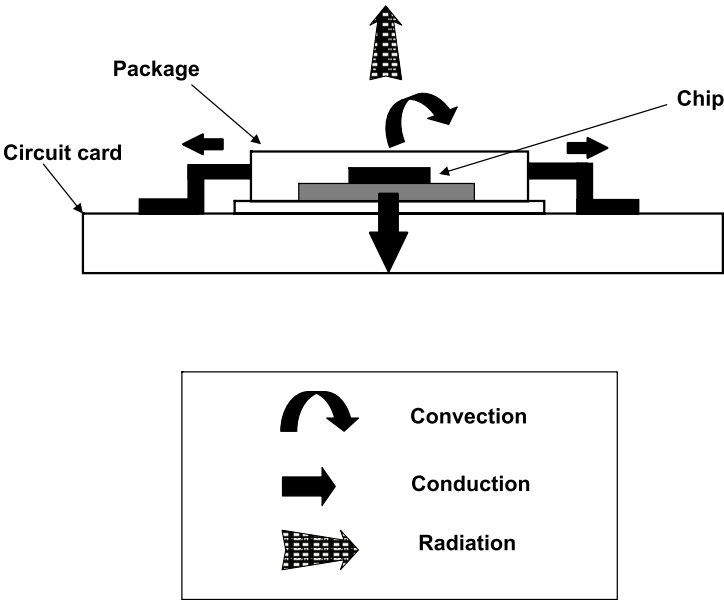
FIGURE 3.1
Mechanisms of heat transfer.

the use of ceramic interconnects for heat transfer and mechanical support will be discussed.

3.2 Fundamentals of Heat Transfer

3.2.1 Mechanisms of Heat Transfer

There are three mechanisms for heat transfer — conduction, convection, and radiation — as depicted in Figure 3.1. These mechanisms will be discussed from Subsection 3.2.2 through Subsection 3.2.4. Several basic principles of thermodynamics need to be addressed prior to delving into heat transfer.

3.2.1.1 First Law of Thermodynamics

A steady-state condition is one in which there is no energy storage, and the heat-in equals the heat-out. This empirical law is a way of saying that energy can be neither created nor destroyed. It is also called "conservation of energy." Mathematically, for a closed or isolated system, the first law of thermodynamics can be stated as:

$$Q - W = \Delta E \tag{3.3}$$

$$\Delta E = 0 \qquad\qquad\qquad (3.4)$$

where
   Q = heat
   W = work
   E = stored energy
   ΔE = change in energy [7]

3.2.1.2   Second Law of Thermodynamics

The second law of thermodynamics states that heat always flows from a hotter region to a lower temperature. In electronic systems, the heat flows from the active and passive heat-generating components to the ambient [8].

3.2.2   Conduction

Thermal conduction is a mechanism in which heat flows through a solid, liquid, or gas, or between two media in intimate contact. Conduction is the most influential mechanism for heat transfer within solids. It involves the transfer of kinetic energy from one electron to the next, causing no visible motion of particles. This transfer of energy is similar to that of electric charge. Good electrical conductors such as silver and copper are also good thermal conductors. Copper has a thermal conductivity of 401 W/m·K and a very low electrical resistivity of 1.60×10^{-6} Ω·cm. Silver's thermal conductivity is 419 W/m·K, and electrical resistivity is slightly lower at 1.55×10^{-6} Ω·cm [9].

Liquids conduct thermal energy in a lesser extent than solids. When a material undergoes a phase change from a solid to a liquid, there is a lessening of the molecular bonds and a resulting weakening of the order state of the solids results. This leads to more freedom for thermal motion of the molecules and a lowering of the material's thermal conductivity. An example of the low thermal conductivity of liquids is water's value of 5.22 W/m·K [9].

When a material undergoes a phase change from liquid to gas, there is a further loosening of the molecular bonds. The gas molecules, free to move in any direction and restrained only by random collisions, have a significantly lower probability that contact areas will exist. As a result, the thermal conductivity of gases is quite low. For example, the thermal conductivity of air is 0.0024 W/m·K. This is many orders of magnitude lower than the thermal conductivity of water [9].

3.2.2.1   Fourier's Law (for conduction only)

Fourier's law of heat conduction, named after French mathematician Jean Fourier, states that the rate of heat flow equals the product of the area normal to the heat flow, the temperature gradient along the path, and the thermal conductivity of the material. Mathematically, this is expressed as:

$$\frac{dq}{dt} = -KA\frac{dT}{dX}$$ (3.5)

where
  Q = Heat generated per unit volume in J/cm³
  t = Time in seconds
  K = Thermal conductivity of medium in W/m-°K or W/in.-°C
  A = Cross-sectional area of medium normal to the heat flow path in square inches or square centimeters
  T = Temperature of medium in degree Celsius
  X = Position along the medium in inches or centimeters
  q = Heat flow in watts normal to the cross-sectional area of heat transfer

$$\frac{dQ}{dt} = \text{ power in watts or calories/sec}$$ (3.6)

$$\frac{dT}{dX} = \text{ temperature gradient in °C/in or °C/cm.}$$ (3.7)

The temperature gradient and the cross-sectional area are defined at the same point x as shown in Figure 3.2. Heat flow is considered positive when the temperature is decreasing.

Fourier's law can be extended from the one-dimensional generalization described earlier to three dimensions. For an elemental volume ΔV with dimensions Δx, Δy, and Δz, that is generating Q_v watts/unit volume as shown in Figure 3.3, the following equations hold:

$$q_x = -k_x\,\Delta y\,\Delta z\,\frac{\partial T}{\partial X}\quad\text{at point 3}$$ (3.8)

$$q_{x+\Delta x} = -k_x\,\Delta y\,\Delta z\,\frac{\partial T}{\partial X}\quad\text{at point 4}$$ (3.9)
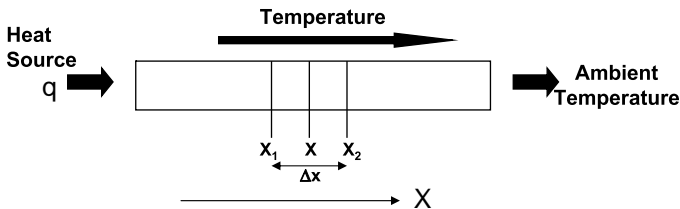
FIGURE 3.2
Fourier's law.
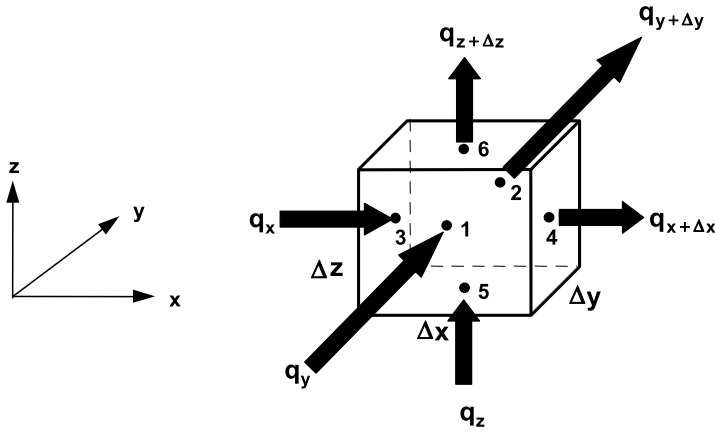
FIGURE 3.3
Elemental volume.

$$q_y = -k_y \, \Delta x \, \Delta z \, \frac{\partial T}{\partial Y} \ \text{ at point 1} \tag{3.10}$$

$$q_{y+\Delta y} = -k_y \, \Delta x \, \Delta z \frac{\partial T}{\partial Y} \ \text{ at point 2} \tag{3.11}$$

$$q_z = -k_z \, \Delta x \, \Delta y \, \frac{\partial T}{\partial Z} \ \text{ at point 5} \tag{3.12}$$

$$q_{z+\Delta z} = -k_z \, \Delta x \, \Delta y \, \frac{\partial T}{\partial Z} \ \text{ at point 6} \tag{3.13}$$

Applying the conservation of energy principle (heat-in = heat-out) described in Subsection 3.2.1.1 to the elemental volume ΔV, and adopting the convention that heat-in is positive:

$$
\begin{aligned}
&\left[\left(-k_x \, \Delta y \Delta z \frac{\partial T}{\partial x}\right)\Big|_3 - \left(-k_x \, \Delta y \, \Delta z \frac{\partial T}{\partial x}\right)\Big|_4\right] \\[4pt]
+&\left[\left(-k_y \, \Delta x \, \Delta z \frac{\partial T}{\partial y}\right)\Big|_1 - \left(-k_y \, \Delta x \, \Delta z \frac{\partial T}{\partial y}\right)\Big|_2\right] \\[4pt]
+&\left[\left(-k_z \, \Delta x \, \Delta y \frac{\partial T}{\partial z}\right)\Big|_5 - \left(-k_z \, \Delta y \, \Delta y \frac{\partial T}{\partial z}\right)\Big|_6\right] \\[4pt]
+&Q_v \, \Delta x \, \Delta y \, \Delta z = 0
\end{aligned}
\tag{3.14}
$$

Dividing both sides of the equation by the elemental volume $\Delta V = \Delta x \, \Delta y \, \Delta z$:

$$\left(\frac{1}{\Delta x}\right)\left(k_x \frac{\partial T}{\partial x}\right)\Big|_3^4 + \left(\frac{1}{\Delta y}\right)\left(k_y \frac{\partial T}{\partial y}\right)\Big|_1^2 + \left(\frac{1}{\Delta z}\right)\left(k_z \frac{\partial T}{\partial z}\right)\Big|_5^6 = -Q_v. \quad (3.15)$$

Taking the limit as $\Delta V \to 0$:

$$\lim_{\Delta x \to 0}\left(\frac{1}{\Delta x}\right)k_x \frac{\partial T}{\partial x}\Big|_3^4 = \lim_{\Delta x \to 0}\left(\frac{1}{\Delta x}\right)k_x \frac{\partial T}{\partial x}\Big|_{x,y,z}^{x+\Delta,x,y,z} \frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) \quad (3.16)$$

Repeating this process in the y and z directions, the result is the three-dimensional heat conduction formula for steady state:

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) = -Q_v. \quad (3.17)$$

For non-steady-state conditions, such as in warm-up or in the application of power in a time-dependent manner, Equation 3.17 is modified.

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) = -Q_v + \rho C_p \frac{\partial T}{\partial t} \quad (3.18)$$

where
ρ = density in kg/m³
C_p = specific heat in W-sec/kg-°C
t = time

Fourier's law, described in Equation 3.5, can be rewritten as:

$$dT = -\left(\frac{Q_K}{k\,A}\right)dx. \quad (3.19)$$

Integrating both sides of this equation,

$$\int_{T_1}^{T_2} dT = -Q_k \int_{x_1}^{x_2} \frac{dx}{kA_k}. \quad (3.20)$$

Assuming a homogeneous material whose thermal conductivity does not vary over the length
$L = x_2 - x_1$, Equation 3.20 reduces to

$$\Delta T = T_2 - T_1 = Q_k \frac{L}{k A} \tag{3.21}$$

where $\Delta T = T_2 - T_1$ is the temperature difference along the length L.
The thermal resistance θ can be defined as:

$$\theta = \frac{L}{k A} \tag{3.22}$$

Combining Equation 3.21 and Equation 3.22 [8,10]

$$\theta = \frac{\Delta T}{Q_k}. \tag{3.23}$$

3.2.2.2   Electrical Analogies

The understanding of thermal characteristics can be aided by considering the various thermal properties analogous to electrical properties. The rate of heat flow P (or Q) is analogous to current flow I. Temperature drop ΔT is analogous to voltage drop V. Thermal resistance θ is analogous to electrical resistance R. Thermal conductivity K is analogous to electrical conductivity σ.

When several materials are joined together and heat flows through them in a series fashion, such as a die attached to a ceramic package, the equivalent thermal resistance is the sum of the individual thermal resistances. This is analogous to several resistors in series. For N materials in series, each with its own thermal resistance θ, the equivalent thermal resistance θ_{equiv} is

$$\theta_{Equiv} = \theta_1 + \theta_2 + \theta_3 + \dots + \theta_N \tag{3.24}$$

where θ_1 through θ_N = thermal resistance of each material.

When there are multiple heat paths from the dissipating element to the ambient, then the equivalent thermal resistance can be considered to be the parallel equivalent of the individual resistances. This is analogous to electrical resistances in parallel. For N thermal paths, the θ_{equiv} is calculated using the formula:

$$\frac{1}{\theta_{Equiv}} = \frac{1}{\theta_1} + \frac{1}{\theta_2} + \frac{1}{\theta_3} + \dots + \frac{1}{\theta_N}. \tag{3.25}$$
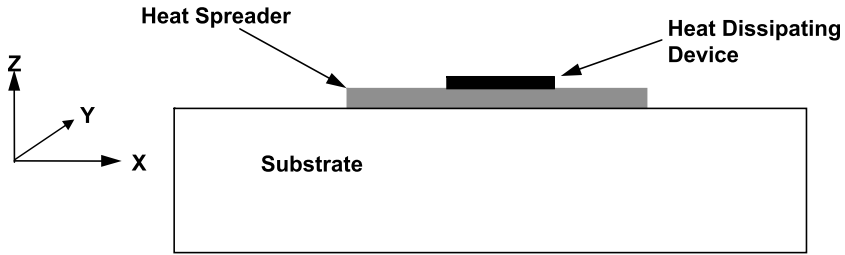
FIGURE 3.4
Heat spreader. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 3–6, 1995, Los Angeles, CA. With permission.)

3.2.2.3 Heat Spreading

According to the second law of thermodynamics, conductive heat flows from a relatively small dissipating element to the ambient in a complex manner. As described in Fourier's law in Subsection 3.2.2.1, the heat flow is three-dimensional. When a high thermal conductivity material is placed in the heat path as shown in Figure 3.4 [11], the heat flow in the x and y horizontal directions is greater than in the vertical direction z. The heat will spread with a resulting increase of the effective thermal cross-sectional area A (in Equation 3.22) of a relatively poor thermal conductivity material. This provides a lower thermal resistance than the configuration without the heat spreader. The heat spreader is typically a high-thermal-conductivity material and is placed between the dissipating element and the heat sink.

The spreading angle α is defined in Figure 3.5. When the thermal conductivity of the lower layers is significantly higher than the current layer, spreading will be at a minimum. Because there will always be some lateral heat spreading attributed to the randomness of the thermal energy, the spreading angle will be greater than $0°$. When the lower material's thermal conductivity is very low (a thermally insulating material) compared to the current layer, the spreading angle will be large, approaching $90°$ asymptotically.
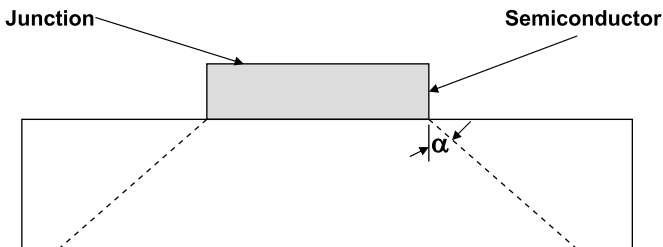
FIGURE 3.5
Spreading angle α. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 3–6, 1995, Los Angeles, CA.

An approximation for the spreading angle, based on the ratio of thermal conductivities of the layers, is given by N.B. Nguyen [12].

$$\alpha = \tan^{-1} \frac{K_1}{K_2} \qquad (3.26)$$

where
   α = spreading angle (degrees)
   K_1 = thermal conductivity of current layer
   K_2 = thermal conductivity of underlying layer

When $K_1 = K_2$, the spreading angle will be 45°. As the ratio of K_1/K_2 increases, the spreading angle asymptotically approaches 90°.

3.2.2.3.1 Spreading Angle Example

For the configuration shown in Figure 3.6 [11], which depicts a silicon chip on a direct-bond-copper metallized substrate, the spreading angle in the copper is:

$$\alpha = \tan^{-1} \frac{K_1}{K_2} = \tan^{-1} \frac{401}{21} = 87°.$$

A good approximation in first-order thermal calculations is to use a 45° spreading angle.

A more exact spreading angle model uses 26.6° for cases when the ratio of heat-spreader thickness to heat-dissipating-element side is less than 2 [13].

If the dissipating device is close to the thermal boundaries as shown in Figure 3.7, then the model needs to be adjusted so that there are two resistances in series. The first resistance, θ_1 is the trapezoidal section as shown
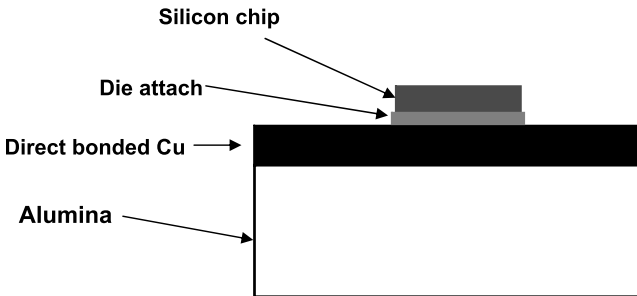
FIGURE 3.6
Silicon chip on direct-bond-copper substrate. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 3–6, 1995, Los Angeles, CA. With permission.)

Figure (a) — Dissipating Element, Thermal Boundaries

Figure (b) — θ_1

Figure (c) — θ_2
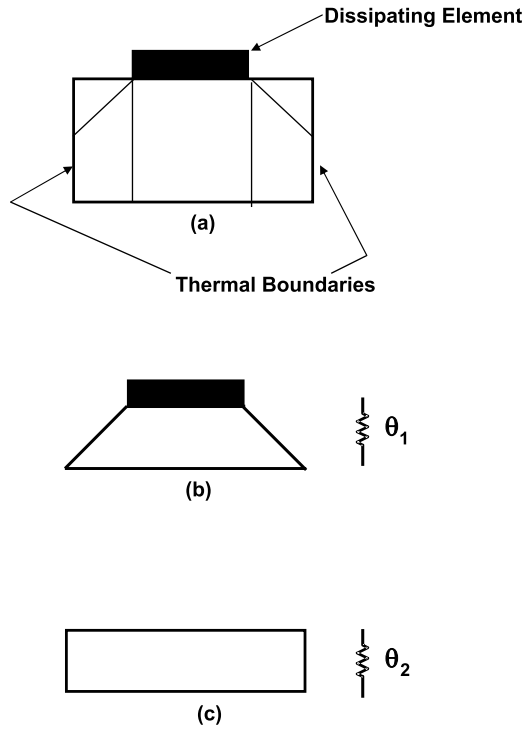
FIGURE 3.7
Restricted spreading. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 3–6, 1995, Los Angeles, CA.)

in Figure 3.7b. The second impedance θ_2, the rectangular section shown in Figure 3.7c, will not have any heat spreading. The total thermal resistance θ_{Total} is the series combination of the trapezoidal and rectangular sections.

$$\theta_{Total} = \theta_1 + \theta_2$$

where
   θ_{Total} = total thermal resistance
   θ_1 = thermal resistance of the trapezoidal section
   θ_2 = thermal resistance of the rectangular section

   Heat spreaders are typically used for small heat sources such as microwave transistors. Typical materials for heat spreaders include molybdenum, copper, beryllium oxide, aluminum nitride, copper-tungsten, Silvar™*, and CVD diamond.

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* Silvar is a trademark of Engineered Materials Solutions, Inc.

3.2.3   Convection

Convection, also known as Newtonian cooling (after Sir Isaac Newton), is a mechanism of heat transfer that occurs only in fluids. It involves the transfer of thermal energy by the mixing of fluids. The amount of convective heat transfer is a function of surface area in contact with the fluid, the temperature difference between the solid and the fluid, and the properties of the fluid. There are two types of convective heat flow — natural (or free) and forced.

The mathematical expression for convective heat transfer is shown in Equation 3.27.

$$Q_c = h_c A_s (T_s - T_A) = h_c A_s \Delta T \tag{3.27}$$

where
  Q_c = heat transferred from a surface to ambient by convection in watts
  h_c = convection heat transfer coefficient in W/cm³-°C or W/in.³-°C
  A_s = surface area in cm³ or in.³
  T_s = surface temperature in degree Celsius
  T_A = ambient temperature in degree Celsius (temperature to which the
          heat is being transferred)

A simplified approximation of Equation 3.27 can be written as:

$$\Delta T = \frac{1}{h_c A_s} Q_c. \tag{3.28}$$

The convective surface thermal resistance θ_s states the quantity of heat transferred through a temperature difference. It is defined as:

$$\theta_S = \frac{1}{h_C A_S}. \tag{3.29}$$

3.2.3.1   *Natural Convection*

In natural convection cooling, the heat flows by conduction from the surface to the fluid particles that are in contact with the surface. The fluid particles in contact with the surface increase their internal energy and cause a resulting decrease in density of the nearby fluid particles. The hotter particles move to a region lower in temperature through buoyant forces. At the lower-temperature region, further energy transfer takes place via conduction. This produces a boundary layer of hot air immediately adjacent to the surface. Natural convection cooling is entirely because of differences in density within the fluids.
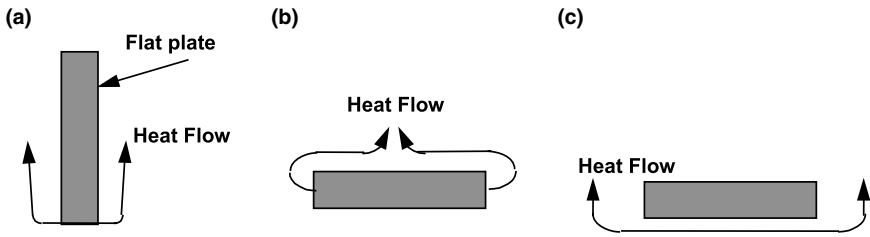
FIGURE 3.8
The value of D in Equation 3.30. (a) D = 0.56 vertical flat plate. (b) Hot top surface of flat plate D = 0.52. (c) Hot bottom surface of a flat plate. D = 0.26.

The convection heat transfer coefficient for natural (or free) convection is calculated by:

$$h = D E \frac{\Delta T^{0.25}}{L^{0.25}} \tag{3.30}$$

where
   D = constant for air properties (see Figure 3.8)
   E = constant for surface configuration ($E = 1.9 \times 10^{-4}$ for a flat plate)
   ΔT = temperature difference in degree Celsius between dissipater and
            ambient air
   L = characteristic length in centimeters or inches of dissipater surface with
            area factor

3.2.3.2 Forced Convection

In forced convection, the heat is transferred from the solid to the adjacent fluid particles in the same manner as in natural convection. However, the fluid motion is caused artificially by fans, pumps, or blowers.
In forced convection, the convection heat transfer coefficient is calculated from:

$$h = B \frac{V^{0.75}}{L^{0.25}} \tag{3.31}$$

where
   B = constant of air properties and surface configuration
   V = linear velocity of air in cm/sec or in./sec
   L = characteristic length of surface in direction of flow in centimeters or
            inches

On examining Equation 3.31, it is obvious that the key parameter in the amount of heat removed in forced convection is the linear velocity of the air current as it passes the dissipating element.

In convection cooling, there are several dimensionless parameters [14]:

$$\text{Reynolds number } \text{Re} = \rho V \frac{d}{\mu} \qquad (3.32)$$

where
ρ = fluid density in kg/m³
μ = viscosity of fluid
V = linear velocity of fluid in cm/sec or in./sec
d =length of surface which fluid flows across

$$\text{Prandtl number } \text{Pr} = C_p \frac{\mu}{k}, \qquad (3.33)$$

$$\text{Nusselt number } Nu = h \frac{d}{k}, \qquad (3.34)$$

$$\text{Stanton number } St = \frac{Nu}{\text{Re}\,\text{Pr}}. \qquad (3.35)$$

Forced convection cooling can be divided into laminar flow and turbulent flow. The transition from laminar to turbulent flow in air usually occurs at a velocity of 180 ft/min (180 lfm). In laminar (or streamline) flow, the fluid particles follow a smooth, continuous path where the velocity vectors of the particles are always parallel and never intersect. The heat is transferred by molecular conduction in the fluid and by the solid–fluid interface. Turbulent flow, characterized by the irregular motion of fluid particles, has eddies in the fluid in which the particles are continuously mixed and rearranged. The heat is transferred in turbulent flow from the eddies back and forth across the streamlines. The greater heat transfer occurs for turbulent flow.

The laminar heat transfer coefficient for flow over a flat plate is the most-often-used expression for computing external-flow heat transfer. The flat plate, which can be a substrate or a package heated over its entire surface, has a Nusselt number:

$$Nu_x = 0.332\,\text{Pr}^{\frac{1}{3}}\,\text{Re}_x^{\frac{1}{2}} \qquad (3.36)$$

where x is measured along the flow direction on the plate.

The average heat transfer coefficient for the plate is obtained by integrating over the length of the plate to obtain:

$$Nu = \frac{hL}{k} = 0.664 \, Pr^{\frac{1}{3}} \, Re_L^{\frac{1}{2}}. \tag{3.37}$$

For turbulent flow, the local Nusselt number is:

$$Nu_x = 0.0288 \, Re_x^{\frac{4}{5}} \, Pr^{\frac{1}{3}} \tag{3.38}$$

and the average is:

$$Nu = 0.036 \, Re_L^{\frac{4}{5}} \, Pr^{\frac{1}{3}}. \tag{3.39}$$

3.2.4 Radiation

Radiation cooling, the transfer of heat by electromagnetic emission, primarily in the infrared wavelengths (0.1–100 µm), does not require a transport medium. All objects with a temperature above 0 K emit thermal radiation.

The absorption of radiation between surfaces for most earth-bound electronic systems is relatively small.

In the vacuum of space, radiation is a key mechanism for heat transfer. Inside the spacecraft, conduction is the primary mode of heat transfer from the components, through various levels of packaging, to the surface of the space of the vehicle. At the surface, the heat is transferred via radiation. Ceramic interconnects, whether used as substrates or packages, do not play a significant role in radiation cooling in ground, airborne, or space applications. Therefore, there will be no further discussion of radiation cooling in this chapter. For further information on radiation cooling, the reader is directed to the references [8,10,14].

3.3 Thermal Design

In order to predict temperature rises in electronic components, a thermal model needs to be created, which shows all of the dissipating elements and the entire heat path. Starting at the junction of each dissipating semiconductor, the model needs to include all layers in the thermal path: the die attach, substrate (if used and its attachment), package, thermal interface materials (if used), heat sink and circuit card assembly (CCA). The heat dissipated in each component, physical layout, and availability of cooling air are required to calculate the temperature-rise predictions.

TABLE 3.2

Thermal Interface Materials

Material	Typical Thickness (in.)	Thermal Conductivity (W/m·K)	Dielectric Strength (V)
Thermal grease	0.003	0.7	—
Sn 63	0.005	50	na
Mica	0.002–0.003	0.71	—
Phase change	0.002	4	3,900
Elastomer	0.010	6	4,000
Gap filler	0.010	1.5	4,000
Epoxy film	0.005	6.5	na
Diamond-filled epoxy	0.005	11.6	>2,250
Adhesive tape	0.002–0.015	0.6	
Ceramic wafers			
Alumina wafer	0.015–0.060	25	>9,000
Aluminum nitride wafer	0.015–0.060	170	>9,000
Beryllia wafer	0.015–0.060	217	>11,500
Polyimide film		0.15	

Sources: From CRC, *CRC Handbook of Chemistry and Physics*, Boca Raton, FL: CRC Press, 1984; Wells, R.H. and Hunadi, R., Low outgassing, high thermal conductivity greases, in *International Conference on Microelectronics*, 1998; AI Technology, Product Literature, http://www.aitechnology.com/, accessed September 26, 2003; Williams Advanced Materials, Packaging Materials-Solder Alloys, 2002; Theramagon, Product Literature, http://www.thermagon.com/, accessed September 26, 2003; Berquist Company, Product Literature, http://www.bergquistcompany.com/thermal_materials.cfm, accessed September 26, 2003; Chromerics, Product Literature, http://www.chomerics.com/products/thermal.htm, accessed September 26, 2003; MatWeb: The Online Materials Information Resource, www.matweb.com, accessed September 26, 2003.

The thermal resistances for many discrete components, both active and passive, have been characterized, and their values published in data sheets. Table 3.2 lists the properties of various thermal interface materials. For custom components, a thermal model needs to be created.

Many physical designers approach the thermal predictions in a two-step manner. First, they perform some first-order individual device calculations to determine if the temperature rises for the highest heat flux devices will be within specifications. If not, iterations are made on materials, dimensions, and the cooling method. Once a satisfactory first-order prediction is made, then a complete thermal analysis is performed using one or more of the simulation tools discussed in Section 3.6.

An example of a first-order analysis will be shown in the following subsection.
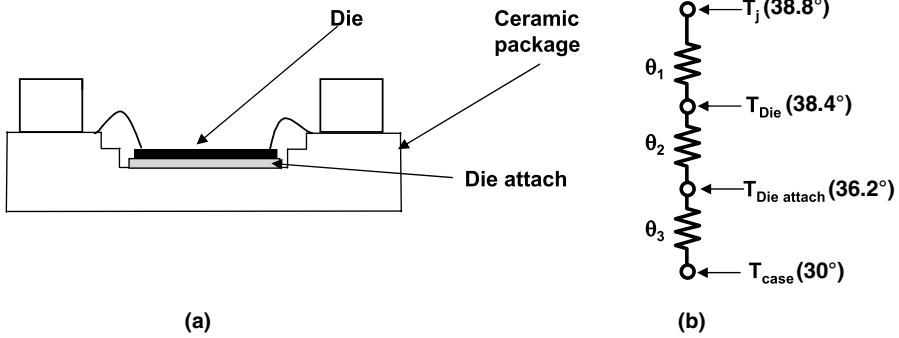
FIGURE 3.9
(a) Packaged die cross section. (b) Electrical analog.

3.3.1 Thermal Design Example

A custom CMOS integrated circuit measuring $0.35 \times 0.35 \times 0.022$ in. is mounted in a 1-in. square ceramic quad flat package (QFP). The device dissipates 10 W during normal operation. Find the thermal resistance from junction to case.

A cross section of the die, die attach, and package is shown in Figure 3.9 along with the thermal analog. The die consists of many hundreds of thousands of transistors spread across its entire area. For the purpose of the first-order analysis, the entire die area can be considered as one large junction generating a uniform heat flux. The thermal resistance for the die θ_1 is calculated using Equation 3.22 with the length of the heat path L replaced by the thickness t. The dimensions are first converted to metric. The thickness t becomes 5.59×10^{-4} m, and the length and width become 8.89×10^{-5} m.

$$\theta_1 = \frac{t_1}{K_1 A_1} = \frac{5.558 \times 10^{-4}\ m}{(147\ W/m-K)(8.89 \times 10^{-5}\ m)^2} = 0.048°C/W.$$

The die is attached to the package with conductive epoxy that has a thermal conductivity of 3.0 W/m·K. The thermal resistance of the die attach layer, θ_2 is calculated as follows. The thickness of 0.002 in. is first converted to 5.08×10^{-5} m. There is no heat spreading in the die.

$$\theta_2 = \frac{t_2}{K_2 A_2} = \frac{5.08 \times 10^{-5}\ m}{(3\ W/m-K)(8.89 \times 10^{-3}\ m)^2} = 0.215°C/W.$$

The package base is 0.040 in. (1.02×10^{-3} m) thick 92% alumina, which has a thermal conductivity of 17 W/m·K [22]. The thermal resistance of the package base θ_3 is calculated as follows. Assuming 45° spreading, the effective area in the alumina base can be approximated by the geometric mean
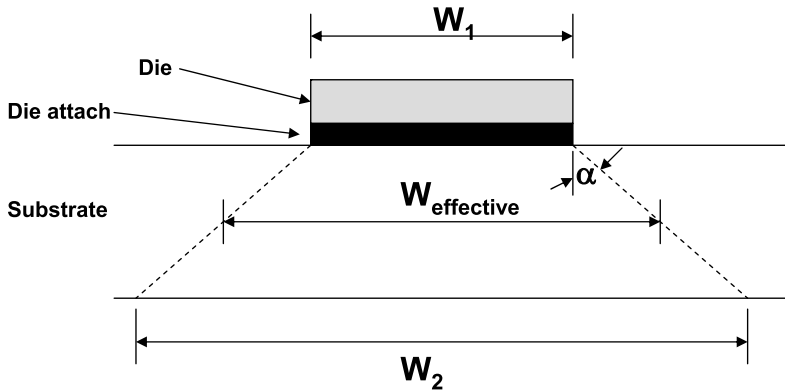
FIGURE 3.10
Dimensions for effective spreading area.

of the top area (0.35 × 0.35 in.) and the bottom area after spreading (0.43 × 0.43 in.). For a square heat source as shown in Figure 3.10, the effective area is calculated as follows.

$$A_{die} = W_1^2$$

$$A_{base} = W_2^2$$

$$A_{effective} = \sqrt{A_{die}\ A_{base}} = \sqrt{0.35^2 \times 0.43^2} = 0.387\ in^2 =$$

$$= (9.71 \times 10^{-5}\ m^2) = 9.71 \times 10^{-5}\ m^2$$

$$\theta_3 = \frac{t_3}{K_3 A_3} = \frac{1.02 \times 10^{-3}\ m}{(17\ W/m-K)(9.71 \times 10^{-5}\ m)^2} = 0.618°C/W.$$

The total thermal resistance from junction to case bottom is the sum of the three individual thermal resistances.

$$\theta_{Total} = \theta_1 + \theta_2 + \theta_3 = 0.048 + 0.215 + 0.618 = 0.881°C/W.$$

The temperature rise of the junctions from the case bottom is calculated using a rearranged Equation 3.23:

$$\theta = \frac{\Delta T}{Q_k}$$

$$\Delta T = \theta \times Q_K = 0.881 \times 10\ W = 8.8°C.$$

The 8.8° temperature rise needs to be compared with the design requirements. If acceptable, then a complete thermal analysis is performed. If the calculated temperature rise was too high, the designer would have several options. The first would be to lower the thermal resistance of the largest contributor (the base θ_3) by changing to a higher thermal conductivity ceramic such as aluminum nitride or beryllium oxide, or decreasing the thickness. Another technique to lower the base thermal resistance would be the addition of a heat spreader. An alternative to this would be replacing the ceramic base with a copper–tungsten base. A lesser improvement can be made in the θ_{Total} by decreasing the thermal resistance of the die-attach adhesive by using either eutectic attach or silver glass attach.

Assume that the base of the package in the above example is fixed at 30°C. The temperature at the die junction is calculated as follows:

$$T_{Die} = T_{Case} + \Delta T \tag{3.39}$$

$$\Delta T = 8.8° \text{ (calculated earlier)}$$

$$T_{Die} = 30° + 8.8° = 38.8°C.$$

The temperature at the base of the die (on top of the die attach material) is calculated as follows:

$$T_{Die\ attach} = T_{Die} - \theta_1 \times P \tag{3.40}$$

$$T_{Die\ attach} = 38.8° - 0.048 \times 8.8 = 38.38°C.$$

The temperature on the top of the package base is calculated as follows:

$$T_{pkg\ top} = T_{Die}\ (\theta_1 + \theta_2) \times P \tag{3.41}$$

$$T_{pkg\ top} = 38.8° - (0.048 + 0.215) \times 10 = 38.8° - (0.263) \times 10 = 36.2°C.$$

The temperatures calculated at each interface are shown in Figure 3.9b.

3.3.2   Heat Sinks

Heat sinks are used to increase the surface area exposed to the air or other cooling gas. They are the final interface between the heat generating devices and the outside world. The most common type is the finned heat sink, which consists of a flat plate and a number of fins extending from the surface. The fins are formed in a number of ways: extrusion, casting, machining, molding, or by attachment with a thermally conductive material. In some applications, only a flat plate is used for the heat sink.

The most common materials used for a heat sink are aluminum and copper. Both are low cost and easy to extrude and machine. With high CTEs (23.1 and 16.8 ppm/°C, respectively) [21], aluminum and copper heat sinks cannot be rigidly attached to low-CTE ceramic packages. If rigid attachment is required, composite materials, such as copper–tungsten and aluminum-silicon-carbide, with matching CTEs, may be used.

To calculate the amount of heat that can be removed with heat sink, one can use the natural and forced convection equations from the previous sections. Many physical designers, however, use graphical solutions instead of those based on curves available from the heat sink manufacturer. Figure 3.11b and Figure 3.11c show the temperature rises for a finned heat sink. Figure 3.11b shows the temperature rise (ΔT) vs. power dissipated with natural convection whereas Figure 3.11c shows the temperature rise (ΔT) vs.
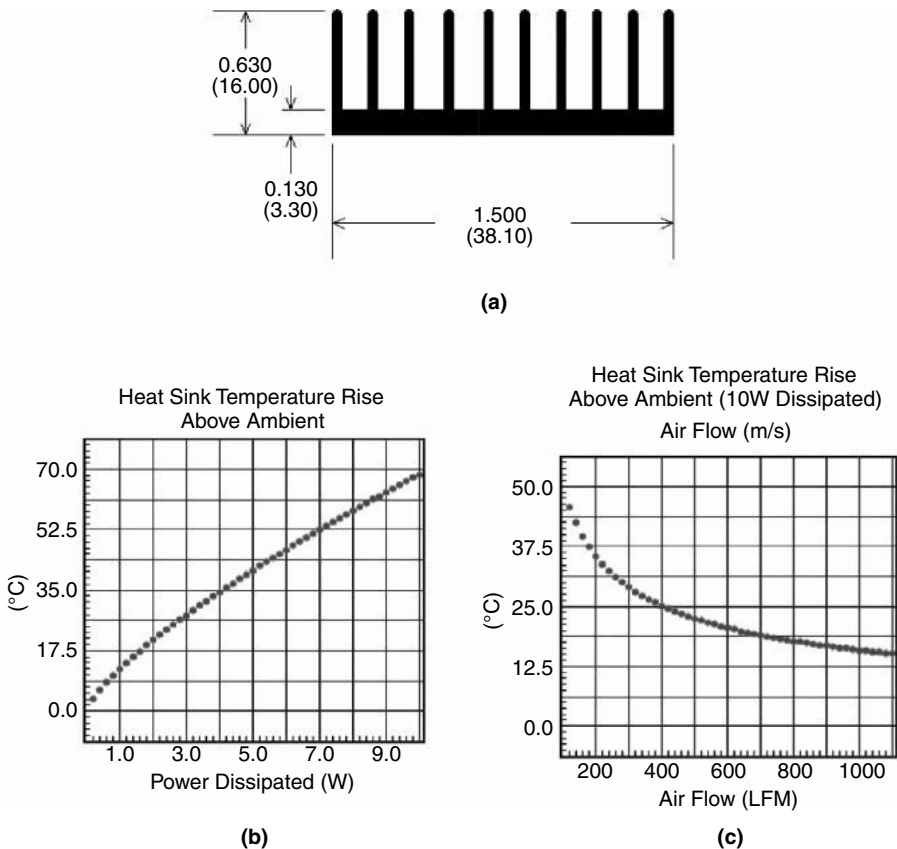
FIGURE 3.11
(a) Extrusion heat sink mechanical drawing. (From Aavid-Thermalloy, Product Data Sheet 63455, 2003. With permission.) (b) Natural convection for 2-in. length. (From Aavid-Thermalloy, Product Data Sheet 63455, 2003. With permission.) (c) Forced convection for 2-in. length. (From Aavid-Thermalloy, Product Data Sheet 63455, 2003. With permission.)

air velocity with forced convection. With the temperature rise and dissipation, a thermal resistance value for the heat sink-to-air can be calculated.

3.3.2.1 Natural Convection Example

The ceramic package described in Subsection 3.3.2 is mounted on the heat sink shown in Figure 3.11a and dissipates 10 W. From the curve in Figure 3.11b, the temperature rise (ΔT) for the 10-W dissipation is 66°C [23]. The thermal resistance of the heat sink is:

$$\theta = \frac{\Delta T}{P} = \frac{66}{10} = 6.6°C \, / \, W.$$

3.3.2.2 Forced Air Example

The ceramic package and heat sink described earlier with 200 lfm of air flow has a temperature rise of 35°C (Figure 3.11b). Increasing the air flow to 400 lfm lowers the temperature rise to 25°C. The thermal resistance of the heat sink with 200-lfm air flow is:

$$\theta = \frac{\Delta T}{P} = \frac{35}{10} = 3.5°C \, / \, W.$$

For 400-lfm air flow, the thermal resistance is reduced to 2.5°C/W.

3.3.3 Thermal Interface Materials

Air, which has a very poor thermal conductivity (0.026 W/m·K) [24] must be eliminated from the thermal path from the junction to the heat sink. All package bottoms, no matter what style material they are made from, are not perfectly flat or smooth. Accordingly, the portion of the heat sink that interfaces with the electronic package is not perfectly flat or smooth; when looking at the interface of the package and the heat sink on a microscopic level, one sees point-to-point contacts surrounded by air, as shown in Figure 3.12. This air impedes the heat flow. CCAs act as heat sinks to some extent and will be treated as such in this discussion. Reducing the effect of the air in the heat path lowers the thermal resistance and can be accomplished in several ways. Applying mechanical pressure works to some extent with soft metals. However, the amount of pressure required to obtain a good thermal interface may degrade the materials' strength and cause a fatigue failure.

One of the most accepted techniques in removing the gaps between a package and the heat sink is to fill them with a material having a thermal conductivity at least an order of magnitude higher than air. Materials used for this purpose include thermal grease, elastomeric pads, conductive adhesives, phase change materials, mica pads, adhesive tapes, and solders.
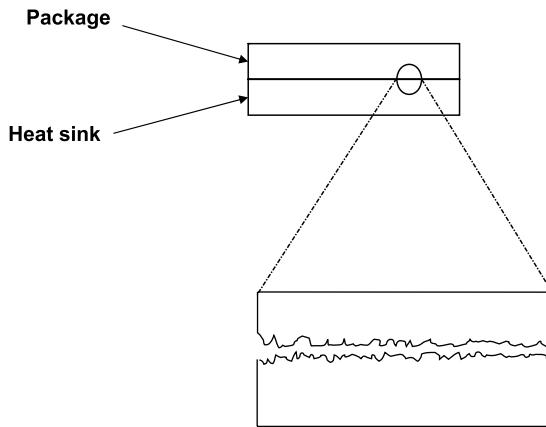
FIGURE 3.12
Microscopic view of heat sink-to-package interface.

3.3.3.1 Thermal Grease

Thermal grease uses a hydrocarbon oil or silicone as a base and is filled with a thermally conductive material such as aluminum oxide or zinc oxide. The typical thermal grease used in production applications has a thermal conductivity of approximately 1.0 W/m·K. The typical thickness is 0.001–0.003 in. Newer thermal greases have thermal conductivities as high as 16 W/m·K [15,24].

Thermal grease does not provide adhesion. Therefore, some form of mechanical attachment is necessary to apply sufficient pressure and minimize the thickness.

3.3.3.2 Elastomers

Elastomers are electrically insulating materials, usually in the form of silicone rubber pads, ranging in thickness from 0.001 to 0.20 in. and filled with high-thermal-conductivity materials such as alumina and boron nitride. They require a mechanical pressure to fill the voids. Figure 3.13 shows the variation of thermal impedance vs. pressure of an elastomeric pad for a TO-220 package [19].

For large spaces in the thermal path, a gap filler is used. This special type of elastomer ranges in thickness from 0.02 to over 0.20 in.

3.3.3.3 Thermally Conductive Adhesives

High-thermal-conductivity adhesives, either thermoplastics or thermosets, are used to attach packages to heat sinks and CCAs. Depending upon their application, they may be electrically insulating or electrically conductive. The adhesive serves two purposes — mechanical attachment and thermal
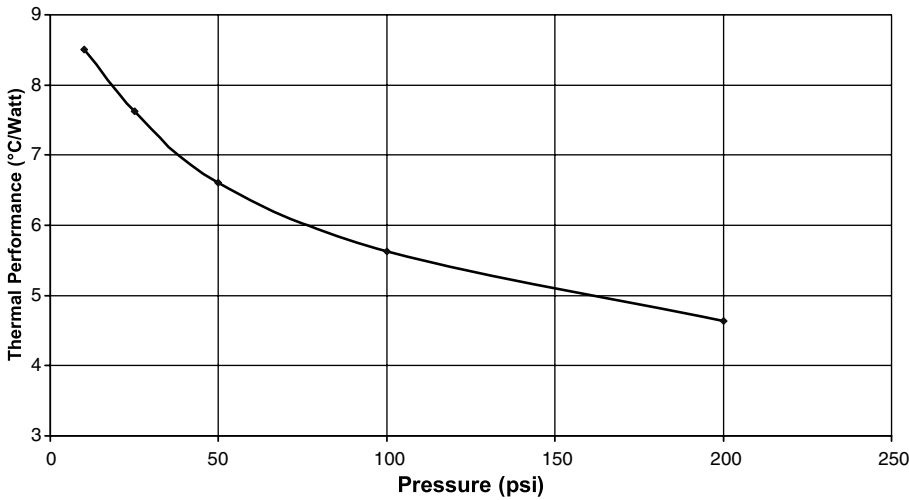
FIGURE 3.13
Thermal resistance vs. pressure for an elastomer pad.

interface. Available in both liquid and in preform, these adhesives have thermal conductivities ranging from 0.8 to 11.6 W/m·K.

3.3.3.4 Phase-Change Materials

Phase-change materials are either electrically insulating or conductive compounds that are coated onto carrier materials and then placed between the component or CCA. The materials are placed under pressure and subsequently heated externally or self-heated to the material's melting temperature, where it softens and fills all of the voids between the component and the heat sink. Figure 3.14 shows the relationship of device temperature vs. time when phase-change materials are used. When the part is turned on for the first time, the initial thermal resistance of the phase-change material is high because of the air in the thermal path. This allows the part to self-heat briefly to a higher-than-normal operating temperature, when the phase-change material alters from a solid to a flowable form and wets the interface between the component and the heat sink, and fills all of the voids. After wetting, the part returns to normal operating temperature, and the phase-change material returns to a solid state.

3.3.3.5 Mica

Mica insulators, having a thickness of 0.002–0.003 in., have been used for many years in mounting power devices to heat sinks. Used in conjunction with thermal grease, they provide a low-cost method of reducing the thermal resistance caused by air gaps. Mica has a thermal conductivity of 0.75 W/m·K [9].
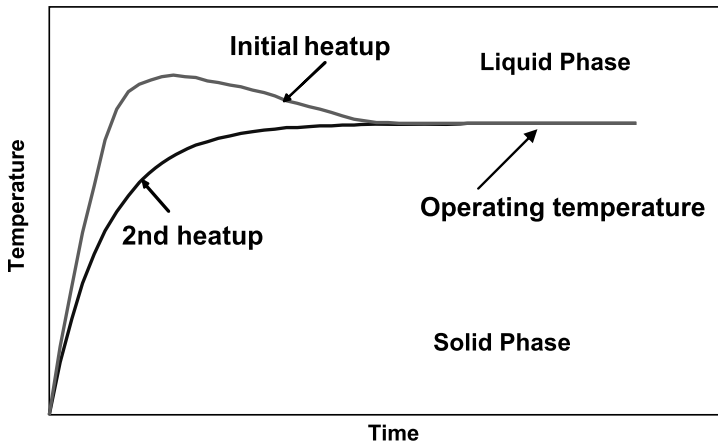
FIGURE 3.14
Phase change material thermal performance.

3.3.3.6   Adhesive Tapes

Thermally conductive adhesive tapes are double-sided, pressure-sensitive adhesive films filled with ceramic powder. The adhesive is typically supported either with a carrier made from polyimide film or with aluminum foil to provide ease of handling and strength. If electrical isolation is required, polyimide is the carrier used. Acting in a fashion similar to elastomeric films, they require some initial mating pressure to conform to the surface irregularities. If the gap between the surfaces is too large, the adhesive tape is unable to fill it. Once a joint is formed with an adhesive tape, mechanical pressure is no longer required to maintain the mechanical or thermal performance of the joint [24].

3.3.3.7   Solder

Solder can be used in two ways to fill the gap between the component and the CCA. In the first, the component base is reflowed to the CCA. This requires that the component have a solderable base. A second method is to use a solder preform in the same manner as an elastomeric pad. Lead–tin solder with a thermal conductivity of 50 W/m·K is typically used.

3.3.4   Air Cooling

Two types of air cooling — natural and forced convection — were presented in Subsection 3.2.3. In low-heat-flux applications, natural convection cooling is the choice of physical designers. It is low in cost, easy to implement, and reliable. When the heat load is high, forced convection is the most effective cooling method. To produce the air motion, either a fan or blower is used.

A fan moves the air parallel to the fan blades while a blower delivers air normal to the blower axis.

The performance characteristics of fans — speed, pressure, flow, density, and power — have been quantified in a series of equations called the *fan laws.* The reader is directed to the references for the details [14,25].

Fans have drawbacks. Besides creating significant acoustic noise in a system, they also create unwanted vibration.

3.3.5 Liquid Cooling

When the heat flux of a component or subsystem exceeds 30 W/cm², standard conduction and convection cooling techniques are not sufficient. To handle these high-heat loads, special techniques are required to maintain junction temperatures within specifications. One such technique is liquid cooling where a liquid is circulated through a heat sink that is in intimate contact with the dissipating elements. The circulating liquid carries away the heat by conduction. Fluids used for liquid cooling include water, fluorocarbons, and liquid carbon dioxide and nitrogen.

3.3.5.1 *Cold Plate*

The liquid-cooled cold plate is a closed system where coolants are continuously pumped through a high thermal conductivity block, usually metal, in intimate contact with a CCA or a component. Attached (or imbedded) in the block are tubes for circulating the coolant. Heat flows from the dissipating elements via conduction into the block where it is taken away by the circulating liquid. The liquid then dumps the heat into the ambient air at a heat exchanger, into facilities cooling water via a liquid-to-liquid heat exchanger, or at a liquid-cooled recirculating chiller.

A typical cold plate consists of a flat metal plate, usually aluminum, with a series of channels holding serpentine metal tubing through which the coolant flows. The tubing is either copper or stainless steel.

Cold plate performance is normally expressed as thermal resistance. Manufacturers provide curves of flow rate vs. thermal resistance for various models of cold plates [26].

3.3.5.2 *Immersion Cooling*

In immersion cooling, the high-heat-flux component or subsystem is totally immersed in a dielectric fluid such as Freon® (a registered trademark of E.I. duPont de Nemours & Co.) or a fluorocarbon. The main requirements of the fluid are chemical compatibility with the electronics and heat transfer characteristics.

The dielectric fluid needs to be circulated and moved to a heat exchanger for this cooling technique to be effective. It is advantageous to have as high a flow of the fluid as possible so that the convective heat transfer is maximized.

A key advantage of this cooling technique for high-heat fluxes is that there are no intervening thermal resistances in the cooling path [27].

3.3.6 Advanced Cooling Techniques

When the conventional cooling techniques discussed in the previous sections cannot be used, then the physical designer may want to use some advanced techniques. These include thermoelectric, jet impingement, heat pipes, and microchannel cooling.

3.3.6.1 Thermoelectric Cooling

Thermoelectric coolers (TEC) are solid-state heat pumps based upon the Peltier effect without any fluids or moving mechanical parts. In the Peltier effect, a potential is applied to two junctions as shown in Figure 3.15. Heat will be expelled from one junction and absorbed into the other in an amount proportional to the applied current. The thermoelectric cooler consists of an array of junctions using bismuth telluride (Bi_2Te_3), lead telluride (PbTe), or silicon germanium (SiGe). These materials are doped during fabrication to optimize the parameters of the cooler. Bismuth telluride has been found to have the best performance and is widely used for thermoelectric coolers.

A p-n combination is referred to as a *couple.* To fabricate the TEC, a number of couples, up to 100, are placed in series, electrically, and in parallel, thermally, between two metallized ceramic plates as shown in Figure 3.16. The completed assembly acts as a heat pump. When the junctions are biased on, one side (the cold junction) removes heat from the heat source whereas the other side (the hot junction) increases in temperature. Typically, a heat sink is placed on the hot junction side to transport the heat to ambient.
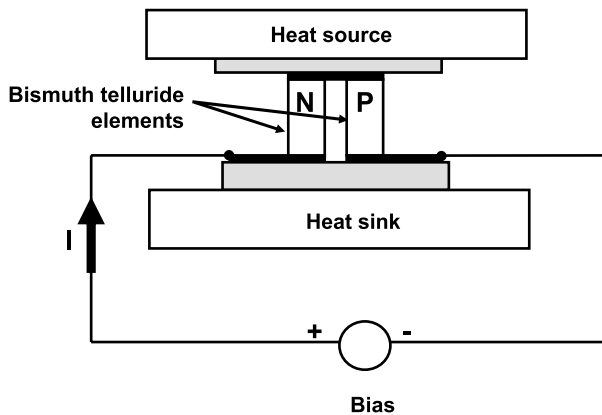
FIGURE 3.15
Thermoelectric cooler with one element.
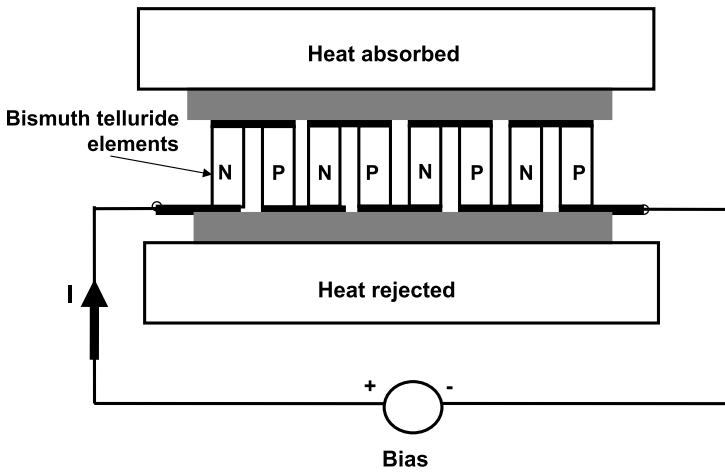
FIGURE 3.16
Thermoelectric cooler assembly with three elements.

TECs are usually integrated with thermocouples and temperature controllers to form a closed-loop system in which a fixed temperature is maintained on one side of the assembly. In designing a TEC system, there are three key parameters: hot-side temperature, desired cold-side temperature, and the total heat load to be pumped over the differential temperature. If a single TEC stage cannot meet the desired temperature differential, then additional stages must be cascaded [28].

3.3.6.2 Jet Impingement Cooling

In jet impingement cooling, a coolant under pressure is passed through a capillary tube, or jet, aimed at the surface of the component to be cooled. The coolant, a dielectric material or air, strikes the surface of the component and absorbs its heat dissipation.

Jet impingement cooling can operate in two modes: single-phase or two-phase cooling. In the single-phase mode, small jets of air are blown onto the dissipating element. In the two-phase mode, a dielectric liquid is passed through one or more jets onto the dissipating element. The latent heat associated with the phase change of the liquid is used to obtain higher heat transfer.

In both the single-phase and two-phase jet impingement modes, localized cooling of individual components can be achieved using one jet. For cooling larger areas, arrays of jets can be used.

Jet impingement cooling has been used effectively with heat densities up to 90 W/cm^2 [29–31].
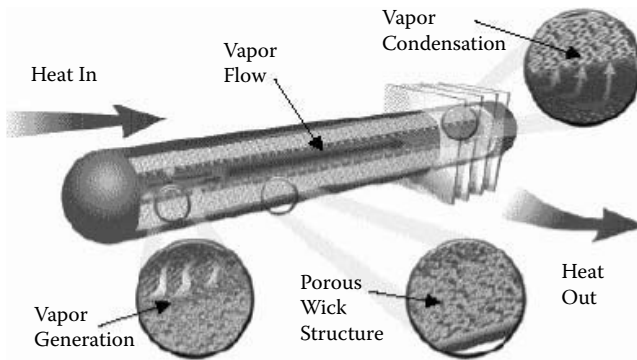
FIGURE 3.17
Heat-pipe cross section. (From Thermacore, Thermacore Product Literature, http://www.ther-macore.com, accessed September 26, 2003. With permission.)

3.3.6.3 Heat Pipe Cooling

A heat pipe is a passive device used for transferring heat from one area to another. In its typical application, the heat pipe transfers heat from a dissipating component to a CCA or a module housing. First used in space cooling, the heat pipe has recently found applications in commercial electronics. Some notebook computer manufacturers use heat pipes to transfer heat from the CPU to the keyboard.

An example of a heat pipe's construction is shown in Figure 3.17 [28]. It can be round or rectangular in shape. After the interior atmosphere has been evacuated, a working fluid is placed inside the heat pipe. This fluid can be water, ammonia, acetone, methanol, Dow-A, Dow-E, Freon-11™, or Freon-113® (a registered trademark of E.I. duPont de Nemours & Co.). The heat pipe vessel must be compatible with the fluid. Vessel materials used include copper, stainless steel, aluminum, nickel, and refrasil. The wick can be made from felt, a fine-screen mesh material, sintered material, or just grooves in the wall of the heat-pipe vessel.

Heat enters the evaporator end of the heat pipe via conduction to the vessel and to the fluid-filled wick. The liquid in the wick changes into its liquid phase. Inside the heat pipe, there is a small pressure differential between the evaporator end and the condenser end, caused by the small temperature differential. The pressure differential causes the vapor to flow toward the condenser area where it condenses within the wick and releases heat. The released heat is conducted through the heat-pipe walls to the ultimate heat sink. The condensed liquid in the wick flows back to the evaporator area via capillary action.

Low-cost heat pipes do not have wicks and rely on gravity for operation and must be oriented with the condenser on top and the evaporator on the bottom.

Heat pipes have two key parameters — maximum power and an effective thermal resistance. The latter parameter is sometimes expressed as an overall temperature difference (ΔT). Based on their construction, heat pipes also have a maximum-temperature limit. For some heat pipes, the thermal resistance data are given for both vertical and horizontal mounting.

Heat pipes can be used to cool individual components or groups of components. They can also be embedded into CCAs.

Because heat pipes are two-phase heat-transferring devices that do not have constant thermal conductivities like solid materials, an equivalent thermal conductivity parameter is used. This effective conductivity is a function of the heat-pipe length, the temperature difference over its ends, its cross-sectional area, and the amount of heat transported. Typical values of heat-pipe effective thermal conductivities range from 10,000 to 100,000 W/m·K [32].

3.3.6.4   *Microchannel Cooling*

In microchannel cooling, very small fins or channels are placed extremely close to the heat-dissipating element. At present, there are no standards for defining microchannel size. For the purposes of this chapter, microchannel cooling will be defined as fins with dimensions less than 0.005 in. The fins can be in the dissipating device or in a separate heat exchanger. Closed-loop cooling is accomplished by forcing either a liquid or gas over the extremely small fins to carry away the heat.

Fins in the silicon are fabricated in a variety of ways. Argonne National Laboratory uses electrical discharge machining (EDM). MESA+ Research Institute, University of Twente, The Netherlands, uses a KOH etch of the silicon to form the channels [33]. Others use an anisotropical etch of KOH [34,35].

The amount of heat removed is a function of the fin design, the fluid used, the fluid temperature, and the fluid velocity. Air-cooled microchannels can easily remove heat fluxes of 30 W/cm^2, whereas water-cooled microchannels can remove 100 W/cm^2 [36].

Figure 3.18 shows the cross section of microchannels fabricated in silicon. The channels were fabricated by etching two wafers and then bonding them together [35].

3.4   Techniques for lowering thermal resistance

As described in Equation 3.22, the thermal resistance θ can be minimized by using materials with the highest thermal conductivity k, the largest cross-sectional area A, and the thinnest thickness t. For example, a package base fabricated from Kovar® (a registered trademark of Carpenter Technology) has a thermal conductivity of 16.5 W/m·K. Changing the base to copper
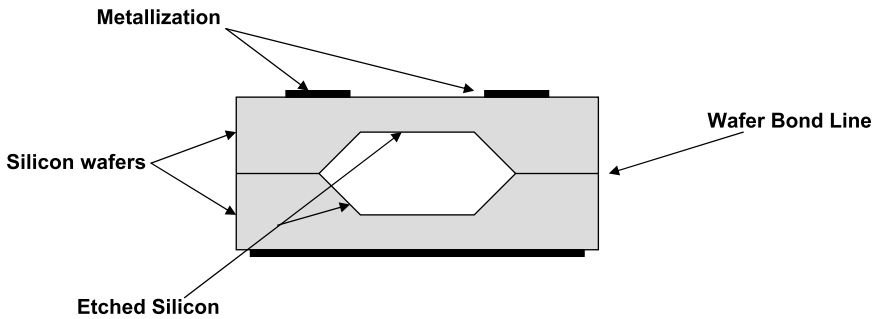
FIGURE 3.18
Microchannel-cooling cross section.

with a thermal conductivity of 401 W/m·K provides a significant decrease in thermal resistance. If a power FET had dimensions of 0.15 × 0.15 in. and was replaced by a device 0.25 × 0.25 in., then the 277% area increase would provide a corresponding decrease in thermal resistance. From an electrical standpoint, the increase in chip size on a power FET usually increases the input capacitance and may cause electrical problems. The thicknesses of the various layers in the thermal path need to be minimized to reduce the thermal resistance. For example, the thermal resistance in a 0.040 in. thick ceramic package base can be reduced by decreasing its thickness. The limit on thickness is fixed by the structural integrity of the package. Once the basic physical parameters of area, thickness, and thermal conductivity have been optimized for minimum thermal resistance and additional reductions are required, then the physical designer must use other techniques. These thermal resistance-reducing techniques include thermal vias, die cavities, heat spreaders, and wafer thinning.

3.4.1   Thermal Vias

Multilayer thick-film substrates use screen-printed glass as the dielectric material. The glass is both an electrical insulator as well as a thermal insulator. Typical values of the thermal conductivity for thick-film glass are 3 W/m·K. To improve the effective thermal conductivity of the dielectric material, the physical designer must make use of thermal vias. These vias, as shown in Figure 3.19, are a series of filled vias stacked on each other in an array. The bottom of the stack is attached either to a plane or to the ceramic substrate. The via-fill material is a thick-film conductor material, formulated with a permanent binder for a CTE match with the dielectric, and for good adhesion to the ceramic and the dielectric. The properties of the fired via-fill material are no longer that of a pure metal. Thick-film gold via fill has a measured thermal conductivity of 20.1 W/m·K [37].

In designing thermal vias in thick films, there are two key parameters — via diameter and via pitch. The via diameter is determined by the filling
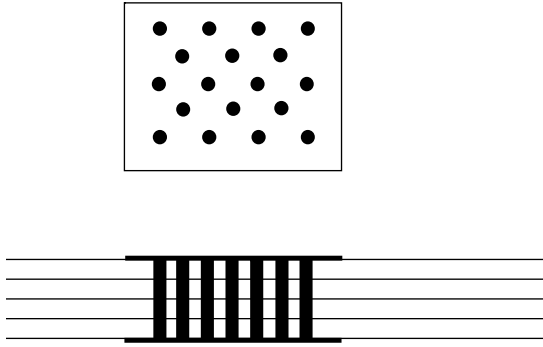
FIGURE 3.19
Thermal-via array.

process. Too large a diameter requires more than one screen-printing for filling. This is purely an economic factor. From a thermal standpoint, maximum thermal conductivity occurs when the pitch or spacing is the highest. Because via-fill materials are designed to match the CTE of the dielectric, placing too many vias per unit area increases the effective CTE and puts the dielectric material into stress, which can lead to cracking. In addition to the potential cracking, too high a via density will also restrict circuit routing [38].

Thermal vias in low-temperature cofired ceramic (LTCC) are fabricated in the same manner with the same constraints as in multilayer thick films. The only difference is the formulation of the via-fill material.

High-temperature cofired ceramic (HTCC) packages make use of thermal vias in the same manner as in multilayer thick-film substrates. The via-fill material used in HTCC packages is a refractory material such as tungsten or moly-manganese.

Whenever thermal vias are used, the physical designer needs to take into account the electrical connection of the chip. If the backside of the chip needs to be isolated, then the via array must end in an insulator (dielectric or bare ceramic). In LTCC or in HTCC, electrically isolating the chip requires additional layers of ceramic.

One method used to improve the thermal conductivity of thin film, metallized alumina substrates is to place filled thermal vias under the high-dissipating devices. In this process, holes are drilled into the alumina, filled with copper–tungsten, fired, and lapped flat [39].

3.4.2 Die Cavities

The number of layers of tape in LTCC substrates can range from as few as 5 to over 50. Depending upon the tape manufacturer and tape type, the thermal conductivity of LTCC ranges from 2.0 to 4.4 W/m·K. To minimize the thermal resistance under a chip in an LTCC design with a high layer count, the physical designer can place the high-dissipating component in a
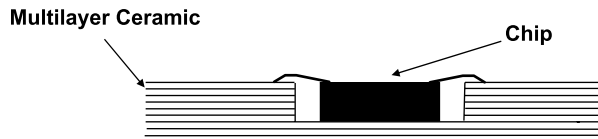
FIGURE 3.20
Die cavity with electrically isolated base.

cavity as shown in Figure 3.20. In this figure, the bottom of the die is electrically isolated from the back of the substrate with at least two layers of tape. The actual number of layers of tape under the cavity is a function of the area of the cavity and the strength of the LTCC. For small devices (i.e., less than 0.1 in.²), there can be only one or two layers of tape. For large devices, such as complex ASICS, there must be at least five layers of tape. If electrical isolation is not required for the backside of the chip and additional thermal improvements are needed, then thermal vias can be used in conjunction with the die cavity.

3.4.3   Heat Spreaders

A method to increase the effective area between a small heat source and the heat sink is to use the principle of heat spreaders as described in Section 3.2.2.3. The heat spreader is fabricated from a high thermal conductivity material with a TCE match to the adjacent materials. Typical materials used for heat spreaders include copper, molybdenum, copper–tungsten, copper–molybdenum, CVD diamond, aluminum nitride, and beryllium oxide. Copper, when used as a heat spreader, may be free standing, plated, or direct bonded. CVD diamond can be either free standing or deposited. The heat spreader can be used both inside and outside the package. When used inside the package, the semiconductor is mounted on a heat spreader as shown in Figure 3.21. Heat spreaders can also be mounted on the base of a ceramic package as shown in Figure 3.22. In very-high-power-density applications,
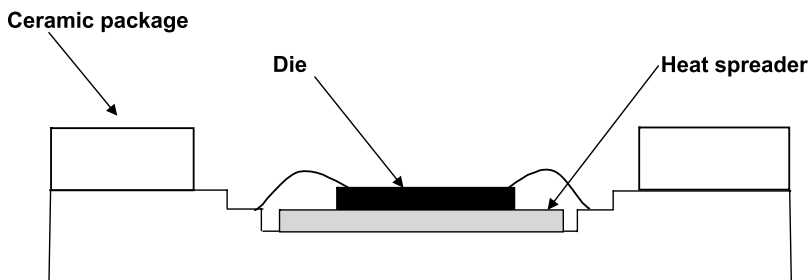
FIGURE 3.21
Heat spreader inside package.
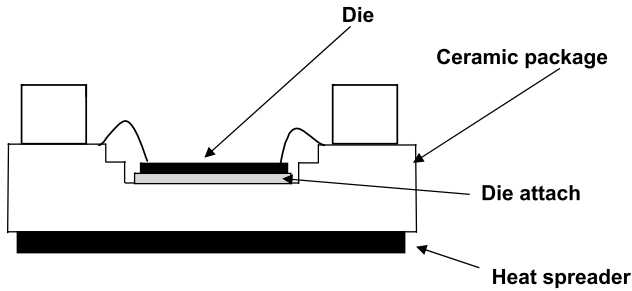
FIGURE 3.22
Heat spreader on outside of package.
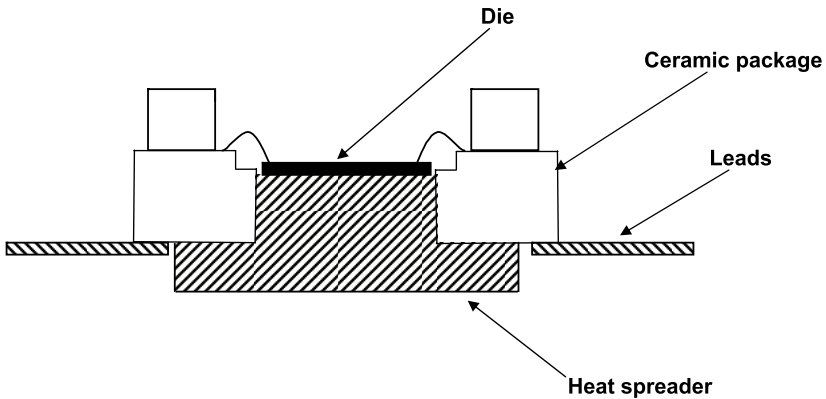
FIGURE 3.23
Heat spreader as base of ceramic package.

the base of the hermetic ceramic package can be fabricated from a heat-spreader material as shown in Figure 3.23.

Heat spreaders, when free standing, need to be attached to both the dissipating element and the next level. The material used for attachment is usually a trade-off between thermal conductivity and elasticity. Rigid attachment materials, such as gold–tin and gold–germanium solders, have high thermal conductivities, 57 and 44 W/m·K, respectively. Compliant materials, such as conductive epoxy, have significantly lower thermal conductivities (1.6–6.0 W/m·K).

3.4.4 Thinner Chips

On high-power-density chips, such as gallium arsenide, it is a common practice to reduce the thermal resistance by thinning the wafer via chemical and mechanical means from 0.015 in. to as thin as 0.002 in. If a chip thickness

were 0.015 in. and the chip lapped (at the wafer level) to 0.004 in., the decrease in the term *L* (in Equation 3.22) would reduce the thermal resistance by approximately 73%.

3.5 Mechanical Design Considerations

3.5.1 Thermal and Mechanical Stress

Most materials, with a few exceptions, expand when heated and contract when cooled. The *temperature coefficient of expansion* (TCE) is a parameter found in the literature for each material. It is also called the *coefficient of thermal expansion* (CTE). Table 3.3 lists the various mechanical properties of packaging materials including their CTEs. The thermal expansion of most materials is linear with temperature.

TABLE 3.3

Thermomechanical Properties of Materials

Material	CTE (ppm/°C)	Thermal Conductivity @25°C (W/m·K)	Modulus of Elasticity (GPa)
Ceramics			
Alumina 92%	7.2	17	280
Alumina 96%	6.3	21	303
Alumina 99.9%	7.4	30	370
Aluminum nitride	4.2	170	350
Beryllium oxide	6.4	248	345
LTCC	4.5–8.0	2.0–4.4	152
Metals			
Aluminum	23.6	237	68
AlSiC (37% SiC)	10.9	170	167
AlSiC (55% SiC)	10.16	181.4	167
AlSiC (63% SiC)	8.37	180	188
Kovar®*	5.5	16.5	137.9
Copper–tungsten 80:20	8.3	185	
Copper–tungsten 85:15	7.2	180	274
Copper–tungsten 90:10	6.5	170	306
OFHC copper	16.8	401	117
Dispersion-strengthened copper	16.6	365	
Molybdenum	5.35	138	330
Cu–Mo–Cu (1:6:1) clad	6.4	233	
CuMo (15 Cu, 85 Mo)	6.7	160	239
Cu–Invar–Cu (1:3:1) clad	6.5	174 x and y 24.8 z	
Silva®*	6.6–7.0	110–153	110
Aluminum–graphite	7.5	190	
Aluminum–silicon	7–23	120–180	45

TABLE 3.3 (CONTINUED)

Thermomechanical Properties of Materials

Material	CTE (ppm/°C)	Thermal Conductivity @25°C (W/m·K)	Modulus of Elasticity (GPa)
Adhesives	(below T$_g$)		
Nonconductive epoxy	50–170	0.7–1.8	1.0–4.6
Conductive epoxy	40–110	1.6–6.5	1.4–6.1
Silver glass	16–21	60–80	11.5–15.1
Solder			
Sn10	27.9	36	0.030
Sn63	25	51	0.050
Sn96	30.2	33	0.039
AuSn	15.9	57	0.276
AuGe	13.4	44	0.204
Circuit cards	(below T$_g$)		
FR-4	15–20 x and y	0.8 x and y, 0.3 z	
	50–70 z		
Polyimide	23–56	0.11	
Benzocyclobutene (BCB)	45–70	0.19	
Gases			
Air	na	0.0024	na
Nitrogen	na	0.0024	na
Semiconductors			
Silicon	2.49	150	112.4
Silicon carbide	4.5	155	450
Gallium arsenide	5.4	45	85.9
Indium phosphide	4.6	97	

Sources: From Williams Advanced Materials, Packaging Materials-Solder Alloys, 2002; NTK Technical Ceramics, *Ceramic Package Design Guide*, Komaki, Aichi, Japan, 2001, p. 4; Polese Company, Silvar-K®* Heat Sink Product Literature, http://www.polese.com/thermal.html, accessed September 26, 2003; Brush Wellman, Inc., BeO Dry Pressed Ceramics As-Fired or Machined CDDP-10 Rev. F; Brush Wellman, Inc., BeO Isopressed Ceramics CDI-20, Rev E; E.I. du Pont de Nemours and Company, DuPont Green Tape™* Design and Layout Guideline; Ceramics Process Systems Corp., AlSiC Material Properties; Osprey Metals Ltd., Osprey Controlled Expansion Alloys; Morgan Advanced Ceramics, Thermal Properties of Silicon Carbide; Ioffe Physico-Technical Institute, GaAs — Gallium Arsenide, http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaAs/, accessed September 26, 2003; Loctite, Loctite Product Literature, http://www.loctite.com/int_henkel/loctite/entry.cfm, accessed September 26, 2003. *Kovar® is a registered trademark of Carpenter Technology. Green Tape™ is a trademark of E.I. duPont de Nemours & Co. Silvar® is a registered trademark of Engineered Materials Solutions, Inc.

When dissimilar materials are joined and subsequently heated, the differential expansion introduces stresses and strains in the materials and joints. Examples of material pairs that may see differential expansions are: semiconductors to substrates, semiconductors to packages, leadless packages to circuit cards, flip chips to substrates, substrates to packages, and packages to heat sinks. If the differential expansion is not accommodated, then a fracture will occur in one or more of the materials.
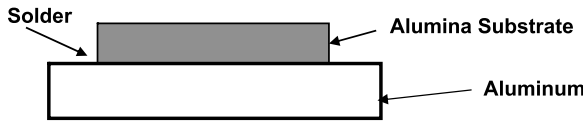
FIGURE 3.24
Alumina substrate bonded to an aluminum block.

When two materials are bonded with a high-temperature material, such as a solder or a braze, the material structure has zero stress when the bonding material is in the molten state. When the structure is cooled, the bonding material solidifies and stress is produced by the mismatch in coefficients of thermal expansion among the materials being bonded and the bonding material.

An example of thermal stress due to CTE mismatch is an aluminum plate soldered to a 96% alumina substrate as shown in Figure 3.24. The alumina has a CTE of 6.3 ppm/°C whereas the aluminum has a CTE of 23.6 ppm/ °C. When this assembly is temperature cycled through a number of periods of heating and cooling, the aluminum expands and contracts at a higher rate than the alumina but is constrained by the solder. This constraint could result, after repeated temperature cycles and time, in the aluminum plate bending, the solder joint failing, the ceramic warping, or the ceramic cracking. To reduce or eliminate the differential expansion and subsequent stresses requires either changing the materials or reducing the temperature range during temperature cycling (or operation) [14].

The change in length of a material when subjected to a change in temperature is calculated from the formula:

$$\delta = L_0 \, \alpha \, \Delta T \tag{3.42}$$

where
δ = change in length
L_0 = initial length
α = CTE in ppm/°C
ΔT = change in temperature in degree Celsius

For a 1-in.-long strip of copper heated from 25 to 125°C, the change in length (ΔL) is:

$$\Delta L = L_0 \, \alpha \, \Delta T = 1.0 \times 16.8 \times 10^{-6} \times (125 - 25) = 1.68 \times 10^{-3} \text{ in.}$$

The elongation of the material due to temperature develops a stress (σ) as given by Hooke's Law:

$$\sigma = \varepsilon \times E \tag{3.43}$$

where
 E = elastic modulus (also called modulus of elasticity or Young's modulus)
 ε = the strain

The volume of a solid remains constant when placed under stress. Therefore, there is a tangential displacement when a force is applied in the normal direction. *Poisson's ratio* is the ratio of the tangential force to the normal force.

$$\upsilon = \frac{\varepsilon_T}{\varepsilon_N}. \tag{3.44}$$

For elastic strains, Poisson's ratio is constant for a given material and can be used to determine the strain in the other directions.
The *shear modulus (G)* is defined as:

$$G = \frac{\varepsilon}{2(1+\upsilon)}. \tag{3.45}$$

One particular configuration of interest is the component, such as a semiconductor die, mounted flat on a ceramic substrate with an adhesive. In most cases, the TCE of the die is lower than that of the substrate, which results in a tensile stress in the die when the assembly is temperature cycled. In calculating the differential expansion of two bonded materials, the dimension used for the worst-case expansion is the longest, the diagonal. The strain is given by:

$$\varepsilon = (\alpha_{\text{Die}} - \alpha_{\text{sub}}) \, \Delta T \tag{3.46}$$

where
 α_{die} = TCE of die
 α_{sub} = TCE of substrate
 $\Delta T = T_{\text{equilibrium}} - T_{\text{ambient}}$

The maximum stress occurs at the corners of the die and can be calculated from:

$$\sigma = \frac{(\alpha_{die} - \alpha_{sub}) \, x \, \Delta T \, x \, L \, x \, G \, x \, \tanh(\beta)}{\beta \, x \, t_b} \tag{3.47}$$

where
 L = length of diagonal
 G = shear modulus

$$\beta = \sqrt{\frac{G}{t_s}\left(\frac{1}{E_d t_d} + \frac{1}{E_s t_s}\right)}$$ (3.48)

E_d = Young's modulus of die
E_s = Young's modulus of substrate
t_d = die thickness
t_s = substrate thickness

The critical force (σ_{crit}) can be defined as

$$\sigma_{crit} = Z\frac{\varepsilon}{\sqrt{\pi a}}$$ (3.49)

where
 Z = dimensionless constant, typically 1.2
 ε = plain strain fracture toughness in MPa·m$^{1/2}$
 a = length of crack in meters

The fracture toughness for various packaging materials is given in Table 3.4.

TABLE 3.4

Fracture Toughness of Selected Materials

Material	Fracture Toughness MPa·m$^{1/2}$
Alumina 90%	3–4
Alumina 96%	4.5
Alumina 99.9%	4.0
Aluminum nitride	3.4
Beryllium oxide	3.4
Silicon	0.8

Sources: From Krum, A. and Sergent, J.E., *Thermal Management Handbook for Electronic Assemblies*, McGraw-Hill, New York, 1998; MatWeb: The Online Materials Information Resource, www.matweb.com, accessed September 26, 2003; TechnicalCeramics.net, Material Properties, http://www.mcelwee.net/html/material_properties.html, M.M.C., accessed September 26, 2003; Brush Wellman Inc., Internal data on beryllium oxide toughness.

3.5.1.1 Stress Example

A CMOS ASIC dissipating 10 W is mounted on an aluminum plate 0.050 in. thick with Sn96 solder. The die size is $0.50 \times 0.50 \times 0.025$ in. The solder bond thickness is 0.002 in. The shear modulus of the Sn96 solder is 2.89×10^6 psi or 20 GPa. Calculate the stress in the die when the temperature is cycled from 0 to 100°C.

Because the Sn96 solder has a eutectic at 221°C, that is the temperature equilibrium point. The worst-case temperature occurs during the temperature cycling at 0°C.

The stress in the die is calculated as follows:

$$\beta = \sqrt{\frac{G}{t_s}\left(\frac{1}{E_d t_d} + \frac{1}{E_s t_s}\right)} =$$

$$= \sqrt{\frac{2.89 \times 10^6}{0.050}\left(\frac{1}{16.3 \times 10^6 \times 0.025} + \frac{1}{9.86 \times 10^6 \times 0.050}\right)} = 16.09,$$

$$\sigma = \frac{(2.49 - 23.6)10^{-6}(221 - 0) \ (.50 \times 1.414) \times 2.89 \times 10^6 \times \tanh(16.09)}{16.09 \times 0.002} =$$

$$= 296,218 \ psi,$$

$$\sigma = \frac{(2.8 - 23.6)10^{-6}(221 - 0)(.50 \times 1.414) \times G \times \tanh(4.91)}{4.91 \times 0.002} = 95,675 \ psi.$$

The critical stress is calculated using Equation 3.49 where Ed and Es have been converted to psi from GPa, based on data in Table 3.3.

$$\sigma_{crit} = Z\frac{\varepsilon}{\sqrt{\pi a}} = 1.2\frac{0.8 \times 10^6}{\sqrt{\pi \times 1 \times 10^{-6}}} = 5.42 \times 10^8 \ Pa = 78,968 \ psi.$$

The maximum stress (σ) in the die is much greater than the critical stress (σ_{crit}). This indicates that the die is likely to crack.

Because the above analysis only looked at stress and strain in one dimension, it can be considered an oversimplification. For an exhaustive analysis, the reader should refer to Lau [50], and Krum and Sergent [14].

3.5.2 Thermomechanical Properties of Materials

Table 3.3 provides a listing of the thermomechanical properties of the various packaging materials used with ceramic interconnects.

3.6   Thermal and Mechanical Simulation Tools

The goal in performing a thermal simulation is to determine the temperature distribution within a medium with the given boundary conditions [6]. Once the simulated temperature distribution is obtained, it is compared to the proposed maximum device temperatures. If temperatures are too high, the thermal design must be iterated using alternative materials, construction and/or sizes. Once the temperature distribution is determined to be satisfactory, the physical design is completed, prototypes built, and temperature measurements made, using the techniques in Section 3.7.

Numerical methods to obtain the temperature distributions include finite element method (FEM), finite difference method (FDM), flow network modeling (FNM), and computational fluid dynamics (CFD). The FEM can also provide structural analysis.

There are a number of commercially available software packages that do thermal simulation using the various numerical methods listed earlier. They do simulations across the full gamut of electronic packaging, ranging from the single chip to the entire system. It is beyond the scope of this section to either recommend or evaluate the various software packages. The reader is directed to the various references in this section for additional information on each of the simulation tools [51–54]. An overview of the numerical methods used for the various simulation tools will be presented.

3.6.1   Finite Element Method

The FEM was first used in 1960 to solve elasticity problems. Its first application for heat transfer analysis was in 1965 by Zienkiewicx and Cheung [55].

In the FEM, the solution domain is broken down into a finite number of smaller regions called *elements*. These elements are connected at specific points called *nodes*. An important criterion of the FEM is that the solution must be continuous along common boundaries of adjacent elements. For thermal analysis, the governing heat equations are solved using standard numerical methods. For structural analysis, stress/strain equations are solved.

Most commercial FEM tools have preprocessing capabilities in which mechanical design data is ported to the FEM software. The creation of the elements and nodes can be done either automatically or manually. The completed analyses are then put through a postprocessor for data viewing and analysis. A simplified finite element thermal model and temperature map are shown in Figure 3.25. The typical temperature map generated by an FEA is color coded. (This figure has been converted to gray scale.)

The FEM is a widely used tool that is effective in performing the thermomechanical design of an electronic system. It is capable of simulating irregular and complex geometries where a closed-form solution is difficult to obtain. The FEM tool is capable of doing sensitivity analyses comprising
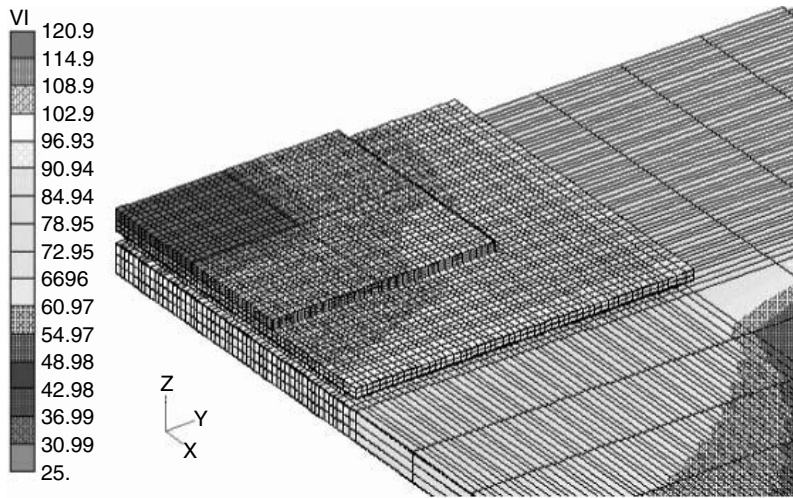
FIGURE 3.25
Finite element analysis model of ball grid array.

changes in dimensions, material properties, and loading characteristics [6,50,54].

3.6.2 Finite Difference Method

The FDM dates back to 1910, with initial work by Richardson and later by Liebman in 1918. In this method, finite differences replace the differential equations in the heat transfer equations. This method suffers from problems in handling irregular boundaries. To overcome these problems, the analyst typically increases the density of the grid points at the boundaries [6,55].

3.6.3 Flow Network Modeling

FNM is based on the overall behavior of different flow components. It is a methodology for calculating system-level distributions of temperatures and flow rates in a network representation of a cooling system. FNM uses overall characteristics of the various components in lieu of attempting to calculate a detailed distribution of velocity and temperature within the component.

In the FNM analysis, the flow network of an electronic cooling system is composed by graphically representing the paths followed by the flow streams as they pass through the different components of the system. No restrictions are placed on either the size of the network or on the interconnections of the components in the network. The system-wide flow and the temperature distributions are predicted from the flow and heat transfer characteristics of the components in the network model.

A typical FNM analysis is usually limited to calculating 50 to 100 quantities. This minimal amount of data (compared to other analysis tools) provides a one to two order-of-magnitude reduction in analysis time.

Data for standard components of FNM are available from handbooks whereas data for nonstandard components can be obtained from the supplier, through testing or through CFD analysis.

The results for the temperature and flow distributions can be subsequently examined after postprocessing in either graphical or numerical format [51].

3.6.4 Computational Fluid Dynamics

CFD software, introduced commercially in the 1970s, allows engineers to model their products through detailed simulation of fluid flow and heat transfer.

In a CFD analysis, a mesh is created over the entire electronic system for the solution of the Navier–Stokes and energy transport equations to obtain a prediction of the velocity, pressure, and temperature fields.

The computational fluid dynamics consists of three processes — preprocessing, solving, and postprocessing. In preprocessing, a model is constructed from scratch or imported from a CAD package. A mesh is applied and followed by the entering of the data. The solver does the calculations and produces the results. The postprocessing organizes and interprets the data and the images.

A CFD thermal analysis of an entire electronic system may involve solving for 500,000 or more grid points.

Although finite element and finite difference analyses are unable to model complex three-dimensional fluid flow accurately, CFD excels at it. However, CFD is not very efficient at combining the details of conduction modeling with fluid flow and radiation. This can be addressed by coupling the CFD analysis with thermal finite element and finite difference analysis [51].

3.7 Thermal and Mechanical Measurements

During the hardware validation of new designs, it is often advantageous to measure device temperatures or thermal resistances and compare them to the simulated values. If the measured temperatures are too hot or the thermal resistances too high, then either physical design changes or assembly process improvements are required. With sufficient margin between the measured temperatures and the reliability design limits, future measurements can either be performed on a sample basis or eliminated entirely.

The easiest method to measure the temperature of packages, circuit cards, and heat sinks is to mount fine-gauge thermocouples on them and take

readings. The measurement of the junction temperatures requires the use of alternative techniques that are described in subsequent sections. These techniques can measure the temperature or thermal resistance either directly or indirectly.

For many years, engineers validated their mechanical designs by running accelerated stress testing on their product. This type of testing usually consisted of a series of temperature cycles along with temperature shocks. If the product survived the testing, then the mechanical design was acceptable. To quantify the amount of stress and strain in a component, the engineer can use a variety of tests. They include piezoresistive stress sensors, Moiré interferometry, and silicon test chips.

3.7.1 Direct Thermal Measurement Techniques

Direct thermal techniques, which include fiber-optic thermometry, theta-JC testing, infrared thermal imaging, and liquid crystal microthermography, either give a direct temperature measurement or a thermal resistance.

3.7.1.1 Fiber-Optic Thermometry Probe

In the fiber-optic thermometry probe technique, a temperature sensor, consisting of a small amount of a temperature-sensitive material (manganese-activated magnesium fluorogermanate), is mounted on the end of a probe and is placed on the surface of the device under test (DUT). A filtered xenon flash lamp provides a blue-violet light to excite the phosphor on the probe to fluoresce. When excited by this wavelength of light, the phosphor in the sensor exhibits a deep red fluorescence.

After the excitation pulse is over, the intensity of the fluorescent radiation decays. Because the decay time is a function of temperature, a direct temperature measurement is available through the use of a time–temperature lookup table.

The fiber-optic thermometry probe technique can measure temperatures with accuracies of ±0.1°C. Using the smallest probe, this probing technique can measure temperatures of 0.001-in. spot sizes. After the DUT has reached thermal equilibrium, the system can make up to four measurements per second. To accurately measure junction temperature, the device must be unencapsulated and unsealed. The probe is placed on the junction.

3.7.1.2 Theta-JC Tester

Every active device has a temperature-dependent parameter that can be used with the theta-JC tester to directly measure thermal resistance. These parameters are listed in Table 3.5. A typical circuit for measuring the thermal resistance in a junction diode is shown in Figure 3.26. The diode is biased on with an idle current I_0, which sets a low power level P_0, in the device that results in a junction temperature of T_0. The power (P_0) in the idle state is [56]:

TABLE 3.5

Temperature-Dependent
Parameters

Active Device	Parameter
Diode	V_f
Bipolar transistor	V_{be}, V_{bc}
Junction FET	V_{gs}, R_{DS-ON}
Power FET	Bulk diode
IGBT	Saturation voltage
Integrated circuit	Substrate diode

Sources: From Krum, A., Course Notes,
UCLA Extension, Engineering 881.152,
Power Hybrids: Design and Processing,
April 3–6, 1995, Los Angeles, CA.
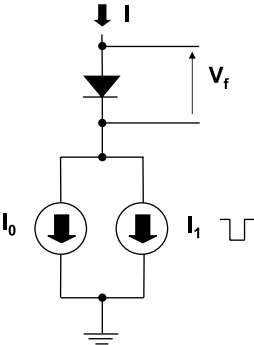
FIGURE 3.26
Thermal-resistance test circuit.

$$P_0 = I_0 \, V_F. \tag{3.50}$$

The DUT is then pulsed on with a significantly higher current I_1 for a short period of time, raising its temperature to T_1. During this current pulse, the power (P_1) in the DUT is:

$$P_1 = I_1 \, V_F. \tag{3.51}$$

The temperature of DUT is determined by measuring the temperature-dependent parameter, the diode forward drop (V_F). To minimize error, a four-point measurement is usually used. As shown in Figure 3.27, the temperature is inversely proportional to the forward drop (V_F).

For the junction diode, the temperature coefficient K of the forward drop V_F is:

$$-1.8 \le K \le -2.2 \text{ mV} / {}^\circ\text{C}. \tag{3.52}$$
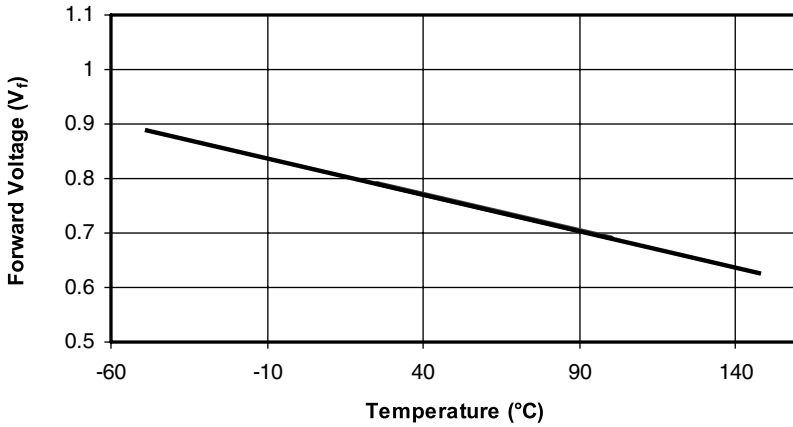
FIGURE 3.27
V_f vs. temperature of a junction diode.

The slope of the temperature vs. forward drop is the temperature coefficient of the junction and is negative. Therefore, the above equation may be rewritten as:

$$1.8 \leq k' \leq 2.2°C/mV \tag{3.53}$$

where

$$k' = \frac{1}{K}. \tag{3.54}$$

This temperature coefficient k will vary from device type to device type and from wafer lot to wafer lot. Therefore, to obtain accurate temperature measurements, each wafer lot must be calibrated by running a temperature vs. V_F curve as shown in Figure 3.27. However, for many applications, accurate measurements are not required to detect defects in assembly. A large amount of voiding will show up as an abrupt change from nominal in the thermal resistance measurement.

From the idle current measurement, the temperature T_0 value is calculated. From the pulsed current measurement, the T_1 value is then calculated. The difference in temperatures is:

$$\Delta T = T_1 - T_0. \tag{3.55}$$

Thermal resistance has been previously defined as:

$$\theta_{jc} = \frac{\Delta T}{P} \tag{3.56}$$

$$\theta_{jc} = \frac{T_1 - T_0}{P_1 - P_0} = \frac{k'(V_{be1} - V_{be0})}{P_1 - P_0}. \tag{3.57}$$

The theta-JC tester can only be used when electrical connections for the temperature-sensitive device are available. This method does not need to remove potting or a package lid to run the tests.

3.7.1.3 Infrared Thermal Imaging

Infrared (IR) thermal imaging is based upon the principle that hot bodies emit thermal radiation as electromagnetic waves that can be viewed after detection. Although radiation is not a primary method of removing heat from packages and substrates, it does provide an accurate means to measure temperature.

The rate of emission of radiant energy from the surface of a body is proportional to the temperature and the surface emissivity. Black bodies have high emissivities and are good radiators of IR radiation. Shiny metal surfaces tend to have low emissivities and are poor radiators. The differences in surface emissivities will give different surface-temperature readings for devices at the same temperature. Therefore, to obtain accurate readings, it is necessary to compensate for the differences in emissivities.

The output of an IR system is typically a colored image of the DUT. Each of the colors in the image corresponds to a different temperature.

IR measurements can be made on sealed or encapsulated devices as well as on open devices. For the sealed or encapsulated device, the IR image provides a case temperature, and the image of an open device gives the true junction temperatures. Spatial resolution as fine as 3 μm is available in commercial systems [57].

IR measurement provides an accurate, noncontact method for measuring device temperature. Depending upon base-temperature stabilization time, the test time can range from as fast as 1 to over 5 min.

3.7.1.4 Liquid Crystal Microthermography

The liquid crystal microthermography method of temperature measurement requires that the surface of the DUT be exposed. Therefore, this technique cannot be used on sealed or encapsulated devices without deprocessing.

Once the surface of the DUT is exposed, it is coated with a nematic liquid crystal that has a phase transition temperature of 110°C. The liquid crystal material is then viewed through a polarizing microscope where it is possible to distinguish the transition with a spatial resolution of approximately 2 μm. The DUT sits on a hot plate or equivalent heater monitored by a thermocouple or other temperature measuring device. The bias to the DUT is then increased until a phase transition is detected through the polarizing microscope. The power for the DUT is recorded for this transition. The measurement is then repeated for a series of different base temperatures. The
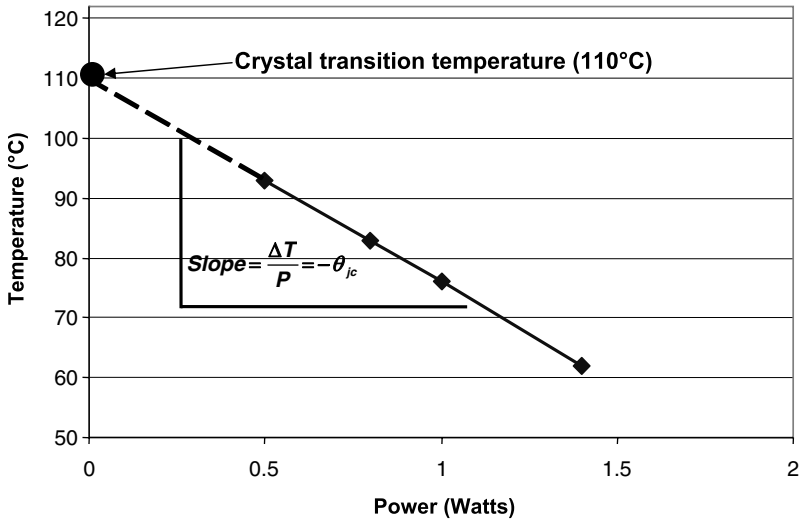
FIGURE 3.28
Phase transition temperature.

resulting phase transition temperatures are plotted against the DUT power dissipation, as shown in Figure 3.28 [56]. A trend line for the curve is then plotted. The slope of the trend line is the negative of the thermal resistance. The intercept of the trend line and zero power should be at the crystal transition temperature of 110°C.

Liquid crystal microthermography is an extremely accurate method for determining thermal resistance. Because it is a time-consuming method and requires devices to be unencapsulated and subsequently coated, it is not used in production.

3.7.2 Indirect Thermal Measurement Techniques

There are three indirect, nondestructive measurement techniques to determine thermal resistance: acoustic microimaging, x-ray, and thermal test chips. The acoustic microimaging and x-ray methods can be used in both development and production, but the thermal test chip is restricted to development. The first two indirect thermal techniques find the amount of voiding in the thermal path and, through the use of thermal modeling, calculate the thermal resistance. The thermal test chip can only find the thermal resistance capability of the physical design.

3.7.2.1 Acoustic Microimaging

In acoustic microimaging, high-frequency ultrasound in the 10 to 100 MHz range is used to nondestructively create images of internal features of microelectronic components. Acoustic transducers alternately pulse ultrasound

into a DUT and then, a few microseconds later, detect the return echo. The ultrasound's round trip through the DUT's layers (die, die attach, substrate, substrate attach, and package) produces reflections at the discontinuities and interfaces. The amount of each reflection is a function of the acoustic impedance on either side of the interface. The acoustic impedance is a product of the density of the material and the speed of the ultrasound in the material. This method of acoustic microimaging is known as *reflection mode C-SAM®* (a registered trademark of Sonoscan).

The interface of the various packaging materials creates a moderate difference in acoustic impedance, which results in a computer-generated graphical image. The most visible differences in acoustic impedances are caused by voids or gaps in the interface. In most cases, the voids are either air, nitrogen, or a vacuum in which ultrasound does not propagate and creates zero acoustic impedance. The computer image for zero acoustic impedance appears as a different color and is easy to detect.

The ultrasound, on its return, arrives back at the transducer at various times, depending on its distance from the transducer. Electronic gating is used to mask out all of those echoes except for the interface being observed. This allows for examination of the features of a particular interface.

In C-SAM analysis, no special preparations are required. Sealed units can be examined as readily as open units. A coupling fluid is required between the DUT and the transducer. Although the most common fluid used is water, other fluids may be used.

The output of a C-SAM instrument is a multicolor graphical image that indicates discontinuities. A sample of a C-SAM output of a die attach with voids (converted to gray scale) is shown in Figure 3.29 [58].

C-SAM is a nondestructive test that provides voiding information on the heat path. By correlating the location and amount of voiding in conjunction with thermal modeling, C-SAM becomes a method that indirectly provides thermal resistance measurements.

C-SAM testing does not require the DUT to be powered. Test times range from several seconds to a minute depending upon the DUT size and scan speed. The C-SAM technique can be used in both development and production.

3.7.2.2   *X-Ray*

X-ray imaging of electronic assemblies can check for voids in the die-attach material to the substrate or to substrate-attach material to the package. There is no need to apply power to the DUT nor measure any electrical parameter. Devices may be potted or hermetically sealed for this test.

The classical mode of x-ray imaging passes x-rays through the DUT and hits a sensitive film on the other side. An image is created on the exposed film that is a shadow of the materials in the DUT that the x-rays have passed through. Modern x-ray equipment, called *real time x-ray*, passes the same waves through the DUT and detects the x-rays in an electronic device. The output of this device is converted to a graphical image for viewing on a
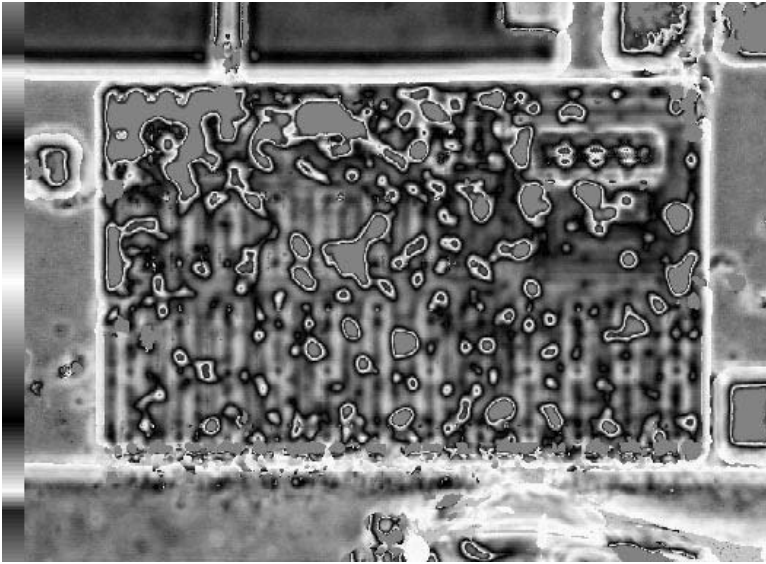
FIGURE 3.29
C-SAM image showing die attach voids. (From Sonoscan, Product Literature, http://www.sonoscan.com, accessed September 26, 2003. With permission.)

high-resolution computer monitor. The results of the x-ray test are a digitized image that may be viewed, stored, or printed. The digitized image can be processed to calculate the amount of voiding.

A shortcoming of the x-ray imaging techniques is their inability to detect cold solder joints when preforms are used. Some materials, such as aluminum and silicon, are transparent to x-rays. When high-density materials such as copper–tungsten, lead, or copper are used, it is difficult to see an image without increased x-ray power. An example of an x-ray image of a hybrid package and substrate is shown in Figure 3.30.

Both x-ray and C-SAM testing require a combination of thermal modeling with a maximum amount of voiding for each interface.

3.7.2.3 Thermal Test Chip

The thermal test chip is a specialized semiconductor consisting of a heater element, a temperature-sensitive device, and a diode forward voltage to measure temperature. The technique used is very similar to that of the theta-JC tester. A typical thermal test chip is shown in Figure 3.31. Prior to measuring the DUT temperature, the sensor diode is calibrated over a temperature range. With the base of the DUT held at a constant temperature, current is applied to the heater element, developing a power P in the chip and raising its temperature ΔT. For a known current in the sensor diode, the change in temperature is calculated by measuring the change in the diode forward voltage V_f, with and without the heater current.
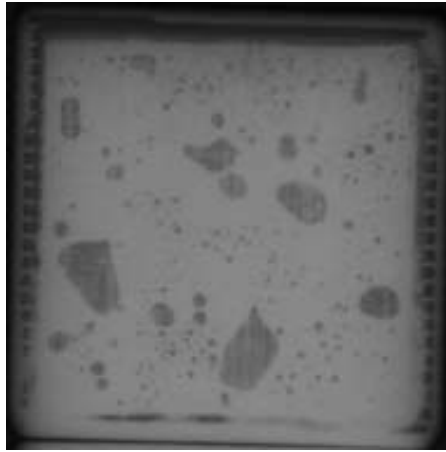
FIGURE 3.30
X-ray of hybrid package and substrate showing voiding.
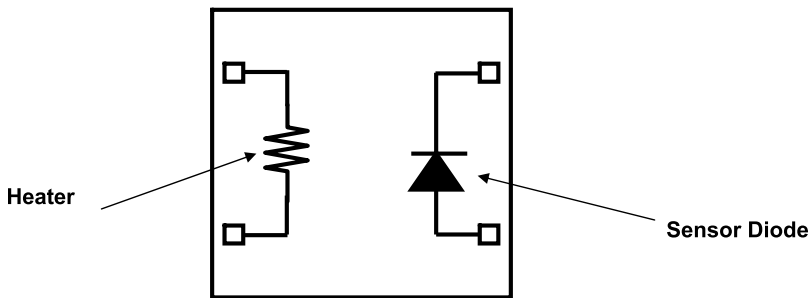
FIGURE 3.31
Thermal test chip. (From Krum, A., Measuring Thermal Resistance, *Advanced Packaging*, 1999. With permission.)

The thermal resistance θ of the microelectronic assembly is obtained in an indirect manner. The test assembly is the same as that of the actual assembly with one exception — the active device is replaced with the thermal test chip. Measuring the junction temperature of the test chip, the case temperature of the test DUT, and the power dissipation of the resistive heater, the thermal resistance of the test assembly is calculated with the formula:

$$\theta_{Test} = \frac{\Delta T}{P}. \tag{3.58}$$

The overall thermal resistance of the test assembly is the sum of the thermal resistances of the individual layers:

$$\theta_{Test} = \theta_{Die} + \theta_{Die\ Att} + \theta_{Sub} + \theta_{Subst\ Att} + \theta_{Package}. \tag{3.59}$$

If the thermal test chip were the same size as the actual active device and mounted in the test assembly with the same die-attach material, then the thermal resistance of the test assembly would be the same as the actual assembly. However, the chances of the thermal test die being the same size as the actual die are remote. Therefore, to find the thermal resistance for the actual assembly, the thermal resistance of the die (θ_{Die}) and the die attach ($\theta_{Die\ Att}$) need to be scaled. The equation for the die thermal resistance is

$$\theta_{Die} = \frac{t_{Die}}{K_{Die} A_{Die}}. \tag{3.60}$$

Scaling both the thickness (t_{Die}) and area ($A_{die} = L \times W$), a new value of thermal resistance is calculated that is a very good approximation for the minimum thermal resistance expected for actual production assemblies. However, this technique does not take into account die-attach and substrate-attach voids that may occur [56,59].

3.7.3 Stress Measurements

3.7.3.1 Piezoresistive Stress Sensors

Piezoresistive stress sensors make use of the material property in which the bulk resistivity is a function of the mechanical stresses applied to the material. The sensor is fabricated by placing a piezoresistive device on a thin silicon membrane, supported by a thicker silicon rim as shown in Figure 3.32. The thin membrane is fabricated by etching away the bulk silicon on
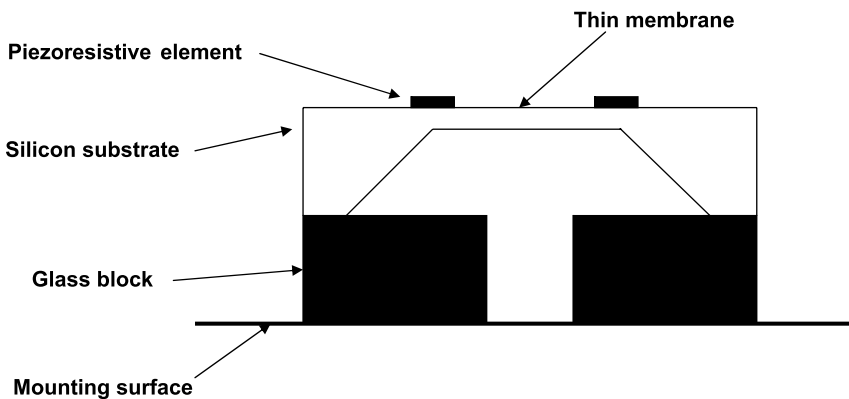
FIGURE 3.32
Piezoresistive stress sensor cross section.

FIGURE 3.33
Moiré interferometry showing part in compression.

a defined region until the required thickness is reached. The resistance of the device will change as a function of stress.

The assembly is mounted with a stress-free adhesive on the material in which the stress will be measured. Electrical connections are made to the piezoresistors and monitored at ambient and various temperatures [60].

3.7.3.2   *Moiré Interferometry*

Moiré interferometry is a technique used in microelectronic packaging to measure thermal deformation. A grating is photolithographically deposited on the surface of the specimen. This grating typically has a pitch of 5 μm for large strain measurements and can be much smaller for elastic strain measurements. Two coherent laser beams are shone on the surface of the specimen. The diffracted beams from the grating are collected and interfered producing a fringe pattern. The resulting interference pattern is proportional to the in-plane displacements. This scheme is used in both horizontal and vertical directions so that the deformations in perpendicular directions can be obtained. An example of a Moiré interferometry pattern is shown in Figure 3.33.

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4

Ceramic Materials

Jerry E. Sergent

CONTENTS

4.1 Introduction

Ceramics are the foundation of many microelectronic circuits, acting as the substrate to deposit conductive, resistive, and dielectric films to form

interconnections and passive components. They are formed by the bonding of a metal and a nonmetal and may exist as oxides, nitrides, carbides, or silicides. Ceramics are ideal as substrates for thick-film and thin-film circuits because they have a high electrical resistivity, are very stable chemically and thermally, and have a high melting point.

The primary bonding mechanism in ceramics is ionic bonding. Ionically bonded materials are crystalline in nature and have both a high electrical resistance and a high relative dielectric constant. A degree of covalent bonding as a result of sharing of electrons in the outer shell may also be present, particularly in some of the silicon and carbon-based ceramics. Both types of bonds are very strong, resulting in ceramics that have a high melting point, are very stable chemically, and are not attacked by ordinary solvents and most acids.

From the user's standpoint, there are two basic types of ceramic substrates: prefired or standard ceramics and cofired ceramics [1]. Although the end result is basically the same, there is a substantial difference between the manner in which low-temperature cofired ceramics (LTCC) and high-temperature cofired ceramics (HTCC) substrates are used as compared to standard substrates. Standard substrates are furnished as prefired structures that permit thick- and thin-film deposition directly. Multilayer structures are formed by depositing sequential layers of conductor and dielectric materials, interconnecting the conductor layers where necessary by small openings in the dielectric material called *vias*. Circuits manufactured in this manner by thick-film technology are often limited to three conductor layers, which is insufficient for circuits of very high complexity. By contrast, LTCC and HTCC substrates are furnished in the unfired or "green" state. The vias are punched in each layer as appropriate and each layer is printed with thick-film paste corresponding to the desired pattern and dried. The individual sheets are laminated together under pressure to form a monolithic structure. The structure is then fired by the user to form the finished circuit. Circuits of this type can consist of many layers to accommodate even the densest circuits. Further, passive components can be fabricated between the layers, increasing the area available for active devices on the top layer, permitting even higher circuit density.

This chapter primarily considers the properties of ceramics used in LTCC circuits, HTCC circuits, and the more standard ceramics, including aluminum oxide (alumina, Al_2O_3), beryllium oxide (beryllia, BeO), and aluminum nitride (AlN).

4.2   Substrate Manufacturing

Substrates made from pure ceramics are not easy to manufacture. Referring to Table 4.1, the processing temperature is very high and the degree of

TABLE 4.1

Melting Points of
Selected Ceramics

Material	Melting Point (°C)
SiC	2700
BN	2732
AlN	2232
BeO	2570
Al_2O_3	2000

sintering necessary to form a solid structure is difficult to obtain. For these reasons, ceramic substrates are typically mixed with fluxing and binding glasses that melt at a lower temperature and promote sintering, making the finished product denser. The LTCC materials have a higher percentage of glass than the other types and are often referred to as glass-ceramics. Materials used for LTCC circuits include as base materials cordierite (MgO, SiO_2, and Al_2O_3), glass-filled composites (SiO_2, B_2O_3, Al_2O_3, PbO, SiO_2, CaO, and Al_2O_3), and crystalline phase ceramics, (Al_2O_3, CaO, SiO_2, MgO, and B_2O_3) [2].

The initial steps in the manufacturing process of LTCC, HTCC, Al_2O_3, BeO, and AlN substrates are very similar [1]. The base material is ground into a fine powder, several microns in diameter, and mixed with various fluxing and binding glasses, also in the form of powders. At this point, the processes begin to diverge. As shown in Figure 4.1, there are three fundamental processes for fabricating substrates, with the individual steps described in Table 4.2.

In Figure 4.1a, an organic binder, along with various plasticizers, is added to the mixture and the resultant slurry is ball-milled, as depicted in Figure 4.2, to remove agglomerates and to make the composition uniform, followed by milling in a three-roll mill as shown in Figure 4.3. The output of the three-roll mill is a viscous mixture as shown in Figure 4.4. The slurry is formed into a sheet, the so-called green state, by tape casting and dried. The green tape is furnished to the user in a roll. In the green state, the substrate is approximately the consistency of putty and may be punched to the desired size. Holes and other geometries may also be punched at this time. The user then performs the remainder of the processes required to complete the circuit.

In Figure 4.1b, the green sheets are prepared as in Figure 4.1a and fired at a gradually increasing temperature to first completely remove the organics and then to sinter the particles together. In Figure 4.1c, only a small amount of organic material is added, if any, and the substrate is formed under pressure in a mold.

Once the part is formed and punched, it is sintered at a temperature above the melting point of glass and high enough to produce the degree of sintering necessary to form a continuous structure. The temperature profile is very
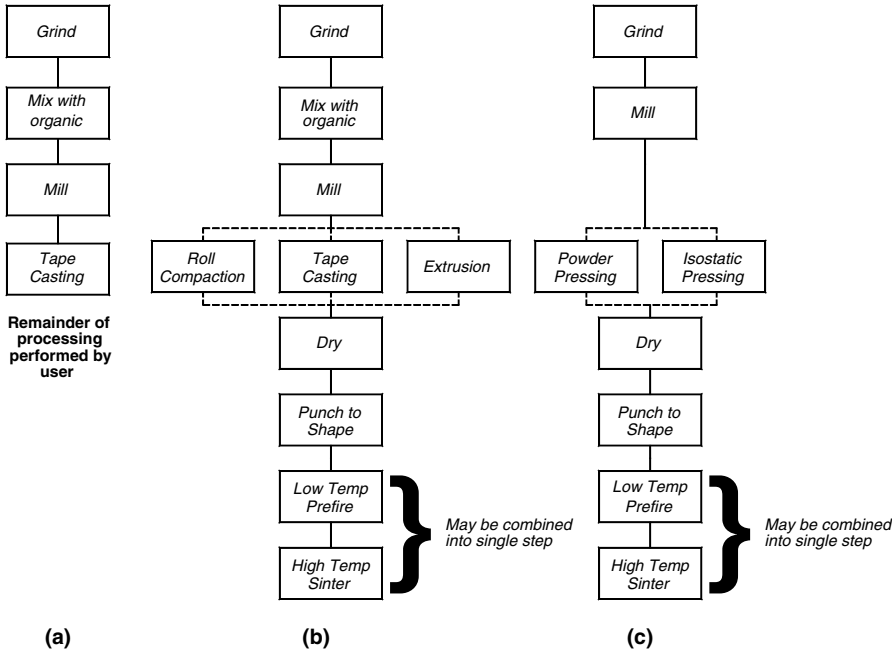
FIGURE 4.1
Flow chart for ceramic substrate fabrication.

TABLE 4.2

Processes for Forming Ceramic Substrates

Process	Description
Tape casting	The slurry is dispensed onto a moving belt that flows under a knife edge to form the sheet. This is a relatively low-pressure process compared to the others.
Powder pressing	The powder is forced into a hard die cavity and subjected to very high pressure (up to 20,000 psi) throughout the sintering process. This produces a very dense part with tighter as-fired tolerances than other methods, although pressure variations may produce excessive warpage.
Isostatic powder pressing	This process uses a flexible die surrounded with water or glycerin and compressed with up to 10,000 psi. The pressure is more uniform and produces a part with less warpage.
Extrusion	The slurry, less viscous than for other processes, is forced through a die. Tight tolerances are hard to obtain, but the process is very economical and produces a thinner part than is attainable by other methods.
Roll compaction	The slurry is sprayed onto a flat surface and partially dried to form a sheet with the consistency of putty. The sheet is fed through a pair of large parallel rollers to form a sheet of uniform thickness.
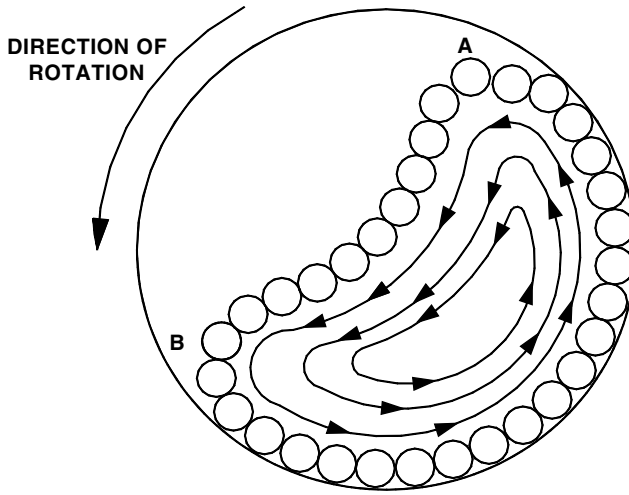
FIGURE 4.2
Ball milling of ceramic slurry.

ARROW DENOTES DIRECTION OF ROTATION

APRON
ROLL

CENTER
ROLL

FEED
ROLL
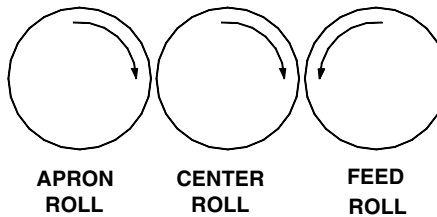
FIGURE 4.3
Three-roll milling of ceramic slurry.

critical and the process is usually performed in two stages; one stage to remove the volatile organic materials and a second stage to remove the remaining organics and to sinter the glass-ceramic structure. The peak temperature may be as high as several thousand degrees centigrade and may be held for several hours, depending on the material and the type and amount of binding glasses. For example, pure alumina substrates formed by powder processing with no glasses are sintered at 1930°C.

It is essential that all the organic material be removed before sintering. Otherwise, the gases formed by the organic decomposition may leave serious voids in the ceramic structure and cause serious weakening. The oxide ceramics may be sintered in air. Further, the CO produced during burnout may even reduce the metal oxides in the ceramic to pure metal. It is highly desirable to have an oxidizing atmosphere to aid in removing the organic materials by allowing them to react with the oxygen to form CO_2. The nitride

FIGURE 4.4
LTCC glass/ceramic after milling. (Photograph courtesy of Ferro Corp.)

ceramics must be sintered in the presence of nitrogen to prevent oxides of the metal from being formed. In this case, no reaction of the organics takes place; they are evaporated and carried away by the nitrogen flow.

In high volumes, the substrates are fired on a continuous belt furnace. This furnace must be very long and takes up a great deal of space. Alternatively, the substrates may be fired in the batch mode in a programmable kiln as

long as there are ample provisions for air circulation to remove the burnout components and to maintain an oxidizing atmosphere.

During sintering, a degree of shrinkage takes place as the organic is removed, the fluxing glasses activate, and sintering occurs. Shrinkage may be as low as 10% for powder processing and as high as 22% for sheet casting. The degree of shrinkage is highly predictable and may be compensated for during the design phase.

4.3   Surface Properties of Ceramics

There are two major surface properties of interest, surface roughness and camber, both highly dependent on the particle size and method of processing. Surface roughness is a measure of the surface microstructure, and camber is a measure of the deviation from flatness.

Surface roughness has a significant effect on the adhesion and performance of thick- and thin-film depositions, and, in general, the smaller the particle size, the smoother will be the surface. For adhesion purposes, it is desirable to have a high surface roughness to increase the effective interface area between the film and the substrate. For stability and repeatability, the thickness of the deposited film should be much greater than the variations in the surface. For thick films, which have a typical thickness of 10 to 12 µm, surface roughness is not a consideration, and a value of 625 nm (25 µin.) is desirable. For thin films [3], however, which may have a thickness measured in angstroms, a much smoother surface is required because a rough surface may result in a wider variation of resistor and conductor thickness across the pattern.

Surface roughness may be measured by electrical or optical means [1]. Electrically, surface roughness is measured by moving a fine-tipped stylus across the surface. The stylus may be attached to a piezoelectric crystal or to a small magnet that moves inside a coil, inducing a voltage proportional to the magnitude of the substrate variations. The stylus must have a resolution of 25.4 nm (1 µin.) to read accurately in the most common ranges. Optically, a coherent light beam from a laser diode or other source is directed onto the surface. The deviations in the substrate surface create interference patterns that are used to calculate the roughness. Optical profilometers have a higher resolution than the electrical versions and are used primarily for very smooth surfaces. For ordinary use, the electrical profilometer is adequate and is widely used to characterize substrates in both manufacturing and laboratory environments.

The output of an electrical profilometer is plotted as shown in schematic form in Figure 4.5, and in actual form in Figure 4.6. A quantitative interpretation of surface roughness can be obtained from this plot in one of two ways: by the rms value and by the arithmetic average.
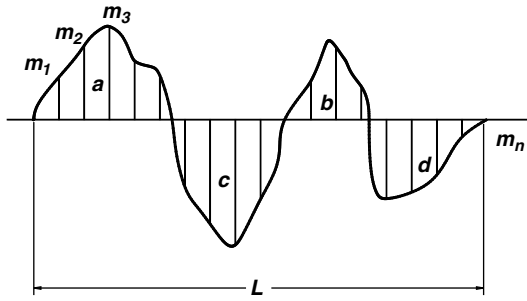
FIGURE 4.5
Schematic of surface trace.

a) 23 microinch surface   b) 0.3 microinch surface   c) 7 microinch surface
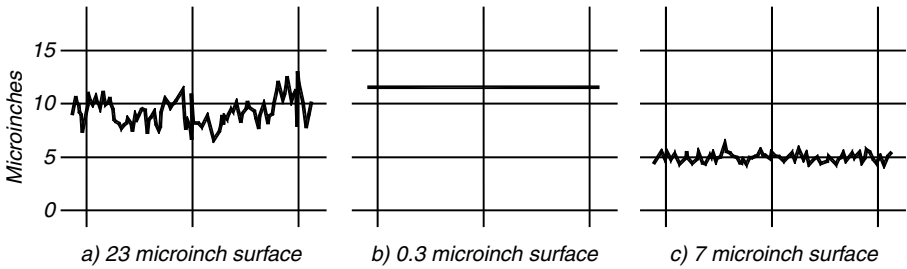
FIGURE 4.6
Surface trace of three substrate surfaces.

The rms value is obtained by dividing the plot into n small, even incre-
ments of distance and measuring the height m at each point, as shown in
Figure 4.5. The rms value is calculated by

$$rms = \sqrt{\frac{m_1^2 + m_2^2 + ... + m_n^2}{n}} \tag{4.1}$$

and the average value (usually referred to as the center line average [CLA])
is calculated by

$$CLA = \frac{a_1 + a_2 + a_3 + ... + a_n}{L} \tag{4.2}$$

where
$a_1, a_2, a_3, ...$ = areas under the trace segments (Figure 4.5)
L = length of travel

For systems in which the trace is magnified by a factor M, Equation 4.2
must be divided by the same factor.
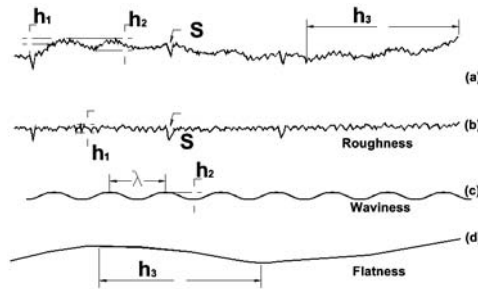
FIGURE 4.7
Surface characteristics.

For a sine wave, the average value is 0.636 × peak and the rms value is 0.707 × peak, which is 11.2% larger than the average. The profilometer trace is not quite sinusoidal in nature. The rms value may be greater than the CLA value by 10 to 30%.

Of the two methods, CLA is the preferred method of use because its calculation is more directly related to the surface roughness. However, it has the following shortcomings:

- The method does not consider surface waviness or camber as shown in Figure 4.7 [2].
- Surface profiles with different periodicities and the same amplitudes yield the same results, although the effect in use may be somewhat different.
- The value obtained is a function of the tip radius.

Camber and waviness are similar in form in that they are variations in flatness over the substrate surface. As seen in Figure 4.7, camber can be considered as an overall warpage of the substrate, whereas waviness is more periodic in nature. Both of these factors may occur as a result of uneven shrinkage during the organic removal/sintering process or as a result of nonuniform composition. Waviness may also occur as a result of a "flat spot" in the rollers used to form the green sheets.

Camber is measured in units of length/length, interpreted as the deviation from flatness per unit length, and is measured with reference to the longest dimension by placing the substrate through parallel plates set at a specific distance apart. Thus, a rectangular substrate would be measured along the diagonal. A typical value of camber is 0.003 in./in. (also 0.003 in. mm/mm), which for a 2 × 2-in. substrate, represents a total deviation of 0.003 in. × 2 in. × 1.414 = 0.0085 in. For a substrate that is 0.025 in. thick (a common value), the total deviation represents a third of the overall thickness!

The nonplanar surface created by camber adversely affects subsequent metallization and assembly processes. In particular, screen printing is made more difficult because of the variable snap-off distance. Torsion bar printing

heads on modern screen printers can compensate to a certain extent, but not entirely. A vacuum hold-down on the screen printer platen also helps, but only flattens the substrate temporarily during the actual printing process. Camber can also create excessive stresses and a nonuniform temperature coefficient of expansion. At temperature extremes, these factors can cause cracking, breaking, or even shattering of the substrate.

Camber is measured by first measuring the thickness of the substrate and then placing the substrate between a series of pairs of parallel plates set specific distances apart. Camber is calculated by subtracting the substrate thickness from the smallest distance that the substrate will pass through and dividing the result by the longest substrate dimension. A few generalizations can be made about camber, as follows:

- Thicker substrates have less camber than thinner substrates.
- Square shapes have less camber than rectangular shapes.
- The pressed methods produce substrates with less camber than the sheet methods.

4.4 Thermal Properties of Ceramic Materials

4.4.1 Thermal Conductivity

The thermal conductivity of a material is a measure of the ability to carry heat and is defined as

$$q = -k\,\frac{dT}{dx} \tag{4.3}$$

where
  k = thermal conductivity in W/m-°C
  q = heat flux in W/cm^2

$\dfrac{dT}{dx}$ = temperature gradient in °C/m in steady state

The negative sign denotes that heat flows from areas of higher temperature to areas of lower temperature.

There are two mechanisms that contribute to thermal conductivity; the movement of free electrons and lattice vibrations, or phonons. Local heating of material causes the kinetic energy of the free electrons in the vicinity of the heat source to increase, causing them to migrate to cooler areas. These electrons undergo collisions with other atoms, losing their kinetic energy in the process. The net result is that heat is drawn away from the source toward cooler areas. In a similar fashion, an increase in temperature increases the

magnitude of the lattice vibrations, which, in turn, generate and transmit phonons, carrying energy away from the source. The thermal conductivity of a material is the sum of the contributions of these two parameters:

$$k = k_p + k_e \qquad (4.4)$$

where
  k_p = contribution due to phonons
  k_e = contribution due to electrons

In ceramics, the heat flow is primarily due to phonon generation, and the thermal conductivity is generally lower than that of metals. Crystalline structures, such as alumina and beryllia, are more efficient heat conductors than amorphous structures such as glass. Organic materials used to fabricate printed circuit boards or epoxy attachment materials are highly amorphous electrical insulators, but tend to be very poor thermal conductors.

Impurities or other structural defects in ceramics tend to lower the thermal conductivity by causing the phonons to undergo more collisions, lowering the mobility and lessening their ability to transport heat away from the source. This is illustrated by Table 4.3, which lists the thermal conductivity of alumina as a function of the percentage of glass. Although the thermal conductivity of the glass binder is lower than that of alumina, the drop in thermal conductivity is greater than expected from the addition of glass alone. If the thermal conductivity is a function of the ratio of the materials alone, it follows the rule of mixtures:

$$k_T = P_1 \, k_1 + P_2 \, k_2 \qquad (4.5)$$

where
  k_T = net thermal conductivity
  P_1 = volume percentage of material 1 in decimal form
  k_1 = thermal conductivity of material 1
  P_2 = volume percentage of material 2 in decimal form
  k_2 = thermal conductivity of material 2

TABLE 4.3

Thermal Conductivity of Alumina Substrates with Different Concentrations of Alumina

Volume Percentage of Alumina	Thermal Conductivity (W/m-°C)
85	16.0
90	16.7
94	22.4
96	24.7
99.5	28.1
100	31.0
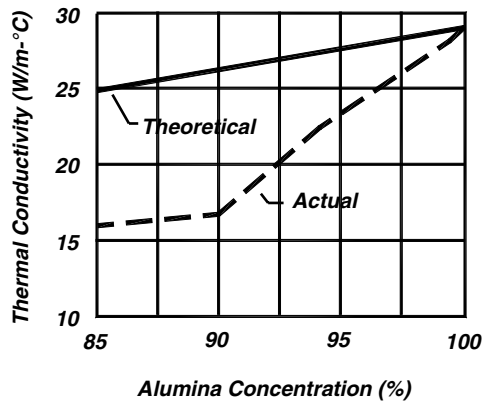
FIGURE 4.8
Thermal conductivity of alumina vs. concentration-theoretical and actual.
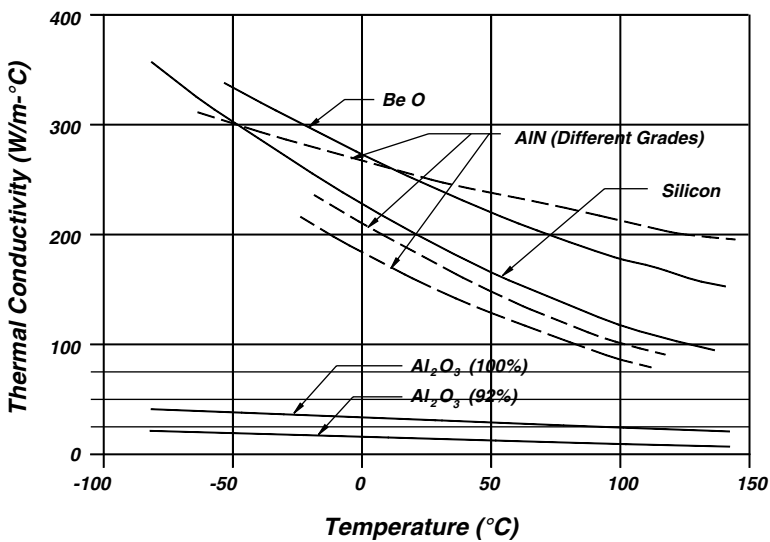
FIGURE 4.9
Thermal conductivity vs. temperature for selected materials.

In pure form, alumina has a thermal conductivity of about 31 W/m-°C, and the binding glass has a thermal conductivity of about 1 W/m-°C. Equation 4.5 and the parameters from Table 4.3 are plotted in Figure 4.8.

By the same token, as the ambient temperature increases, the number of collisions increases, and the thermal conductivity of most materials decreases. A plot of the thermal conductivity vs. temperature for several materials is shown in Figure 4.9 [4]. The thermal conductivity of HTCC materials approximates that of 92% alumina, but virtually no data exist in

TABLE 4.4

Thermal Conductivity of LTCC Materials from
Various Manufacturers at Room Temperature

Material	Thermal Conductivity (W/m·K)
DuPont 951	3.0
DuPont 943-A5	4.4
Ferro A6-5-M-13	2.0
Heraeus CT-2000	4.0
ESL 41110-25C[a]	2.5–3.0
Kyocera GL550	2.0
CeramTec Ceramtape GC	1.2–3.2
Nikko Ag2	3.0
96% Alumina	21.0

[a] Laminated to 96% alumina substrate.

the literature to characterize the thermal conductivity of LTCC materials as a function of temperature. Because of the higher glass content, the thermal conductivity of LTCC materials is substantially lower than that of alumina. A summation of the thermal conductivity of selected materials is given in Table 4.4.

4.4.2 Specific Heat

The specific heat of a material is defined as

$$c = \frac{dQ}{dT} \tag{4.6}$$

where
  c = specific heat in W-sec/g-°C
  Q = energy in W-sec
  T = temperature in K

The specific heat, c, is defined in a similar manner and is the amount of heat required to raise the temperature of 1 g of material by 1°, with units of W-sec/g-°C. The quantity "specific heat" in this context refers to the quantity c_V, which is the specific heat measured with the volume constant, as opposed to c_P, which is measured with the pressure constant. At the temperatures of interest, these numbers are nearly the same for most solid materials. The specific heat is primarily the result of an increase in the vibrational energy of the atoms when heated, and the specific heat of most materials increases with temperature up to a temperature called the *Debye temperature*, at which point it becomes essentially independent of temperature. The specific heat of several common ceramic materials as a function of temperature is shown
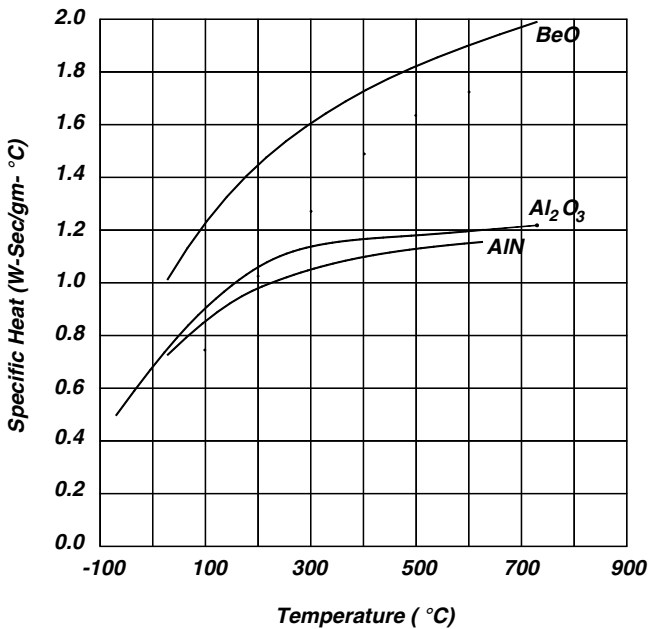
FIGURE 4.10
Specific heat vs. temperature for selected materials.

in Figure 4.10. As is common, there are very few data available for LTCC materials on this topic.

The heat capacity, C, is similar in form, except that it is defined in terms of the amount of heat required to raise the temperature of 1 mol of material by 1°C and is expressed in units of W-sec/mol-°C.

4.4.3   Temperature Coefficient of Expansion

The temperature coefficient of expansion (TCE) is a result of the asymmetrical increase in the interatomic spacing of atoms as a result of increased heat. Most metals and ceramics exhibit a linear, isotropic relationship in the temperature range of interest. The TCE is defined as

$$\alpha = \frac{l(T_2) - l(T_1)}{l(T_1)(T_2 - T_1)} \tag{4.7}$$

where
   α = temperature coefficient of expansion in ppm/°C
   T_1 = initial temperature
   T_2 = final temperature
   $l(T_1)$ = length at initial temperature
   $l(T_2)$ = length at final temperature

TABLE 4.5

Temperature Coefficient of Expansion
of Selected Ceramic Substrate
Materials

Material	TCE (ppm/°C)
Alumina (96%)	6.5
Alumina (99%)	6.8
BeO (99.5%)	7.5
AlN	4.8
DuPont 951[a]	5.8
DuPont 943-A5[a]	6.0
Ferro A6-5-M-13[a]	2.0
Heraeus CT-2000[a]	9.1
Heraeus CT-700[a]	7.5–7.9
ESL 41110-25C[a,b]	4.0–4.5
CeramTec GC[a]	7.9
Kyocera GL550[a]	5.9
Nikko Ag2[a]	7.8
Northrop Grumman Low K[a]	3.9
Samsung TCL-6A[a]	6.3

[a] LTCC material.
[b] Designed to be laminated to prefired
alumina.

The TCE of most ceramics is isotropic, although for certain crystalline or single-crystal ceramics, the TCE may be anisotropic, and some may even contract in one direction and expand in the other. Ceramics used for substrates do not generally fall into this category, as most are mixed with glasses in the preparation stage and do not exhibit anisotropic properties as a result. The temperature coefficient of expansion of several ceramic materials is shown in Table 4.5. This parameter is linear over the temperature range of interest.

4.5 Mechanical Properties of Ceramic Substrates

The mechanical properties of ceramic materials are strongly influenced by the strong interatomic bonds that prevail. Dislocation mechanisms, which create slip mechanisms in softer metals, are relatively scarce in ceramics, and failure may occur with very little plastic deformation. Ceramics also tend to fracture with little resistance.

4.5.1 Modulus of Elasticity

The TCE phenomenon has serious implications in the applications of ceramic substrates. When a sample of material has one end fixed, which may be

considered to be a result of bonding to another material with a much smaller TCE, the net elongation of the hotter end per unit length, or *strain (E)*, of the material is calculated by

$$E = TCE \times \Delta T \tag{4.8}$$

where
   E = strain in length/length
   ΔT = temperature differential across the sample

   Elongation develops a stress (S) per unit length in the sample as given by Hooke's law:

$$S = E\, Y \tag{4.9}$$

where
   S = stress in psi/in. (N/m²/m)
   Y = modulus of elasticity in lb/in.² (N/m²)

   When the total stress, as calculated by multiplying the stress per unit length by the maximum dimension of the sample, exceeds the strength of the material, mechanical cracks will form in the sample, which may even propagate to the point of separation. The small elongation that occurs before failure is referred to as *plastic deformation*. This analysis is somewhat simplistic in nature but serves for a basic understanding of the mechanical considerations. The modulus of elasticity of selected ceramics is summarized in Table 4.6, along with other mechanical properties.

TABLE 4.6

Mechanical Properties of Selected Ceramics

Material	Modulus of Elasticity (GPa)	Tensile Strength (MPa)	Compressive Strength (MPa)	Modulus of Rupture (MPa)	Flexural Strength (MPa)	Density (g/cm³)
Alumina (99%)	370	500	2600	386	352	3.98
Alumina (96%)	344	172	2260	341	331	3.92
Beryllia (99.5%)	345	138	1550	233	235	2.87
Aluminum nitride	300	310	2000	300	269	3.27
DuPont 951[a]	152			320		3.10
DuPont 943-A5[a]	149			230		3.20
Ferro A6-5-M-13[a]	92			130	>170	2.45
Kyocera GL550[a]	110				200	

[a] LTCC material.
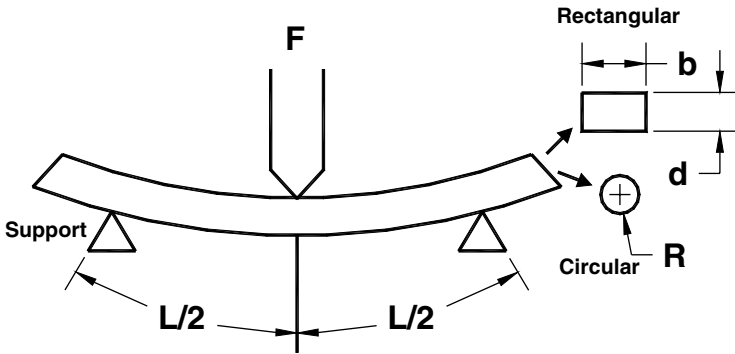
FIGURE 4.11
Modulus of rupture test setup.

4.5.2 Modulus of Rupture

Ordinary stress-strain testing is not generally used to test ceramic substrates because they do not exhibit elastic behavior to a great degree. An alternate test, the modulus of rupture (bend strength) test, as described in Figure 4.11, is preferred. A sample of ceramic, either circular or rectangular, is suspended between two points, a force is applied in the center, and the elongation of the sample is measured. The stress is calculated by

$$\sigma = \frac{M\,x}{I} \tag{4.10}$$

where
σ = stress in MPa
M = maximum bending moment in N-m
x = distance from center to outer surface in m
I = moment of inertia in N-m²

The expressions for σ, M, x, and I are summarized in Table 4.7. When these are inserted into Equation 4.10, the result is

$$\sigma = \frac{3\,F\,L}{2\,x\,y^2} \quad \text{(rectangular cross section)} \tag{4.11}$$

$$\sigma = \frac{F\,L}{\pi\,R^3} \quad \text{(circular cross section)} \tag{4.12}$$

TABLE 4.7

Parameters of Stress in
Modulus of Rupture Test [5]

Cross-Section	M	χ	I
Rectangular	$\dfrac{FL}{4}$	$\dfrac{y}{2}$	$\dfrac{xy^3}{12}$
Circular	$\dfrac{FL}{4}$	R	$\dfrac{\pi R^2}{4}$

where
  F = applied force in N
  x = long dimension of rectangular cross section in m
  y = short dimension of rectangular cross section in m
  L = length of sample in m
  R = radius of circular cross section in m

The modulus of rupture is the stress required to produce fracture and is given by

$$\sigma_r = \frac{3\,F_r\,L}{2\,x\,y^2} \qquad \text{(rectangular)} \qquad (4.13)$$

$$\sigma_r = \frac{F_r\,L}{\pi\,R^3} \qquad \text{(circular)} \qquad (4.14)$$

where
  σ_r = modulus of rupture in N/m²
  F_r = force at rupture

The modulus of rupture for selected ceramics is shown in Table 4.6.

4.5.3 Tensile and Compressive Strength

A force applied to a ceramic substrate in a tangential direction may produce tensile or compressive forces. If the force is tensile, in a direction such that the material is pulled apart, the stress produces plastic deformation as defined in Equation 4.9. As the force increases past a value referred to as the *tensile strength*, breakage occurs. Conversely, a force applied in the opposite direction creates compressive forces until a value referred to as the *compressive strength* is reached, at which point breakage occurs, too. The compressive strength of ceramics is, in general, much larger than the tensile strength. The

tensile strength and compressive strength of selected ceramic materials is shown in Table 4.6.

In practice, the force required to fracture a ceramic substrate is much lower than predicted by theory. The discrepancy is due to small flaws or cracks within these materials that result from processing. For example, when a substrate is sawed, small edge cracks may be created. Similarly, when a substrate is fired, trapped organic material may outgas during firing, leaving a microscopic void in the bulk. The result is an amplification of the applied stress in the vicinity of the void that may exceed the tensile strength of the material and create a fracture. If the microcrack is assumed to be elliptical with the major axis perpendicular to the applied stress, the maximum stress at the tip of the crack may be approximated by [5]

$$S_M = 2\,S_O \le \left(\frac{a}{\rho_t}\right)^{\frac{1}{2}} \tag{4.10}$$

where

S_M = maximum stress at the tip of the crack
S_O = nominal applied stress
a = length of the crack as defined in Figure 4.12
ρ_t = radius of the crack tip

The ratio of the maximum stress to the applied stress may be defined as

$$K_t = \frac{S_M}{S_O} = 2\left(\frac{a}{\rho_t}\right)^{\frac{1}{2}} \tag{4.11}$$
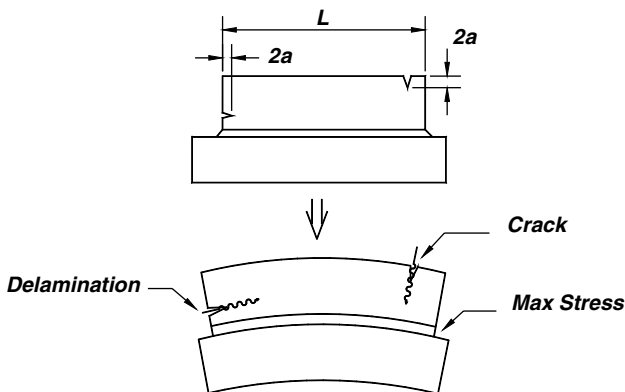
FIGURE 4.12
Stress concentration around a defect.

where

  K_t = stress concentration factor.

For certain geometries, such as a long crack with a small tip radius, K_t may be much larger than 1, and the force at the tip may be substantially larger than the applied force.

Based on this analysis, a material parameter called the *plain strain fracture toughness*, a measure of the ability of the material to resist fracture, can be defined as

$$K_{IC} = Z \, S_C \, \sqrt{\pi \, a} \qquad\qquad (4.12)$$

where

  K_{IC} = plain strain fracture toughness in psi-in.$^{1/2}$ or MPa·m$^{1/2}$
  Z = dimensionless constant, typically 1.2 [5]
  S_C = critical force required to cause breakage

From Equation 4.12, the expression for the critical force can be defined as

$$S_C = Z \, \frac{K_{IC}}{\sqrt{\pi \, a}} \, . \qquad\qquad (4.13)$$

When the applied force on the die due to TCE or thermal differences exceeds this figure, fracture is likely. The plain strain fracture toughness for selected materials is presented in Table 4.8. It should be noted that Equation 4.13 is a function of thickness up to a point but is approximately constant for the area-to-thickness ratio normally found in substrates.

4.5.4 Hardness

Ceramics are among the hardest substances known, and the hardness is correspondingly difficult to measure. Most methods rely on the ability of

TABLE 4.8

Fracture Toughness for Selected Materials

Material	Fracture Toughness (MPa·m$^{1/2}$)
Silicon	0.8
Alumina (96%)	3.7
Alumina (99%)	4.6
Silicon carbide	7.0
Molding compound	2.0

TABLE 4.9

Knoop Hardness for Selected
Ceramics

Material	Knoop Hardness (100 g)
Aluminum oxide	2100
Aluminum nitride	1200
Beryllium oxide	1200

one material to scratch another, and the measurement is presented on a relative scale. Of the available methods, the Knoop method is the most frequently used. In this approach, the surface is highly polished, and a pointed diamond stylus under a light load is allowed to impact on the material. The depth of the indentation formed by the stylus is measured and converted to a qualitative scale called the *Knoop* or *Hunt and Kosnik* (HK) scale. The Knoop hardness of selected ceramics is given in Table 4.9.

4.5.5 Thermal Shock

Thermal shock occurs when a substrate is exposed to temperature extremes in a short period of time. Under these conditions, the substrate is not in thermal equilibrium, and internal stresses may be sufficient to cause fracture. Thermal shock can be liquid to liquid or air to air, with the most extreme exposure occurring when the substrate is transferred directly from one liquid bath to another. The heat is more rapidly absorbed or transmitted, depending on the relative temperature of the bath, because of the higher specific heat of the liquid as opposed to air.

The ability of a substrate to withstand thermal shock is a function of several variables, including the thermal conductivity, the coefficient of thermal expansion, and the specific heat. Winkleman and Schott [6] developed a parameter called the *coefficient of thermal endurance* that qualitatively measures the ability of a substrate to withstand thermal stress:

$$F = \frac{P}{\alpha\,Y}\sqrt{\frac{k}{\rho\,c}} \tag{4.14}$$

where
  F = coefficient of thermal endurance
  P = tensile strength in MPa
  α = thermal coefficient of expansion in $1/°K$
  Y = modulus of elasticity in MPa
  k = thermal conductivity in $W/m·°K$
  ρ = density in kg/m^3
  c = specific heat in W-sec/kg-°K

TABLE 4.10

Thermal Endurance Factor for
Selected Materials at 25°C

Material	Thermal Endurance Factor
Alumina (99%)	0.640
Alumina (96%)	0.234
Beryllia (99.5%)	0.225
Aluminum nitride	2.325

The coefficient of thermal endurance for selected materials is shown in Table 4.10. The phenomenally high coefficient of thermal endurance of BN is primarily a result of the high ratio of its tensile strength to modulus of elasticity as compared to other materials. Diamond also has a high coefficient primarily because of its high tensile strength, high thermal conductivity, and low TCE.

The thermal endurance factor is a function of temperature in that several of the variables, particularly the thermal conductivity and the specific heat, are functions of temperature. From Table 4.10, it is also noted that the thermal endurance factor may drop rapidly as the alumina-to-glass ratio drops. This is because of the differences in the thermal conductivity and TCE of the alumina and glass constituents, which increase the internal stresses. This is true of other materials as well.

4.6 Electrical Properties of Ceramics

The electrical properties of ceramic substrates perform an important task in the operation of electronic circuits. Depending on the applications, the electrical parameters may be advantageous or detrimental to circuit function. Of most interest are the resistivity, the breakdown voltage or dielectric strength, and the dielectric properties, including the dielectric constant and the loss tangent.

4.6.1 Resistivity

The electrical resistivity of a material is a measure of the ability of that material to transport charge under the influence of an applied electric field. More often, this ability is presented in the form of electrical conductivity, the reciprocal of resistivity, as defined in Equation 4.15:

$$\sigma = \frac{1}{\rho} \tag{4.15}$$

where
  σ = conductivity in siemens/unit length
  ρ = resistivity in ohm-unit length

The conductivity is a function primarily of two variables: the concentration of charge and mobility, the ability of that charge to be transported through the material. The current density and applied field are related by Equation 4.16, which defines current density:

$$J = \sigma E \tag{4.16}$$

where
  J = current density in amperes/unit area
  E = electric field in volts/unit length

It should be noted that both the current density and electric field are vectors because the current is in the direction of the electric field.
  The current density may also be defined as

$$J = n \, v_d \tag{4.17}$$

where
  n = free carrier concentration in coulombs/unit volume
  v_d = drift velocity of electrons in unit length/second

The drift velocity is related to the electric field by

$$v_d = \mu \, E \tag{4.18}$$

where
  μ = mobility in length^2/volt-second.

In terms of the free carrier concentration and the mobility, the current density is

$$J = n \, \mu \, E. \tag{4.19}$$

Comparing Equation 4.14 with Equation 4.18 the conductivity can be defined as

$$\sigma = n \, \mu. \tag{4.20}$$

The free carrier concentration may be expressed as

$$n = n_t + n_i \tag{4.21}$$

where
  n_t = free carrier concentration due to thermal activity
  n_i = free carrier concentration due to field injection.

The thermal charge density, n_t, in insulators is a result of free electrons' obtaining sufficient thermal energy to break the interatomic bonds, allowing them to move freely within the atomic lattice. Ceramic materials characteristically have few thermal electrons as a result of the strong ionic bonds between atoms. The injected charge density, n_i, occurs when a potential is applied and is a result of the inherent capacity of the material. The injected charge density is given by

$$n_i = \varepsilon\, E \tag{4.22}$$

where
  ε = dielectric constant of the material in farads/unit length.

Inserting Equation 4.22 and Equation 4.21 into Equation 4.19, the result is

$$J = \mu\, n_t\, E + \mu\, \varepsilon\, E^2. \tag{4.23}$$

For conductors, $n_t \gg n_i$ and Ohm's law applies. For insulators, $n_i \gg n_t$, and the result is a square law relationship between the voltage and the current [7]:

$$J = \mu\, \varepsilon\, E^2. \tag{4.24}$$

The conductivity of ceramic substrates is extremely low. In practice, it is primarily due to impurities and lattice defects, and may vary widely from batch to batch. The conductivity is also a strong function of temperature. As the temperature increases, the ratio of thermal to injected carriers increases. As a result, the conductivity increases, and the V–I relationship follows Ohm's law more closely. Typical values of the resistivity of selected ceramic materials are presented in Table 4.11.

4.6.2 Breakdown Voltage

The term *breakdown voltage* is very descriptive. Although ceramics are normally very good insulators, the application of excessively high potentials can dislodge electrons from orbit with sufficient energy to allow them to dislodge other electrons from orbit, creating an "avalanche effect." The result

TABLE 4.11

Electrical Properties of Selected Ceramic Substrates

	Property			
Material	Electrical Resistivity (Ω-cm)	Breakdown Voltage (AC KV/mm)	Relative Dielectric Constant	Loss Tangent (@ 1 MHz)
Alumina (96%)				
25°C	$>10^{14}$		9.0	
500°C	4×10^9	8.3	10.8	0.0002
1000°C	1×10^6			
Alumina (99.5%)				
25°C	$>10^{14}$			
500°C	2×10^{10}	8.7	9.4	0.0001
1000°C	2×10^6		10.1	
Beryllia				
25°C	$>10^{14}$	6.6	6.4	0.0001
500°C	2×10^{10}		6.9	0.0004
Aluminum nitride	$>10^{13}$	14	8.9	0.0004
DuPont 951[a]	$>10^{12}$	>1.1	7.8	0.0015
DuPont 943-A5[a]	$>2 \times 10^{12}$	>1.0	7.4	0.0009
Ferro A6-5-M-13[a]	$>10^{14}$	>5[b]	5.9	0.002[c]
CeramTec GC[a]	$>10^{12}$	>1.0	7.9	0.002
Nikko Ag2[a]	N/A	N/A	7.1	0.003
Kyocera GL550[a]	N/A	N/A	5.6	0.0009
ESL 41110-25C[a]	$>10^{12}$	>1.2	4.5	0.004

Note: N/A = not available.

[a] LTCC material.
[b] Per layer.
[c] 1–100 GHz.

is a breakdown of the insulation properties of the material, allowing current to flow. This phenomenon is accelerated by elevated temperature, particularly when mobile ionic impurities are present.

The breakdown voltage is a function of numerous variables, including the concentration of mobile ionic impurities, grain boundaries, and the degree of stoichiometry. In most applications, the breakdown voltage is sufficiently high not to be an issue. However, there are two instances in which it must be considered:

1. At elevated temperatures created by localized power dissipation or high ambient temperature, the breakdown voltage may drop by orders of magnitude. Combined with a high potential gradient, this condition may be susceptible to breakdown.

2. The surface of most ceramics is highly "wettable," in that moisture tends to spread rapidly. Under conditions of high humidity, coupled with surface contamination, the effective breakdown voltage is much lower than the intrinsic value.

4.6.3   Dielectric Properties

Two conductors in proximity with a difference in potential have the ability to attract and store electric charge. Placing a material with dielectric properties between them enhances this effect. A dielectric material has the capability of forming electric dipoles (displacements of electric charge) internally. At the surface of the dielectric, the dipoles attract more electric charge, thus enhancing the charge storage capability, or *capacitance*, of the system. The relative ability of a material to attract electric charge in this manner is called the *relative dielectric constant*, or *relative permittivity,* and is usually given the symbol K. The relative permittivity of free space is 1.0 by definition, and the absolute permittivity is

$$\varepsilon_o = \text{permittivity of free space}$$

$$\varepsilon_o = \frac{1}{36\,\pi} \times 10^{-9}\ \frac{farads}{meter}. \tag{4.25}$$

The relationship between the polarization and the electric field is

$$\bar{P} = \varepsilon_o \left(K - 1 \right) \bar{E} \quad \frac{Q}{m^2} \tag{4.26}$$

where
  $\bar{P}$ = polarization, coulombs/m²
  $\bar{E}$ = electric field, V/m

There are four basic mechanisms that contribute to polarization.

1. *Electronic polarization*. In the presence of an applied field, the cloud of electrons is displaced relative to the positive nucleus of the atom or molecule, creating an induced dipole moment. Electronic polarization is essentially independent of temperature and may occur very rapidly. The dielectric constant may therefore exist at very high frequencies, up to 10^{17} Hz.

2. *Molecular polarization.* Certain molecular structures create permanent dipoles that exist even in the absence of an electric field. These may be rotated by an applied electric field, generating a degree of polarization by orientation. Molecular polarization is inversely proportional to temperature and occurs only at low-to-moderate frequencies. Molecular polarization does not occur to a great extent in ceramics and is more prevalent in organic materials and liquids, such as water.

3. *Ionic polarization.* Ionic polarization occurs in ionically bonded materials when the positive and negative ions undergo a relative displacement to each other in the presence of an applied electric field. Ionic polarization is somewhat insensitive to temperature and occurs at high frequencies, up to 10^{13} Hz.

4. *Space charge polarization.* Space charge polarization exists as a result of charges derived from contaminants or irregularities that exist within the dielectric. These charges exist to a greater or lesser degree in all crystal lattices and are partly mobile. Consequently, they will migrate in the presence of an applied electric field. Space charge polarization occurs only at very low frequencies.

In a given material, more than one type of polarization can exist, and the net polarization is given by

$$\bar{P}_t = \bar{P}_e + \bar{P}_m + \bar{P}_i + \bar{P}_s \tag{4.27}$$

where
$\quad \bar{P}_t$ = total polarization
$\quad \bar{P}_e$ = electronic polarization
$\quad \bar{P}_m$ = molecular polarization
$\quad \bar{P}_i$ = ionic polarization
$\quad \bar{P}_s$ = space charge polarization

Normally, the dipoles are randomly oriented in the material, and the resulting internal electric field is zero. In the presence of an external applied electric field, the dipoles become oriented as shown in Figure 4.13.
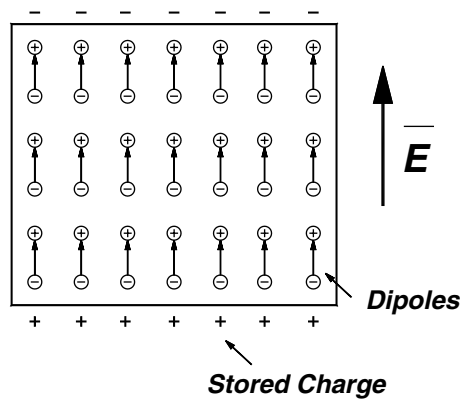
FIGURE 4.13
Orientation of dipoles in an electric field.

There are two common ways to categorize dielectric materials: polar or nonpolar and paraelectric or ferroelectric. Polar materials include those that are primarily molecular in nature, such as water, and nonpolar materials include both electronically and ionically polarized materials. Paraelectric materials are polarized only in the presence of an applied electric field and lose their polarization when the field is removed. Ferroelectric materials retain a degree of polarization after the field is removed. Materials used as ceramic substrates are usually nonpolar and paraelectric in nature. An exception is silicon carbide, which has a degree of molecular polarization.

In the presence of an electric field that is changing at a high frequency, the polarity of the dipoles must change at the same rate as the polarity of the signal to maintain the dielectric constant at the same level. Some materials are excellent dielectrics at low frequencies, but the dielectric qualities drop off rapidly as the frequency increases. Electronic polarization, which involves only displacement of free charge and not ions, responds more rapidly to the changes in the direction of the electric field, and remains viable up to about 10^{17} Hz. The polarization effect of ionic displacement begins to fall off at about 10^{13} Hz, and molecular and space charge polarizations fall off at still lower frequencies. The frequency response of the different types is shown in Figure 4.14, which also illustrates that the dielectric constant decreases with frequency.

Changing the polarity of the dipoles requires a finite amount of energy and time. The energy is dissipated as internal heat, quantified by a parameter called the *loss tangent* or *dissipation factor*. Further, dielectric materials are not perfect insulators. These phenomena may be modeled as a resistor in parallel with a capacitor. The loss tangent, as expected, is a strong function of the applied frequency, increasing as the frequency increases.

In alternating current applications, the current and voltage across an ideal capacitor are exactly 90° out of phase, with the current leading the voltage. In fact, the resistive component causes the current to lead the voltage by an angle less than 90°. The loss tangent is a measure of the real or resistive component of the capacitor and is the tangent of the difference between 90° and the actual phase angle:

$$\text{Loss tangent} = \tan(90° - \delta) \tag{4.28}$$

where
  δ = phase angle between voltage and current.

The loss tangent is also referred to as the *dissipation factor* (DF).

The loss tangent may also be considered as a measure of the time required for polarization. It requires a finite amount of time to change the polarity of the dipole after an alternating field is applied. The resulting phase retardation is equivalent to the time indicated by the difference in phase angles.

Polarization
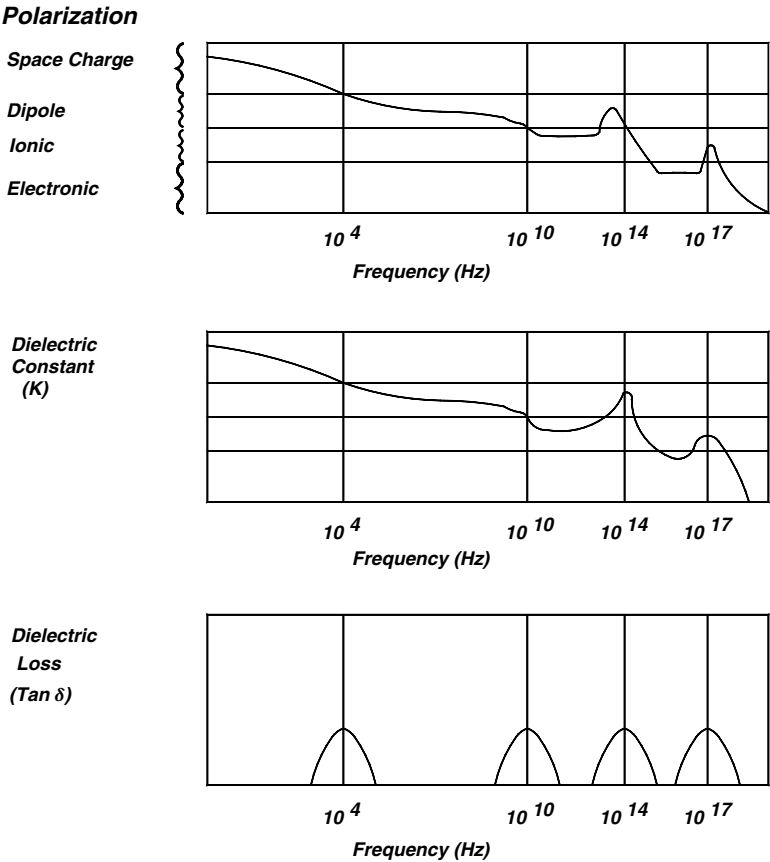
FIGURE 4.14
Frequency effects on dielectric materials.

4.7   Processing of HTCC Substrates

HTCC multilayer circuits are primarily alumina based. The green tape is blanked into sheets of uniform size, and holes are punched where vias and alignment holes are required. The metal patterns are printed and then dried. Despite their relatively high electrical resistance, refractory metals such as tungsten and molybdenum are used as conductors because of the high firing temperature. Via fills may be accomplished during conductor printing or during a separate printing operation. The process is repeated for each layer, as described in detail in Chapter 6.

The individual layers are aligned and laminated under heat and pressure to form a monolithic structure in preparation for firing. The structure is

heated to approximately 600°C to remove the organic materials. Carbon residue is removed by heating to approximately 1200°C in a wet hydrogen atmosphere. Sintering and densification take place at approximately 1600°C.

During firing, HTCC circuits shrink anywhere from 14 to 17%, depending on the organic content. With careful control of the material properties and processing parameters, the shrinkage can be controlled within 0.1%. Shrinkage must be taken into consideration during the design, punching, and printing processes. The artwork enlargement must exactly match the shrinkage factor associated with a particular lot of green tape.

Processing of the substrate is completed by plating the outer layers with nickel and gold for component mounting and wire bonding. The gold is plated to a thickness of 25 µin. for gold wire and 5 µin. for aluminum wire. Gold wire bonds to the gold plating, whereas aluminum wire bonds to the nickel underneath. The gold plating in this instance is simply to protect the nickel surface from oxidation or corrosion.

The properties of HTCC materials are summarized in Table 4.13.

4.8   Processing of LTCC Substrates

The green tape is furnished in a roll or as precut squares approximately 3–12 in. on a side. The first step is to cut four alignment holes with a punch or laser in each corner followed by cutting holes for vias and other requirements. The punch is preferred for high-volume applications whereas the laser is best for prototypes. The most common via size is 250 µm, with vias as low as 100 µm being possible [8]. This is about half the size attainable by conventional thick-film technology.

The individual layers that make up the circuit are processed by first filling the vias with a conductor paste. This is accomplished by conventional screen-printing techniques using a stencil to accommodate the small via holes. The shrinkage of LTCC circuits during firing is in the range of 12–18%. It is highly desirable that the via-fill materials have the same shrinkage rate to prevent open circuits after firing. Once the via-fill material has been dried, the desired pattern for that layer can be printed and dried. The inner layers are typically silver-based for economic reasons with gold on the top and bottom layers to facilitate wire bonding and die mounting. The via-fill materials that interface between the gold and silver layers must be of a special composition to prevent electrolytic reactions between the gold and silver.

The LTCC technology offers the possibility of fabricating resistors and capacitors on inner layers that can be cofired along with the other circuitry. This saves a tremendous amount of area over conventional circuits and increases the packaging density by orders of magnitude. Consider that every input and output of a digital circuit needs a pull-up or pull-down resistor. In a complex circuit, this can require hundreds or even thousands of resistors.

Because the accuracy requirement of these resistors is not very stringent, laser trimming is usually not necessary.

After all the layers have been printed, dried, and inspected, they are stacked using the holes previously cut in the corners for alignment. The circuits are then laminated under heat and pressure to form a monolithic structure. There are two lamination approaches that are commonly used: uniaxial and isostatic. In the uniaxial approach, the circuits are placed between two heated parallel plates, and a force is applied in the normal direction. For better accuracy and lower distortion, the isostatic method is preferred. The circuit is enclosed in tooling and water at about 80°C, and 300 psi is applied to the tool.

Finally, the circuit is fired to remove the organics and to allow the active materials to sinter. First, the laminated circuit is heated to about 450°C with a ramp of 2–5°C/min to allow the organic materials to burn away followed by a ramp to about 880°C at a rate of about 15°C/min. The circuit is allowed to sinter at 880°C for 15 min where sintering occurs and is cooled back to room temperature at a rate of about 5°C/min (approximately 3 h).

Two cofiring methods are commonly used: free sintering and constrained sintering. In free sintering, no constraints are placed on the circuit and shrinking is allowed in the x, y, and z directions. In the constrained sintering process, two additional layers are laminated to the top and bottom of the structure to prevent lateral movement, allowing shrinking only in the z direction. Typical shrinkage factors are shown in Table 4.12.

After cooling, further thick-film processes, such as resistor printing and firing and laser trim, can be performed. A comparison of HTCC and LTCC technologies is presented in Table 4.13. The reader can refer to Chapter 6 for a more detailed discussion of the HTCC and LTCC processes.

4.9 Applications

Standard prefired ceramic substrates have been used to fabricate complex hybrid microelectronic circuits for many years. Figure 4.15 and Figure 4.16 show examples of thick- and thin-film circuits. Figure 4.15 is a digital logic circuit fabricated on a three-layer thick-film circuit, whereas Figure 4.16 is a

TABLE 4.12

Typical Shrinkage Factors for LTCC during Firing

	x–y Shrinkage (%)	z Shrinkage (%)
Free sintering	11.5 ± 0.3	17 ± 0.5
Constrained sintering	0.1 ± 0.05	45 ± 0.4

TABLE 4.13

Properties of LTCC and HTCC Multilayer Ceramic Materials

	Low-Temperature Cofired Ceramic (LTCC)	High-Temperature Cofired Ceramic (HTCC)

Material	Cordierite
	  MgO, SiO_2, Al_2O_3
	Glass-filled composites
	  SiO_2, B_2O_3, Al_2O_3
	  PbO, SiO_2, CaO, Al_2O_3
	Crystalline phase ceramics
	  Al_2O_3, CaO, SiO_2, MgO, B_2O_3
		88–92% alumina

Firing temperature	850–1050°C	1500–1600°C
Conductors	Au, Ag, Cu, PdAg	W, MoMn
Conductor resistance	3–20 mΩ/□	8–12 mΩ/□
Dissipation factor	15×10^4–30×10^{-4}	5×10^4–15×10^{-4}
Relative dielectric constant	5–8	9–10
Resistor values	0.1 Ω–1 MΩ	Not available
Firing shrinkage		
x–y	12.0 ± 0.1%	12–18%
z	17.0 ± 0.5%	12–18%
Repeatability	0.3–1%	0.3–1%
Line width	100 μm	100 μm
Via diameter	125 μm	125 μm
Number of metal layers	33	63
Coefficient of Thermal Expansion (CTE)	3–8 ppm/°C	6.5 ppm/°C
Thermal conductivity	2–6 W/m-°C	15–20 W/m-°C

summing network utilizing the thin-film technology that requires a number of precision resistors.

LTCC technology is used extensively in the microwave industry primarily because of three reasons:

1. The dielectric constant of LTCC materials is somewhat lower than for the standard substrate materials because of the high glass content. This feature minimizes stray capacitance and cross-coupling of signals.

2. The excellent high-frequency transmission characteristics of the LTCC material, as witnessed by the low loss tangent, minimize signal loss.

3. The ability to fabricate circuits with a high number of layers allows for virtually unlimited ground planes, power planes, and shielded signal planes, all of which contribute to improved performance at high frequencies.
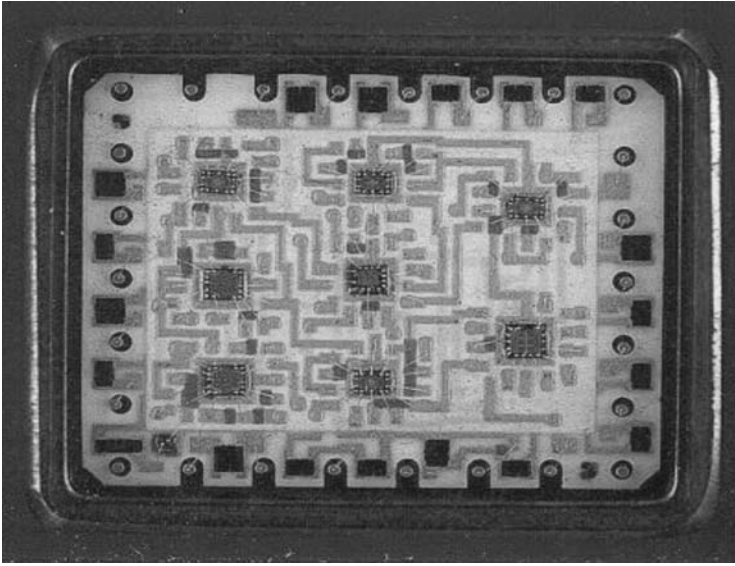
FIGURE 4.15
Digital logic circuit fabricated with the thick film technology on alumina ceramic.
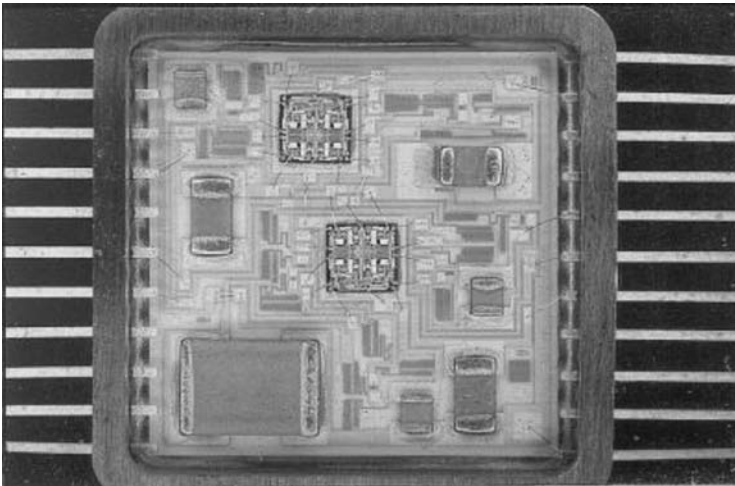
FIGURE 4.16
Summing network fabricated with thin film deposition on alumina ceramic.

Examples of the LTCC technology used in this application are shown in Figure 4.17 and Figure 4.18. Figure 4.17 is a Bluetooth™ module with an integrated antenna designed and manufactured by IMST GmbH in Kamp-Lintfort, Germany. The board is 15 × 32 mm with the antenna and 15 × 21 mm without the antenna. It consists of six conductor layers separated by
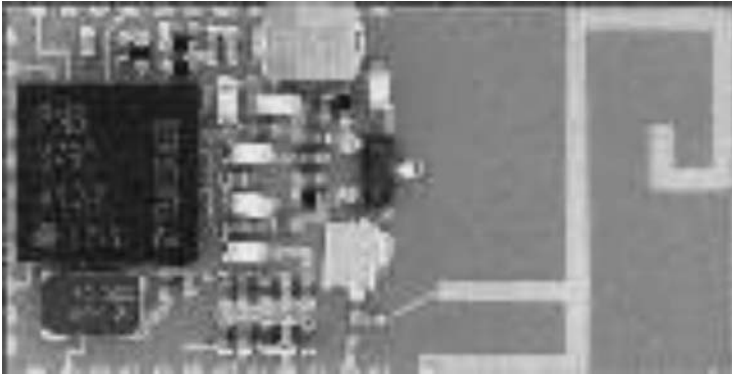
FIGURE 4.17
Bluetooth® module with integrated antenna fabricated with LTCC. (Photograph courtesy of IMST GmbH.)
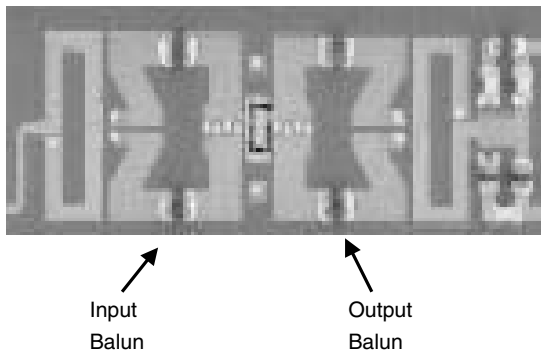
FIGURE 4.18
Balanced push-pull amplifier with integrated balun transformer fabricated with LTCC. (Photograph courtesy of IMST GmbH.)

Ferro A6S LTCC material. Figure 4.18 is a balanced push–pull amplifier, also designed and manufactured by IMST GmbH. This circuit operates between 900 and 1800 MHz and contains an integrated balun transformer.

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5

Screen Printing

Jerry E. Sergent

CONTENTS

5.1   Introduction

Screen printing is a method by which patterns of thick-film paste or solder paste are applied to a substrate as shown in Figure 5.1.

During the design process, artwork is generated for each layer to be printed, with the dark portions corresponding to the printed areas as seen in the examples in Figure 5.2 [2–4].

The artwork is placed in contact with a screen coated with a photosensitive material (photosensitive emulsion resist) and exposed to ultraviolet (UV) light through the artwork. The UV light hardens the areas of photoresist not covered by the dark portions of the artwork. The remainder of the photoresist is removed by washing with a spray of water. The result is a screen, shown in Figure 5.3, with openings that correspond on a 1:1 basis with the areas to be printed.

The screen, thus generated, is placed in a screen-printing machine designed to hold the screen in proximity and parallel to the substrate. Paste is placed on the screen, a substrate is placed directly under the screen, and the printing process is activated. A squeegee formed from a flexible material, such as neoprene, is directed across the screen at a predetermined angle, speed, and pressure. The paste is forced through the openings on the screen to the substrate in a pattern corresponding to the artwork. In this manner,
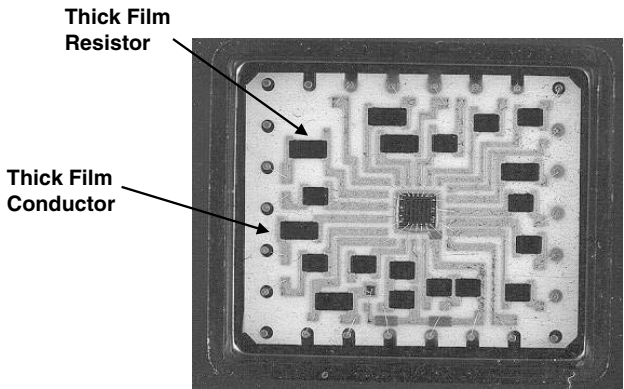
FIGURE 5.1
Patterns on a thick film circuit formed by screen printing.
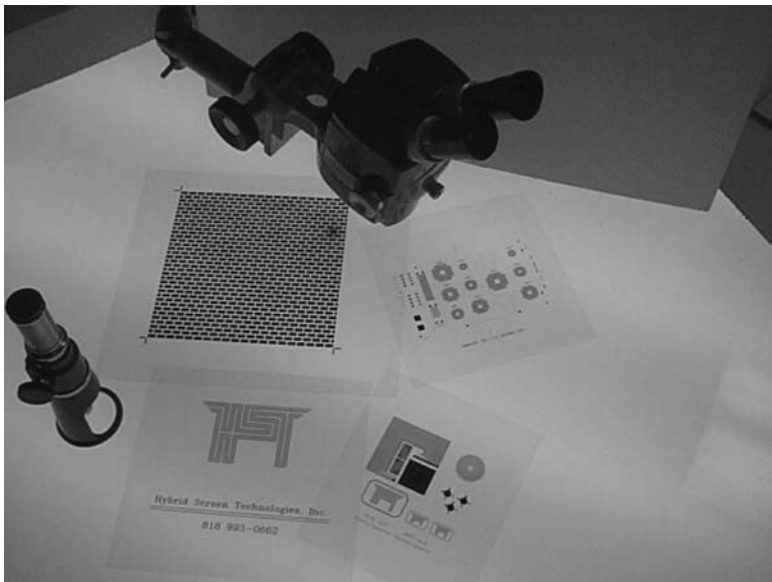
FIGURE 5.2
Typical artwork used to expose screen patterns.
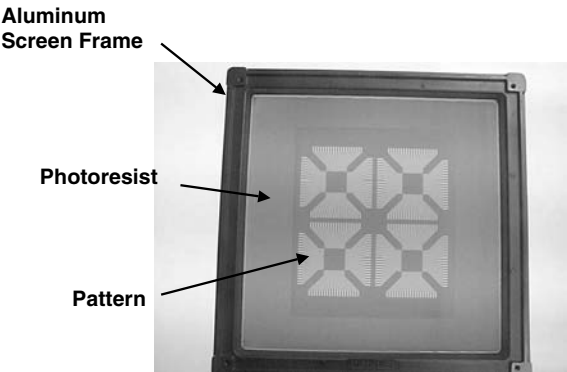
FIGURE 5.3
Finished screen.

the paste can be applied in very precise geometries, allowing complex interconnection patterns to be generated.

Screen printing has been used for thousands of years to generate designs. In ancient China, silk was one of the first materials used as a mesh. A pattern was created in the silk using pitch or similar materials to block out unwanted areas, and dye was forced through the pattern by hand to cloth or other surfaces to create colored patterns. By performing several sequential screenings with different colors and patterns, complex decorative patterns could

be formed. This continues to be one of the most common applications of the screen-printing process [5–7].

Silk continued to be one of the most common materials used until the development of synthetic materials, and the term "silk screening" is still commonly used to describe the screen-printing process. The development of synthetic fibers, such as nylon, made possible greater control of the mesh materials, and the added development of photosensitive materials used for creating the patterns allowed screen printing to become much more precise, repeatable, and controllable [8].

Today, in the electronics industry, the primary mesh material is stainless steel, which adds an additional degree of control and precision over nylon in addition to added resistance to wear and stretching [9]. The crude hand methods of printing have evolved to sophisticated, microprocessor-controlled machines that are self-aligning, have the ability to measure the thickness of the film and also to adjust the printing parameters to compensate for variations in the properties of the thick-film paste [10–12].

Still, of all the processes used to manufacture electronic circuits, the screen-printing process is the least analytical. It is not possible to measure the parameters of the paste and convert them to the proper printer settings needed to produce the desired results due to the large number of variables involved. Many of the variables are not in the direct control of the process engineer and may change as the printing proceeds. For example, the viscosity of the paste may change during a print run as a result of evaporation of the solvent used to thin the paste. Screen printing will remain one of the processes where the skill of the process engineer cannot be replaced by a computer.

Although it is possible to screen very viscous pastes or pastes with large particles using a coarse screen, a stencil — with openings created by etching, laser, or electroforming — is the preferred method of application for these types of pastes. The screen wires interfere with the transfer of the paste to the substrate, leaving voids in the printed film.

This chapter deals primarily with the screen printing of thick-film paste on ceramic substrates. Information on stencils and solder printing is readily found in treatises dealing with the surface-mount technology.

5.2   The Screen

The screen mesh is manufactured by weaving stainless steel wires to form a long sheet. The direction along the length of the sheet is referred to as the "warp" direction, whereas the direction across the width of the sheet is referred to as the "weft" direction. The vast majority of meshes used in thick-film screen printing are woven in the so-called plain weave pattern, as shown in Figure 5.4, formed by routing one wire over and under only one wire at

Cross-Section of Screen and Emulsion
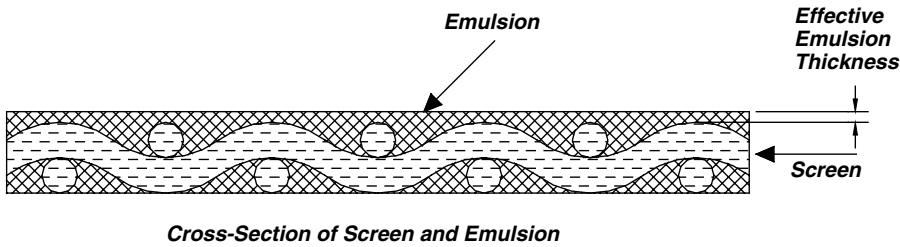
FIGURE 5.4
Plain weave screen with emulsion.
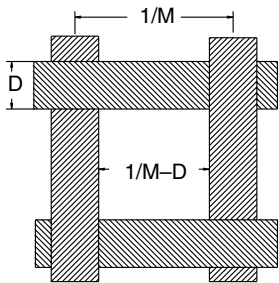
FIGURE 5.5
Screen opening.

a time. In the twilled weave pattern, each wire is routed over and under two wires at a time. The plain weave has more open area for a given mesh count and wire size, whereas the twilled weave is stiffer and is less likely to stretch [13].

One of the most important parameters of the screen is the mesh count, or the number of wires per unit length. In general, the mesh count is the same for both the warp and weft directions, as is the wire size. In practice, the mesh count may vary from 80 wires per inch for coarse screening, such as solder paste, to 400 wires per inch for fine-line printing.

Another important parameter is the size of the opening in the screen, which strongly influences the amount of paste that can be transferred during the printing process, and limits the maximum particle size of the material used to manufacture the paste. The opening is dependent on both the mesh size and the wire count as shown in Figure 5.5, and may be calculated by Equation 5.1:

$$O = \frac{1}{M} - D \qquad\qquad (5.1)$$
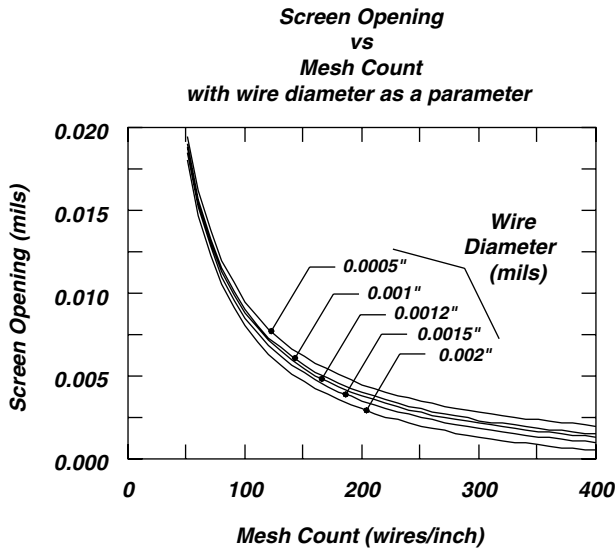
FIGURE 5.6
Graph of screen opening vs. mesh count and wire diameter.

where
O = dimension of the opening
M = mesh count
D = diameter of the wire

A graph of the size of the opening as a function of mesh count and wire diameter is shown in Figure 5.6.

The overall thickness of the screen mesh will be approximately two times that of the wire diameter, but may be slightly smaller or larger than 2X, depending on the technique used in the weaving process. In weaving processes where a great deal of pressure is applied to the mesh, the mesh thickness is slightly less than 2X and the mesh is referred to as a hard mesh. A hard mesh is not as pliable as a soft mesh and is less desirable in most applications.

The amount of paste transferred during the printing process is dependent on the volume of the opening in the screen. Assuming that the thickness of the mesh is 2X the wire diameter, the volume of the opening may be approximated by Equation 5.2:

$$V = (2\,D)\left(\frac{1}{M} - D\right)^2. \tag{5.2}$$

The reader should keep in mind that the emulsion thickness may not be ignored for fine-mesh screens. For example, a 325/0.9/0.7 screen has a wire diameter of 0.9 mil and typically has an emulsion thickness of 0.7 mil.

Empirically, from Equation 6.2, the volume of the opening is zero when either $D = 1/M$ or when $D = 0$. At some value of D, in between 0 and $1/M$, therefore, the volume must be at a maximum. Expanding Equation 5.2 and taking the derivative with respect to D, the volume is maximized when the relationship defined in Equation 5.3 is met:

$$D = \frac{1}{6\,M}\,. \tag{5.3}$$

In most cases, this results in a wire diameter that is too small to be readily woven. In practice, however, this is not a severe problem, because the amount of paste transferred is adequate for most purposes.

Typical parameters of stainless steel mesh are given in Table 5.1. The most commonly used screen meshes are 80 mesh, used primarily for solder paste, 200 mesh used for thick-film conductors and resistors, 325 mesh, used for thick-film conductors, dielectrics, and resistors, and 400 mesh, used for fine-line (< 0.010 in.) thick-film conductors [14].

TABLE 5.1

Parameters of Plain-Weave Stainless Steel Screen

Mesh Count	Nominal Wire Diameter (in.)	Mesh Opening (in.)	Open Area (%)	Weave Thickness Range (in.)
80	0.0020	0.0105	70.5	0.0036–0.0046
80	0.0037	0.0088	49.5	0.0073–0.0090
80	0.0055	0.0070	31.4	0.0010–0.00125
105	0.0030	0.0065	46.9	0.0060–0.0067
120	0.0026	0.0057	47.3	0.0052–0.0058
135	0.0023	0.0051	47.5	0.0045–0.0047
145	0.0022	0.0047	46.4	0.0048–0.0052
150	0.0026	0.0041	37.2	0.0051–0.0057
165	0.0020	0.0041	44.9	0.0042–0.0048
180	0.0018	0.0038	45.7	0.0037–0.0043
200	0.0016	0.0034	46.2	0.0032–0.0038
200	0.0021	0.0029	33.6	0.0041–0.0046
230	0.0014	0.0029	45.9	0.0028–0.0034
230	0.0011	0.0039	54.0	0.0023–0.0027
250	0.0016	0.0024	36.0	0.0034–0.0038
270	0.0014	0.0023	38.6	0.0030–0.0035
280	0.0012	0.0024	44.1	0.0026–0.0032
325	0.0009	0.0022	50.1	0.0020–0.0025
325	0.0011	0.0020	41.3	0.0023–0.0028
400	0.0010	0.0015	36.0	0.0020–0.0024
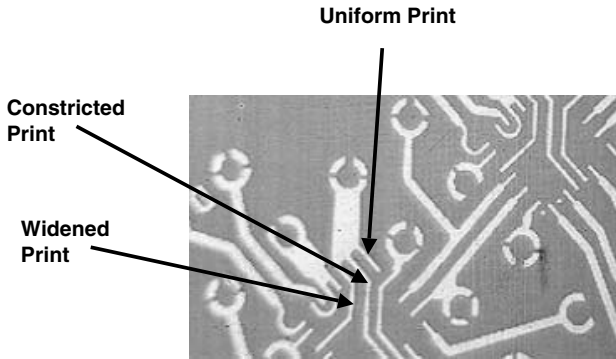
FIGURE 5.7
Screen with traces at 0° and 45° illustrating the effect of pattern orientation.

As most of the traces in a typical thick-film circuit are parallel or at right angles to the screen frame, it is preferable that the mesh be oriented at an angle of 22° to 45° to the frame to prevent the partial blocking of the opening on one side of the trace by the screen wire. On long traces, this can lead to narrowing or widening of the print at periodic intervals, and, on fine-line prints of less than 0.010-in. width, can lead to a discontinuity in the trace. Figure 5.7 illustrates this well. Two of the traces that are printed along the orientation of the mesh (0°) exhibit narrowing and widening, respectively, whereas the trace printed at a 45° angle is very uniform.

The screen frame is usually made from cast aluminum, as shown in Figure 5.3, with the bottom of the frame machined to be parallel to and at a fixed distance from the top. With these specifications, the screen will be parallel to the substrate mounting platform and will have the same reference point with respect to the substrate. This precaution will greatly improve the quality and reproducibility of the print as well as minimizing the setup time.

The screen is prepared for use by stretching the mesh by pneumatic or mechanical methods over a large frame capable of accommodating several smaller screen frames. The tension may be measured by an electronic tensiometer capable of measuring the tension in either the warp or the weft direction, or by simply measuring the deflection in the center of the screen produced by a 1-lb weight. The deflection method is the most common, but the tensiometer allows much greater control over the process. The mesh is attached to the small frames with epoxy that cures at room temperature. After curing, the mesh is trimmed away around the periphery of the epoxy, simultaneously separating the individual screen frames. A screen manufactured in this manner can be expected to last for thousands of prints without losing tension when handled and treated properly. Note that a screen attached at 45° is more expensive than one attached at 90° as more of the screen material is wasted during the manufacturing process.

The final step in preparing the screen for use is to coat it with a photosensitive emulsion. The so-called direct emulsion is initially in liquid form. To

sensitize the screens, a dam or mold is formed around the periphery of the screen with cellophane tape or similar material to control the thickness. The emulsion thickness is measured from the bottom of the screen as shown in Figure 5.4. The top of the screen mesh is placed on a flat surface exactly the size of the inside of the frame. The emulsion is poured on the mesh and smoothed with a straightedge to coat the screen evenly and fill the mesh. The thickness may be built up, if desired, by allowing the initial coating to dry and repeating the process with a second dam. If stored in a black, light-free plastic bag in a cool environment, screens coated with a direct emulsion may be stored for several months prior to exposure. All commercial screen makers use direct emulsions for this reason.

The screen is exposed by placing the emulsion side of the artwork in contact with the emulsion (bottom) side of the screen and exposing the screen to UV light, preferably collimated. The period of exposure varies with the strength of the source, the distance from the source, the type of emulsion, the quality of the artwork, and the thickness of the emulsion. The unexposed emulsion protected by the artwork may be removed by gently washing the screen with a spray of warm water. After drying at room, or slightly elevated, temperature, the screen is again exposed to UV light to further harden the remaining emulsion.

The quality of the screen is critical to the screen-printing process. The wire mesh should initially be inspected for uniformity of wire size and the size of the opening. The screen must be cleaned with detergent to remove any oils and dirt prior to sensitization, and all photoprocesses must be performed under yellow light. The emulsions used for screen printing are not ultrasensitive to light, but the exposure time even to yellow light should be minimized [15].

5.3   The Stencil

Stencils can be formed by photoetching a pattern through a thin sheet of brass or stainless steel from both sides of the metal. The opening created in this manner has a characteristic hourglass shape, narrower in the middle than at the top and bottom. There is also a limitation in the minimum size of the opening owing to the fact that the etching process proceeds laterally, and at the same, time, it is etching vertically through the metal as illustrated in Figure 5.8. This not only limits the pitch of the devices that can be mounted in surface mount technology (SMT) applications, but also necessitates complicated correction factors that vary with the size and thickness of the metal. The so-called hourglass effect can be minimized by electropolishing the stencil. This process is accomplished by attaching the stencil to electrodes and immersing it in an acid bath. The electric field lines concentrate at the sharp edges, causing these areas to etch faster than smoother surfaces. The
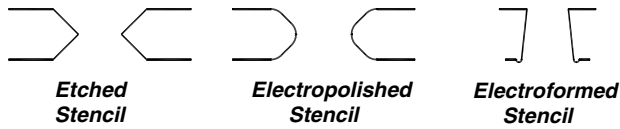
FIGURE 5.8
Cross section of etched, polished, and electroformed stencils.

sharp edges become rounded, resulting in better paste transfer (Figure 5.8) [16,17].

   Whereas small openings can be created with electron-discharge machining (EDM) or with a laser, these are relatively expensive processes because the openings must be cut one at a time. These processes form openings with uniform dimensions, but must frequently be electropolished to provide the desired smoothness [18].

   The electroforming process grows the stencil around a pattern exposed on a thick photoresistive film placed on a flat conducting surface called a *mandrel*. The mandrel, usually copper, allows nickel to be electroplated in the openings in the photoresist to generate a stencil with extremely fine pitch and dimensional control. Stencils grown in this manner have been used to print epoxy and solder in geometries as small as 0.002 in. An added feature of electroformed stencils is the gasket that forms around the edges of the opening, again as a result of the higher field strength. The gasket prevents solder smearing, allowing finer geometries. The opening is trapezoidal-shaped to facilitate paste transfer, as shown in Figure 5.8 [19].

   Stencils are seldom used for printing complex geometries, such as thick-film circuits, because it is difficult to prevent sharp corners and angles in the stencil from bending. Also, all openings must be surrounded by the metal foil to maintain continuity of the stencil, further limiting complexity of the pattern [20].

5.4   The Paste

The composition and characteristics of the paste are critical factors in screen printing. The cermet (combination of ceramic and metal) pastes commonly used in the thick-film technology have four major ingredients: (1) an active element that establishes the function of the film, (2) an adhesion element that provides the adhesion to the substrate, (3) an organic binder a matrix that holds the active particles in suspension and which provides the proper fluid properties for screen printing, and (4) a solvent or thinner that establishes the viscosity of the vehicle phase [21,22].

5.4.1 The Active Element

The active element, or material, within the active element gives the fired film its electrical properties. If the active material is a metal, the fired film will be a conductor; if it is a conductive metal oxide, a resistor; and, if it is an insulator, a dielectric. The active metal is in powder form ranging from 1 to 10 μm, with a mean diameter of about 5 μm. Particle morphology can be varied greatly depending on the method used to produce the metallic particles. Spherical, flaked, or acicular shapes (both amorphous and crystalline) are available from powder manufacturing processes. Structural shape and particle morphology is critical to the development of the desired electrical performance and, therefore, the control on the particle shape, size, and distribution must be maintained to ensure uniformity of the properties of the fired film [23,24].

5.4.2 The Adhesion Element

Two primary constituents are used to bond the film to the substrate. One adhesion element is a glass, or frit, with a relatively low melting point. The glass melts during firing, reacts with the glass in the substrate, and flows into the irregularities on the substrate surface to provide the adhesion. In addition, the glass flows around the active material particles, holding them in contact with each other to promote sintering, and to provide a series of three-dimensional continuous paths from one end of the film to the other. Principal thick-film glasses are based on B_2O_3–SiO_2 network formers with modifiers such as PbO, Al_2O_3, Bi_2O_3, ZnO, BaO, and CdO added to change the physical characteristics of the film, such as melting point, viscosity, and coefficient of thermal expansion. Because of its excellent wetting properties, both to the active element and to the substrate, Bi_2O_3 is also used as a flux. The glass phase may be introduced as a prereacted particle or formed *in-situ* by using glass precursors such as boric oxide, lead oxide, and silicon.

A second class of conductor materials uses metal oxides to provide the adhesion. In this case, a pure metal is placed in the paste and it reacts with oxygen atoms on the surface of the substrate to form an oxide. The conductor adheres to the oxide and to itself by sintering, which takes place during firing. Typical metals used in this application are copper and cadmium. During firing, the oxides react with broken oxygen bonds on the surface of the substrate, forming a Cu or Cd spinel structure. Conductors of this type offer improved adhesion and have a pure metal surface for added bondability, solderability, and conductivity. Conductors of this type are referred to as fritless, oxide-bonded, or molecular-bonded materials.

A third class of conductor materials uses both reactive oxides and glasses. These materials, referred to as mixed-bonded systems, incorporate the advantages of both technologies and are the most frequently used conductor materials.

5.4.3 The Organic Binder

The organic binder is generally a thixotropic fluid and serves two purposes: (1) it acts as a vehicle to hold the active and adhesion elements in suspension until the film is fired and (2) it gives the paste the proper fluid characteristics for screen printing. The organic binder is usually referred to as the nonvolatile organic because it does not evaporate as such, but begins to burn off at about 350°C. The binder must oxidize completely during firing, with no residual carbon that could contaminate the film. Typical materials used in these applications are ethyl cellulose and various acrylics [25,26].

For nitrogen-fireable films, where the firing atmosphere can contain only a few ppm of oxygen, the organic vehicle must decompose and thermally depolymerize, departing as a highly volatile organic vapor in the nitrogen blanket provided as the firing atmosphere, because oxidation into CO_2 or H_2O is clearly impossible.

5.4.4 The Solvent or Thinner

The organic binder in its usual form is too thick to permit screen printing, which necessitates the use of a solvent or thinner. The thinner is somewhat more volatile than the binder, evaporating rapidly above (about) 100°C, and is referred to as the volatile component. Typical materials used for this application are, terpineol, butyl carbitol, or one of the complex alcohols into which the nonvolatile phase can dissolve. The low vapor pressure at room temperature is desirable to minimize drying of the pastes and to maintain a constant viscosity during printing. Additionally, plasticizers, surfactants, and agents that modify the thixotropic nature of the paste are added to the solvent to improve paste characteristics and printing performance.

The combination of the organic binder and the thinner are often referred to as the vehicle that transports the active element and the adhesion element to the substrate.

After the four major ingredients of the thick-film paste are selected, they are mixed together in proper proportions and milled on a three-roll mill for a sufficient period of time to ensure that they are thoroughly mixed and that no agglomeration exists. After the initial mixing, the paste is sometimes maintained on a slow-moving roller to ensure continual slow mixing and ensure that the phases do not separate.

5.5 Critical Parameters of the Paste

There are three critical parameters of the paste that relate to screen printing: (1) the ratio of the solids content, (2) the particle size distribution, and (3) the viscosity.

5.5.1 Solids Content

The solids content (active element + adhesion element) as a ratio of the total weight of the paste will dramatically affect the ability of the paste to be screened and also the density of the fired film. If the solids content is high, the fired film will be dense, but will also be difficult to screen.

The solids content is measured by weighing a sample of the material in a ceramic beaker, burning away the organic vehicle in an oven, and reweighing the solids content. The solids content is the ratio of the weight of the solids to the original weight of the sample and is expressed in percentage. A typical value for thick-film conductors is 85–92%.

5.5.2 Particle Size Distribution

The particle size distribution of a thick-film paste is a compromise between screenability and the properties of the fired film. For screenability, it is desired to have very small particles, but very small particle sizes in thick-film resistors produce parameters that are skewed and not suitable for most circuit applications. Larger particles will obviously be more difficult to screen and may actually block one or more screen openings.

Particle size distribution may be measured in a manufacturing environment by the use of a fineness-of-grind (FOG) gauge. An FOG gauge is created by machining or etching a groove with a very shallow slope in a stainless steel block, as shown in Figure 5.9. A sample of paste is placed in the deeper end and moved toward the shallow end with a flat spatula. At some point, where the depth of the groove is the same as the largest particle, that particle will be trapped and will leave a gap in the film behind the spatula. The size of the particle is determined by noting the depth of the groove on the scale on the side of the FOG gauge. At a later point, all the particles will be trapped, leaving a gap that is the width of the groove. This marks the smallest particle size. At some point between the largest particle size and the smallest, approximately half the groove will be gaps, and the other half, paste. This marks the mean particle size in the sample. If the particle size distribution is uniform, the halfway point will be exactly between the points that mark the largest and smallest particle sizes.

5.5.3 Viscosity

Viscosity is a subset of the science of rheology, the study of the flow and deformation of materials, and is the property that defines the resistance to the flow of a liquid. Viscosity is related to the molecular attraction within the body of the liquid and is the ratio of the shear rate of the fluid (in sec[1]) to the shear stress (in force per unit area).
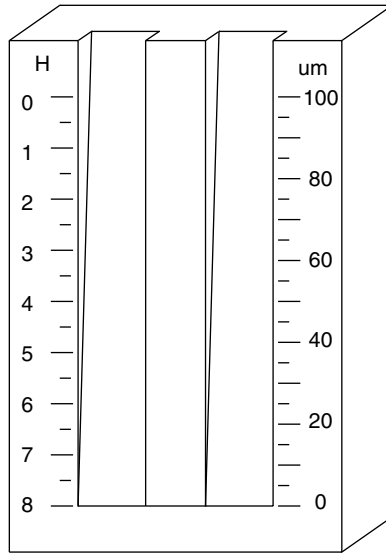
FIGURE 5.9
Fineness-of-Grind (FOG) gauge.

Picture a sample of fluid in layers of area, *A*, as shown in Figure 5.10 [1] with a force, *F*, applied. Assuming no slip, the bottom layer will stay fixed and the other layers will move with a velocity, *V(x)*.

The shear stress is defined as

$$\sigma = \frac{F}{A} \quad \frac{N}{m^2} \tag{5.4}$$

and the shear rate is defined as

$$\dot{\gamma} = \frac{dV}{dx} \quad \frac{1}{sec}. \tag{5.5}$$

The viscosity is defined as

$$\eta = \frac{\sigma}{\dot{\gamma}} \quad \frac{N}{m^2 \cdot sec} \quad (Pascal - sec). \tag{5.6}$$

An alternate unit of viscosity is the poise, where

$$1\ Poise = \frac{1\ dyne}{cm^2 \cdot sec}. \tag{5.7}$$
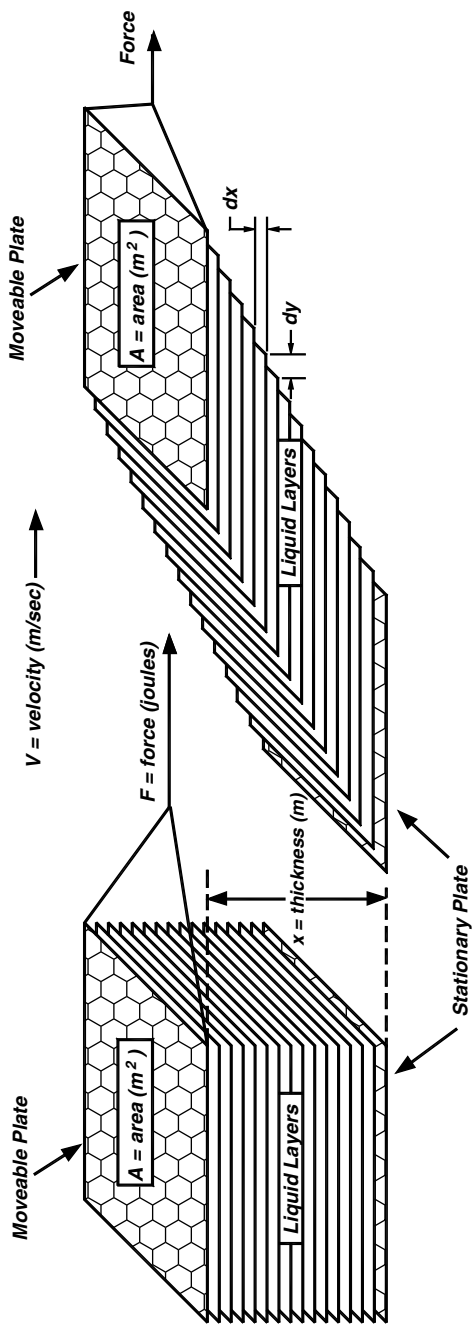
FIGURE 5.10
Fluid flow under the influence of a force.
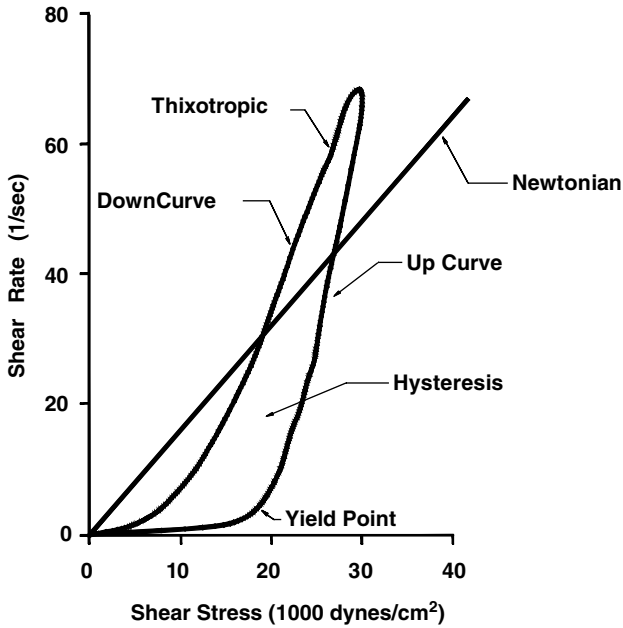
FIGURE 5.11
Shear Rate vs. Shear Stress (Viscosity).

The conversion factor is
1 Pa-sec = 10 P.

By definition, the viscosity of water at 20.2°C is 1 cp.

In an ideal or Newtonian fluid, as shown in Figure 5.11, the characteristic curve is a straight line that passes through the origin. Newtonian fluids are not suitable for screen printing, because the force of gravity is always present. As some degree of flow will always be present, Newtonian fluids will seek a level and will not retain any definition. For example, water very nearly approaches being a Newtonian fluid.

To be suitable for screen printing, a fluid must have the following characteristics as illustrated in Figure 5.11:

1. The fluid must have a yield point, or minimum pressure required to produce flow. This force must obviously be above the force of gravity. With a finite yield point, the paste will not flow through the screen at rest, and will not flow on the substrate after printing.

2. The fluid should be somewhat thixotropic in nature. A thixotropic fluid is one in which the shear rate/shear stress ratio is nonlinear. As the shear rate (which translates to the combination of squeegee pressure, velocity, and screen tension) is increased, the paste becomes substantially thinner, causing it to flow more readily. The
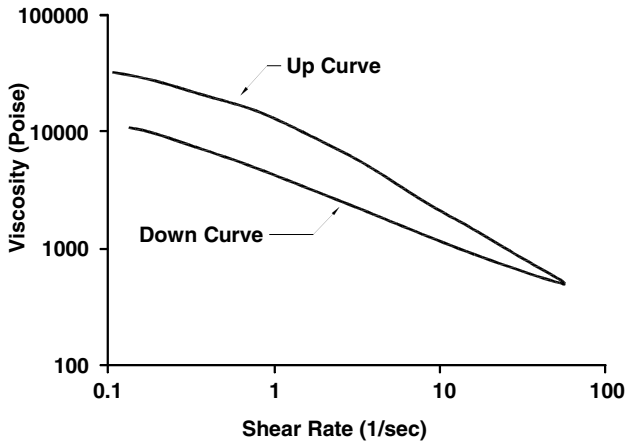
FIGURE 5.12
Viscosity vs. Shear Rate.

corollary to this term is *pseudoplastic*. A pseudoplastic fluid is one in which the shear rate does not increase appreciably as the force is increased.

3. The fluid should have some degree of hysteresis, such that the viscosity at a given pressure is dependent on whether or not the pressure is increasing or decreasing. Preferably, the viscosity should be higher with decreasing pressure, as the paste will be on the substrate at the time and will have a lesser tendency to flow and lose definition.

The viscosity of thick-film paste is tailored to meet these characteristics, with a shear rate vs. shear stress curve shaped like that of Figure 5.11. Figure 5.12 clearly indicates the reduction in viscosity as the shear rate increases. This is a very important characteristic. During the screen-printing process, while force is being applied by the squeegee, it is desirable to have the paste flow readily so that it transfers completely from the screen to the substrate. After the squeegee has passed and the paste is on the substrate, it is desirable for the viscosity to be high so that the paste does not flow, maintaining the definition of the pattern.

The viscosity of a thick-film paste is a function of many variables, the most important to the user being, particle size, temperature, and shear rate. It is also important to note that viscosity is also a function of time due to the hysteresis effect. Figure 5.11 is misleading to a certain extent in that it implies that, if *x* amount of shear stress is applied, the shear rate will instantly be the corresponding value *y*. In reality, there is a finite and significant amount of time that elapses between the time the force is applied and the time when the final viscosity is reached as depicted in Figure 5.13. This time must be accounted for during and after the printing process. During the print, the squeegee velocity must be such as to permit the paste enough time to lower
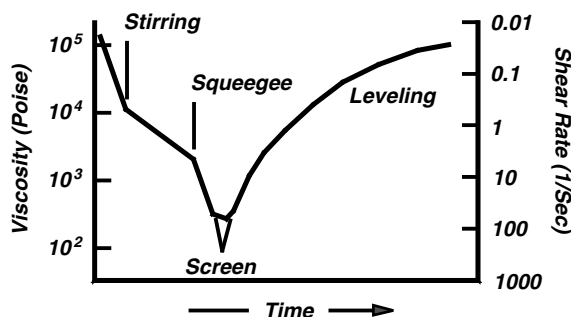
FIGURE 5.13
Viscosity vs. time during the printing process.

in viscosity to enable flow. After the print, sufficient time must be allowed for the paste to increase to nearly the rest viscosity (leveling). If the paste is placed in the drying cycle prior to leveling, the paste will become still thinner because of the increased temperature, and the printed film will lose line definition.

Viscosity can be lowered (by addition of the solvent) or increased (by addition of a thixotropic nonvolatile vehicle), although the latter will require remilling of the paste. It is important to note that a little of the thinner goes a very long way. Three or four drops in a 50-g jar of paste can cause the viscosity to drop by several orders of magnitude.

The measurement of viscosity, in principle, is simple. A force is applied to the paste, and the rate of flow is measured. In practice, however, the problem is very complex in that the viscosity reading is dependent on a number of variables, some of which interact. For example, the viscosity of most liquids is highly dependent on temperature (e.g., molasses in January). The viscosity is also highly dependent on the boundary conditions. Under the same set of parameters, the reading obtained in a large container may vary by orders of magnitude from one obtained in a small container. An added degree of complication is that the cost of the instrument used to obtain the curve pictured in Figure 5.11 is usually prohibitive for most thick-film manufacturing facilities [27].

Two types of viscometers are used to measure viscosity in a manufacturing environment, the cone-and-plate and the spindle. The cone-and-plate uses a rotating cylinder milled to a specific angle plunged into a sample of the material to be measured on a flat plate. The viscometer fundamentally measures the torque required to turn the cone at a constant velocity and converts these figures into a viscosity reading. For purposes of measuring the viscosity of thick-film pastes, the most common instrument is the spindle. A cylinder of known volume is filled with thick-film paste, and a spindle of known size is rotated inside the cylinder. The same parameters are measured and converted to viscosity. The spindle method is generally more accurate because a known volume of paste, with known boundary conditions, is used as a

basis for measurement. In addition, the cylinder can be fitted with a water jacket to control the temperature of the paste, thereby improving the repeatability of the data [28].

Viscometers of this type can generally measure the viscosity at one or two points. Referring to Figure 5.11 it is apparent that an infinite number of curves can be drawn through two points. At best, the viscosity reading can only be used to correlate two pastes or to correlate one paste with a previous reading. It is important to understand that viscometer readings cannot be directly translated into printer settings to achieve a desired result. This is not to say that viscosity readings are not important. In fact, they are one of the most important process controls available to the thick-film process engineer, if they are used in the proper manner. To be useful, the following precautions should be observed:

1. Use the same viscometer and spindle that the manufacturer uses so that results can be correlated. It is extremely difficult to compare readings taken under one set of conditions with another.
2. Always measure the viscosity at the same temperature, using a water bath if necessary.
3. Always use the same volume of paste in the cylinder.
4. Obtain a standard fluid of known viscosity from the paste vendor to calibrate the viscometer.

Another important use of the viscometer is in controlling the paste-thinning process. From time to time, it is necessary to add thinner to the paste to replace that portion lost to evaporation. If the viscosity is measured at incoming inspection and recorded as part of the acceptance process, it is a relatively simple process to add sufficient thinner to return it to the original viscosity.

Referring to Figure 5.14, the viscosity of a typical thick-film paste designed for general purpose use is about 200,000 cp as measured with a #2 spindle at room temperature. Pastes designed for very fine-line printing may have a viscosity twice that value, and pastes designed for through-hole printing may be 75% lower. When specifying the proper viscosity for a paste, it is critical that the application must be considered if optimum results are to be obtained.

5.6 The Squeegee

The purpose of the squeegee is to force the paste through the screen onto the substrate. It is formed of a flexible material such as polyurethane or neoprene and comes in two basic shapes, diamond, and trailing edge, as
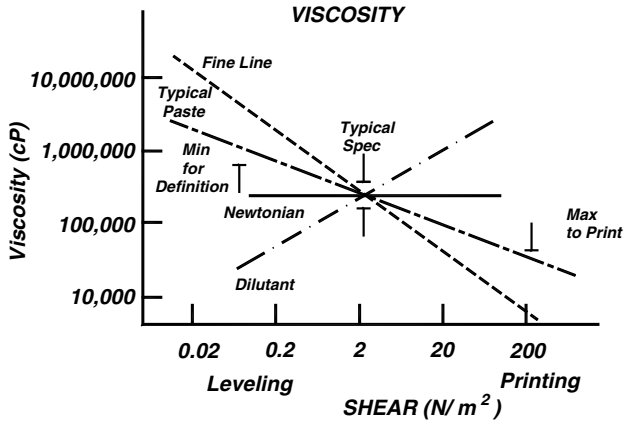
FIGURE 5.14
Viscosity for different applications squeegee shapes.

TABLE 5.2

Hardness for Commonly Used
Thick Film Squeegees

Hardness	Color	Comments
60–65 Shore	Red	Very soft
70–75 Shore	Green	Soft
80–85 Shore	Blue	Hard
90+ Shore	White	Very hard

shown in Figure 5.15. The diamond squeegee comes in strips and is about 10 mm on a side, whereas the trailing-edge squeegee is about 10 mm thick.

Squeegees are available in a range of durometers as given in Table 5.2 [2]. Soft squeegees comply better with irregular or warped substrates and are used in applications where high conformance is required. The trailing-edge squeegee is more compliant than a diamond squeegee for the same durometer.

For solder printing, metal squeegees are often used because of their increased wear-resistant capability. These are made from stainless steel or nickel.

5.7   The Printing Process

There are two basic methods of screen printing; the contact process and the off-contact process. In the contact process, the screen remains in contact with the substrate during the print cycle and then is separated abruptly by either

Diamond

Trailing Edge
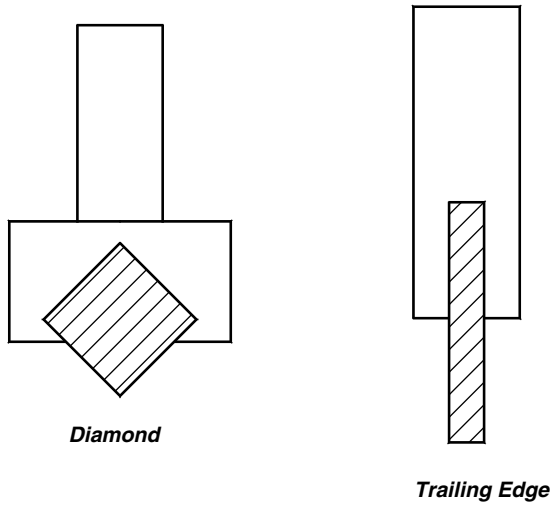
FIGURE 5.15
Squeegee shapes.

lowering the substrate or raising the screen. In the off-contact process, the screen is separated from the substrate by a small distance and is stretched by the squeegee until it contacts the substrate only at a point directly under the squeegee. Once the squeegee passes, the screen snaps back, leaving the paste on the substrate. In general, the best line definition is obtained with the off-contact process and most printing of thick-film pastes is performed in this manner. The contact process is generally used when a stencil is used to print solder paste. The stencil, being solid metal, cannot be continually stretched in the same manner as a screen, without permanent deformation.

In the printing process, the paste is applied to the screen and the squeegee is activated, sweeping across the screen at a predetermined velocity as depicted in Figure 5.16a and Figure 5.16b. The pressure from the squeegee forces the paste through the openings in the screen onto the substrate. The rough substrate surface creates somewhat more surface tension than does the smooth wires of the screen mesh, causing the paste to stay on the substrate when the squeegee passes. The process is facilitated by the thixotropic nature of the paste. As the squeegee applies force to the paste, it becomes thinner and flows more readily. As the squeegee passes, the paste becomes thicker again and retains the line definition on the substrate.

There are several models of the screen-printing process. One depicts screen printing as a simple mechanical process, as shown in Figure 5.17, by which the force of the squeegee fills the openings in the screen with paste and forces the paste into contact with the substrate, where it is transferred to the substrate by surface tension. Another model, depicted in Figure 5.18, describes the printing process as a hydrodynamic one whereby the squeegee shears the paste off at the surface of the screen while forcing it into contact with
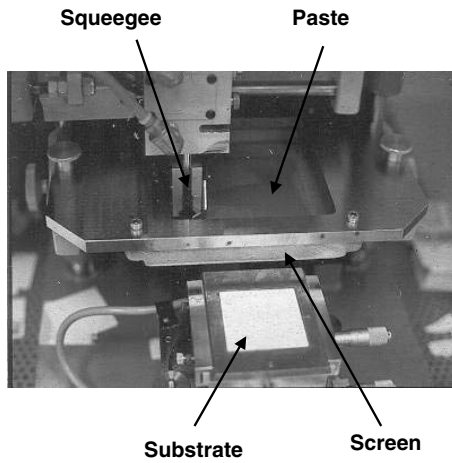
FIGURE 5.16A
Relative positions of substrate, paste, squeegee, and screen prior to printing.
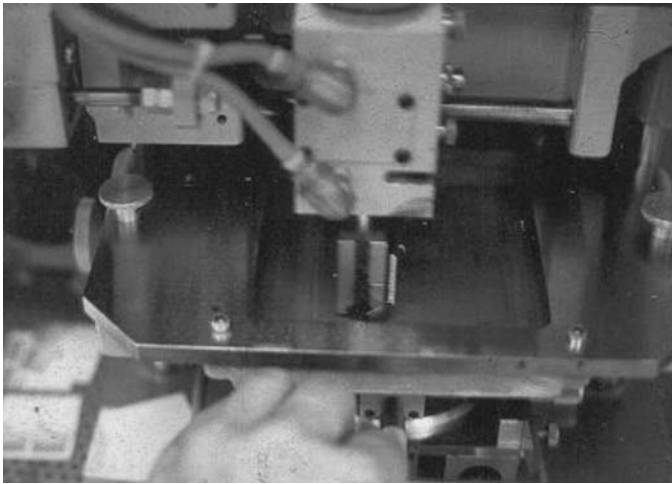
FIGURE 5.16B
Squeegee action after printer activation.

the substrate, where the paste is transferred as described earlier. There have been books and papers written about which is the more accurate and useful. Ultimately, however, it is the skill and experience of the process engineer that determines the success of the screen-printing operation.
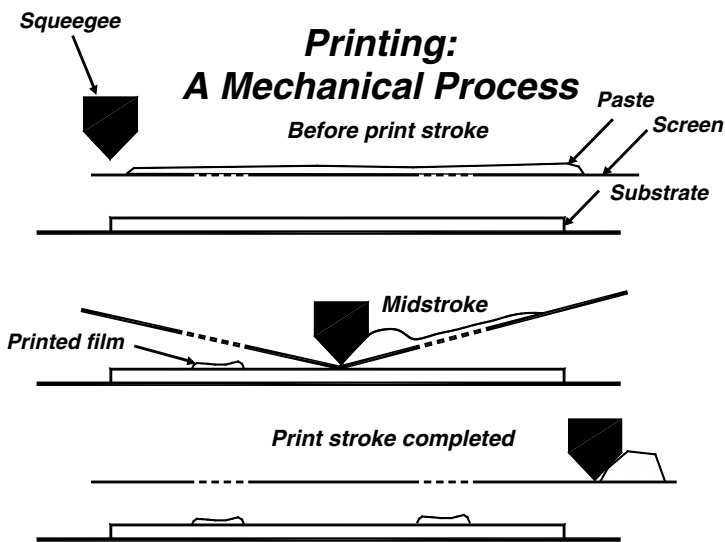
FIGURE 5.17
Printing as a mechanical process.
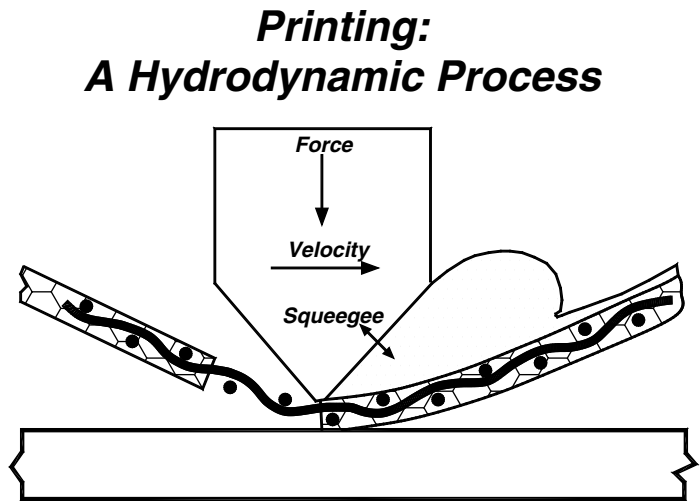
FIGURE 5.18
Printing as a hydrodynamic process.

5.8   Screen Printer Setup and Operation

Over 100 variables have been identified that affect the screen-printing pro-
cess, ranging from the paste properties to the printer setup to the screen
properties. Only a few of these are within the control of the process engineer.
Adjustments in these parameters can compensate for most of the remainder.

5.8.1   Screen-to-Substrate Spacing: The Snap-Off Distance

In the off-contact printing process, this is arguably the most important para-
meter in the screen printer setup. If it is too large, the screen will rapidly
lose tension and the print will lose definition. If it is too small, the tension
on the screen during the print will not be sufficient to transfer the paste to
the substrate. Referring to Figure 5.19, the magnitude of snap-off is depen-
dent on the size of the screen, with a ratio of maximum screen dimension
to snap-off of 200:1. A list of typical snap-off distances for a sample of
standard-size screens is shown in Table 5.3.
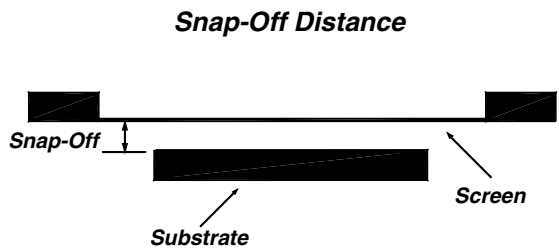
FIGURE 5.19
Snap-off distance.

TABLE 5.3

Snap-Off Distance for Common
Screen Sizes

Screen Size (in.²)	Snap-Off Distance (in.)
5 × 5	0.025
5 × 7	0.035
8 × 10	0.050

5.8.2 The Screen-to-Substrate Parallelism

If the screen is not exactly parallel to the substrate, the snap-off distance will change across the print, causing variability in the print definition and thickness.

5.8.3 Squeegee Velocity

The squeegee velocity not only applies pressure primarily in the tangential direction, but also in the normal direction. If the squeegee speed is too fast, the print definition may be poor because of voiding. If the viscosity of the paste is not allowed sufficient time to drop to the proper value, insufficient paste may be transferred and the print will be thinner than normal. If the velocity is increased past this point, the squeegee will begin to plane over the paste instead of sweeping it along the surface of the screen, and the print will become thicker. If the speed is too slow, the paste may not be properly sheared, and the print may be too thick. In addition, the process time increases with an increase in cost due to the subsequent drop in throughput.

5.8.4 Squeegee Position

The deflection of the squeegee during the printing cycle creates a downward pressure on the paste. If the squeegee is too high, the print will be thin and/or may contain voids. If the squeegee is too low, excessive pressure will be applied to the paste, causing the print to be too thin, possibly forcing paste between the screen and the substrate with a corresponding loss of print definition.

5.8.5 Squeegee Pressure

Squeegee pressure is applied by a spring force that pushes the squeegee downward toward the substrate and is set by adding tension to the spring. The squeegee pressure is most significant when printing with a highly viscous paste. If the pressure is too low in this case, the squeegee may plane on the paste resulting in a thick print with poor definition.

5.8.6 Attack Angle

The attack angle is a measure of the degree to which the squeegee is tilted with respect to the normal as shown in Figure 5.20. A high degree of tilt will have the same effect as increased squeegee pressure or having the squeegee set too low.

Attack Angle

Print Thickness:
$t_{30°} > t_{45°} > t_{60°}$
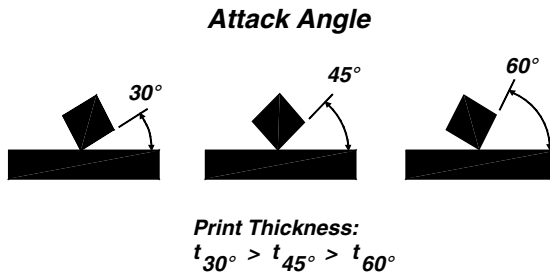
FIGURE 5.20
Squeegee attack angle.

5.9   Screen Printer Setup

This generalized procedure for setting up a screen printer is applicable to most printers and should be executed in sequence. In general, it is important to remember that any adjustment that causes an increase in tangential force will tend to produce a thinner print, and any adjustment that causes an increase in normal force will tend to produce a thicker print. The procedure description follows:

1. With the screen removed, install the squeegee and place a substrate on the platen. Lower the squeegee to the point where it just touches the substrate and adjust it so that it is parallel to the substrate. With the squeegee just touching the substrate, lower it another 3–5 mil. Referring to Figure 5.21, if the squeegee is set too low, it will have a detrimental effect on the print quality and will result in damage to the screen.

2. Set a reference level on the platen using a three-point position indicator. Install the screen and check the parallelism of the screen using the position indicator. If the screen is not parallel, make the appropriate adjustments.

3. Lower the screen to the point where it is just touching the substrate and set a reference level of "0" on the screen position indicator. Set the screen-to-substrate spacing as determined from Table 5.3.

4. Place a substrate on the platen and visually align the substrate to the pattern on the screen (if the printer does not have a vision system).

5. Apply paste to the screen and adjust the velocity and alignment of the print as necessary to optimize the definition and thickness of the print. The squeegee pressure adjustment should be used as a fine control.

Downstop

Correct

0.003" – 0.005"

Incorrect

PROBLEMS:
- **Coining**
- **Stretching**
- **Puncture**
- **Poor Resolution**
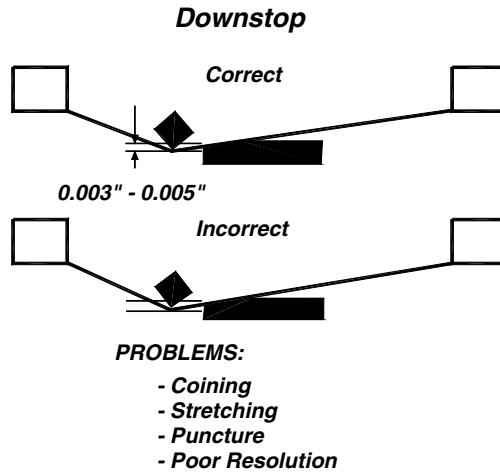
FIGURE 5.21
Squeegee setup position.

This procedure should result in a print that is nearly optimum with a minimum of time. The squeegee speed and squeegee pressure can be used to fine-tune the process if necessary.

5.10 Geometric Effects on Print Thickness

In theory, the wet thickness of a print may be increased indefinitely by simply increasing the emulsion thickness. For smaller openings, this is largely true. The volume created by the screen mesh and the squeegee in tandem fills with paste, and the shape of the print is somewhat flat. As the size of the opening increases, however, the screen can be deflected as a result of squeegee pressure and the profile of the printed film becomes concave. If the size of the opening is sufficiently large so that the screen can be deflected to the point where it is able to touch the substrate, the emulsion thickness becomes less of a factor, and the print thickness is largely determined by the screen mesh. A thicker emulsion in this case simply results in a more pronounced concave effect. The size of the opening where this phenomenon occurs depends on the mesh count and the size of the wire.

Referring to Figure 5.22, the wet print thickness may be estimated by noting that the initial print is in the form of a number of rectangular solids, with a height equal to the sum of the emulsion buildup plus the screen thickness, and an area equal to the area of the mesh opening. The paste will spread out to fill in the gaps, and the overall print will be thinner than the height of the rectangular solid.
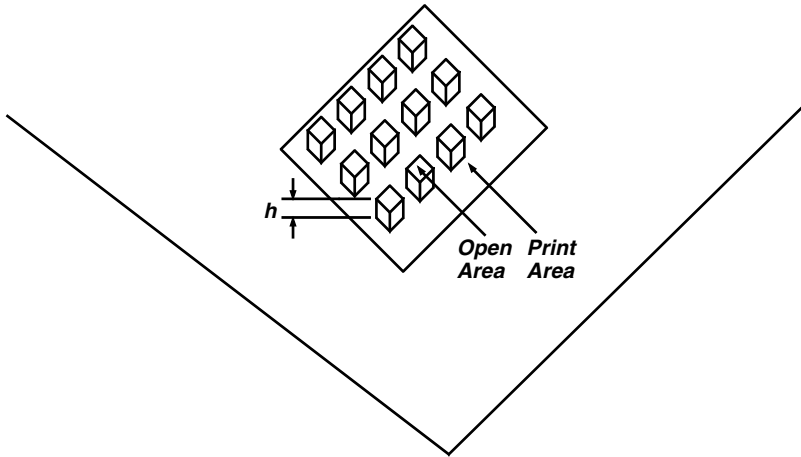
FIGURE 5.22
Determining print thickness.

$$\text{Wet print thickness} = \left(\text{Emulsion buildup} + \text{Screen thickness}\right)$$

$$\times \text{ Percentage open area.} \tag{5.8}$$

Assume that a 325 mesh screen with a wire diameter of 0.0011 in., a height of 0.0025 in., and an emulsion buildup of 0.001 in. is used to print a pattern on a substrate. What will be the average wet thickness of the print?

From Table 5.1, the open area of the screen is 41.3% of the overall area. The average wet-print thickness is:

$$Wet\ print\ thickness = \left(0.001 + 0.003\right) \times \left(0.413\right) = 0.00136\ in.$$

5.11 Measurement of Print Thickness

There are two basic approaches to measuring print thickness; off-contact and contact. Off-contact systems may be used to measure wet, dry, or fired films, whereas contact systems may only be used on dry or fired films. The simplest noncontact method is to focus a high-powered metallurgical microscope with a narrow depth of field on the substrate, mark a reference, and refocus the microscope on the top of the film. The print thickness is the distance the object lens must be moved. This method is somewhat inaccurate as the profile of the print is nonuniform, allowing the thickness to vary considerably across the print.

Another method of off-contact thickness measurement uses light to determine the profile. The light-section microscope employs a split coherent light beam shined directly on a print. The interference pattern of the beam outlines the print, and the thickness is measured by noting the distance between the lines marking the substrate and the top of the print. Although substantially more accurate than the metallurgical microscope, the light-section microscope is highly operator dependent and does not produce a written record of the measurement.

More sophisticated off-contact systems have a *laser* that sweeps across the film, with the reflection picked up by a light detector. The profile is integrated by the system to determine the mean thickness. Either the exact profile or the mean thickness of the print may be used as a basis of comparison with other prints.

Contact systems use a *stylus* that moves across the film at a selected rate of speed. The position of the stylus is detected, and the profile may be plotted as the stylus moves. These can be quite sensitive when the profilometer is placed on a steady table and shielded from air currents. Contact systems may only be used on dried and fired prints. The output from these systems may be plotted graphically or may also be integrated, as for the laser, to provide a mean thickness.

5.12 Printing Considerations and Problems

Successful screen printing begins with a stable printer setup that comprises the following:

- Proper screen mesh and emulsion for desired thickness
- Correct downstop for extended screen life
- Minimum squeegee pressure and speed suitable for paste and pattern
- Proper snap off to insure peel without screen stretch
- Proper flooding to prevent starved prints
- Print registration centered

There are numerous problems that can occur during printing, including:

- Wrong thickness — print too thick or too thin
- Scalloped edges — line definition poor, not straight
- Print voids — incomplete pattern
- Alignment — poor alignment on substrate or between prints

- Resolution — print geometry does not match the layout
- Bleedout — print spreading

If the setup procedures are followed, problems should be at a minimum. However, given the number of variables, it is inevitable that the printing parameters will drift over a period of time. The principles in this section will help to keep the printed patterns within specifications.

5.12.1   Print Resolution

Poor print resolution simply means that the printed film does not match the layout in terms of dimensions or shape. It can be because of spreading of the print because of improper rheology, or a flaw in the screen. These factors help to improve resolution of the pattern [29–31]:

- Emulsion thickness — thinner emulsion is better.
- Pattern alignment to wire mesh — 45° is optimum.
- Attack angle — shallow attack angle is better.
- Durometer — softer durometer is better.
- Speed — slower speed is better.
- Downstop — smaller downstop is better.
- Alignment — tighter alignment is better.
- Rheology — high viscosity is better.
- Pressure — lower pressure is better.
- Screen tension — degrading of tension worsens resolution.

5.12.2   Effect of Screen Parameters on Print Parameters

The screen has a profound effect on both the print thickness and definition. Some characteristics of the screen include:

- A higher mesh count will produce a thinner print.
- A higher mesh count will produce a print with better definition.
- A screen with a 45° mesh will produce a print with better definition.
- A screen with a thinner emulsion will produce a print with higher definition.

Typical applications of different screen meshes include:

- 400 Mesh — printing lines 0.005 in. wide and lower
- 325 Mesh — ordinary conductors and multilayer dielectric materials
- 200 Mesh — resistors
- 80 Mesh — solder [32]

5.12.3   Factors that Affect Print Thickness

There are many factors that affect the thickness of a printed film. The most critical are listed as follows [33]:

- Screen mesh count
- Attack angle
- Durometer
- Pressure
- Speed
- Emulsion
- Snap-off
- Downstop
- Percentage solids content of paste

For prints that are too thick, the parameters that should be checked first include:

- Incorrect downstop setting
- Squeegee too hard
- Paste behind squeegee
- Squeegee pressure too high
- Attack angle too low
- Snap-off distance too high
- Too much paste on screen

For prints that are too thin:

- Incorrect choice of screen mesh
- Squeegee speed too high
- Paste viscosity too low
- Angle of attack too high

For prints that show uneven print thickness:

- Screen/squeegee/substrate not parallel
Variation in squeegee speed
Screen tension too low
Snap-off too low
Squeegee lifting too soon
- Down pressure too low [34]

5.12.4 Preventing Pinholes and Voids during Printing

Pinholes and voids, although seem innocuous, can create insidious problems such as the following, after firing.

- Resistor values will have a wider spread
- Bonding pads may be disturbed
- Conductor traces will carry less current

To minimize this problem:

- Maintain a clean, dust-free atmosphere in the printing area.
- Control temperature in the printing room (20–25°C).
- Adjust screen tension and snap-off distance to obtain screen release over the entire screen area.
- Use soft squeegees (40–60 durometer) with small attack angle.
- Keep squeegee pressure at a minimum.
- Use flood bar to assure adequate paste supply.
- Use soft, lint-free wipes for cleaning the screen during printing.
- Use locking fixtures to keep printing parameters at set point.
- Maintain uniform printing speed and print rate.
- Avoid extended interruption in printing to prevent microscopic particles of dried ink.

5.12.5 Good Practices

Some good practices to follow in a printing environment are:

- Avoid excessive wiping of the screen. This will stretch the screen and may introduce contaminants into the paste.
- Avoid wiping screen with solvent at all times. A few drops of solvent can lower the viscosity by several orders of magnitude.
- Cleanliness is essential. This cannot be overemphasized. A few particles of dust in a jar of thick-film paste will create agglomerates and may ruin the entire jar. Further, particles of dust and hair may burn out during firing, leaving voids that are not visible after the printing process
- Avoid allowing paste to dry in screen. This will clog the screen and introduce particles into the paste when it is returned to the jar.
- Avoid overworking paste. This will cause the solvent to evaporate, increasing the viscosity, and causing the paste to dry out. Also,

excessively working the paste without allowing time for the viscosity to recover will lower the viscosity.

5.13 Inspecting Printed Films

Inspection is an integral part of the screen-printing process, particularly where complex multilayer circuits are involved. A single void, anywhere in any trace or in any layer, can result in the entire structure being scrapped.

Inspecting printed films in the wet state is somewhat difficult because of the high reflectivity of the film. In the dry or fired state, inspection is easier as there is more of a contrast with the substrate. For laboratory or small manufacturing operations, a microscope with backlighting is an essential tool. It is very easy to see voids or thin areas because alumina and beryllia are translucent to a certain degree. However, for multilayer applications or thicker substrates, this method is inadequate, and one must revert to inspection using top lighting.

As circuits become more and more complex, machine vision will be the only method that is viable. Present day technology allows inspection under nonuniform lighting conditions that can detect circuit traces or flaws as small as 0.001 in. It is anticipated that machine vision will be the method of choice in the near future [35].

Glossary of Terms

Attack angle	Angle between squeegee and substrate surface
Downstop	Mechanical limit to squeegee travel
Durometer	Hardness of squeegee
Emulsion	Photosensitive material
Flood	Spread of paste over screen prior to printing
Mesh count	Wires per inch
Open area	Area of the screen opening
Peel	Release of screen from paste print
Snap-off	Distance between screen and substrate surface
Squeegee travel	Length of print stroke

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6

Multilayer Ceramics

Fred Barlow, Aicha Elshabini, and Arne K. Knudsen

CONTENTS

6.1   Introduction

Multilayer ceramics represent a number of technologies that are capable of producing high-density electronic substrates with highly desirable properties. The benefits of this technology include low electrical losses, very high interconnect density, stability at high temperatures, and the ability to easily include three-dimensional structures such as inductors and microelectromechanical system (MEMS) devices. In addition, these materials can be intrinsically hermetic in nature and offer thermal conductivities as much as 100 times greater than traditional polymeric substrates.

The development of multilayer ceramics was first demonstrated in the preparation of capacitors in the late 1940s [1]. Over the following 10 years, the techniques necessary to produce multilayer high-temperature cofired ceramics (HTCC) substrates [2] were developed at American Lava and RCA, culminating in the first comprehensive description of this technology in 1961 [3]. IBM was one of the first adopters of this technology, describing the development of multilayer packages for microprocessor applications in 1967 [4]. Today, multilayer ceramics are manufactured in a number of locations, although high volume production is dominated by companies with their headquarters in Japan, such as Kyocera and NTK. This technology has been used and is still in use for a wide range of single-chip packaging solutions as well as for multilayer substrates used in high-density electronic modules.

6.1.1   High-Temperature Cofired Ceramics

HTCC is an all-inclusive term to describe ceramic substrates that are consolidated at temperatures above about 1000°C. Applied to electronic packaging, this descriptor includes aluminum oxide, aluminum nitride (AlN), and a variety of other developmental or seldom-used materials. Until recently, discriminating between HTCC and low-temperature cofired ceramics (LTCC) was elementary, as the firing temperatures differed by roughly 600°C. To confound that difference, an intermediate-firing multilayer ceramic, or medium-temperature cofired ceramic (MTCC), has recently been introduced. Details on the processing and properties of this material will be discussed in Section 6.2 and Section 6.4.

The HTCC manufacturing process can be described in generic terms although the specific processes often must be adapted for each material. For example, AlN, and even LTCC tape, is processed much like aluminum oxide tape. The firing conditions (binder burnout, atmosphere, furnaces, etc.), however, are quite different. The generic multilayer ceramic production process is depicted in Figure 6.1. In high volume, most of these processes are automated and as such represent a significant capital investment. Small production facilities often adopt more modest equipment, much of which can be purchased from commercial equipment vendors. High-volume, low-cost production, however, requires significant investments and know-how to couple the "art" involved in producing high-quality packages with automated manufacturing and inspection.

6.1.2 Low-Temperature Cofired Ceramics

An extension of this technology is LTCC. LTCC was developed in the early 1980s, in part for applications that suffered from the high conduction loss of HTCC products [5–9]. Engineers found HTCC very attractive for a number of reasons; however, some applications were hard pressed to be implemented in this technology owing to the intrinsically low conductivity of conductors that are able to withstand the high firing temperatures that HTCC requires. LTCC was in some ways an improvement over HTCC in that the reduced firing temperature, ~850°C, allows for the incorporation of nonrefractory metals such as silver, gold, and copper. These materials offer far superior electrical conductivities, and therefore LTCC can, in general, offer superior electrical performance in comparison to HTCC. However, this improvement is not without its limitations, in that LTCC materials are glass–ceramic compositions with inferior mechanical and thermal properties when compared to HTCC. This reduced strength and reduced thermal performance are intrinsically tied to the compositions of the crystallizable LTCC materials or the sintering adds that are added to the alumina–glass LTCC composites. As a result, a trade-off is required to select the material that best matches the requirements of a given application.

HTCC and LTCC offer a number of compelling advantages over traditional thick-film, organic, and other packaging options. In general, HTCC substrates exhibit high mechanical strength, high thermal conductivity, consistent and attractive electrical performance, hermeticity, refractory metallization, and reliable brazing technologies. LTCC offers many of the same features but with reduced mechanical properties and improved electrical properties [10]. With a mature manufacturing technology, HTCC alumina and LTCC represent established and dependable technologies for multilayer packages.
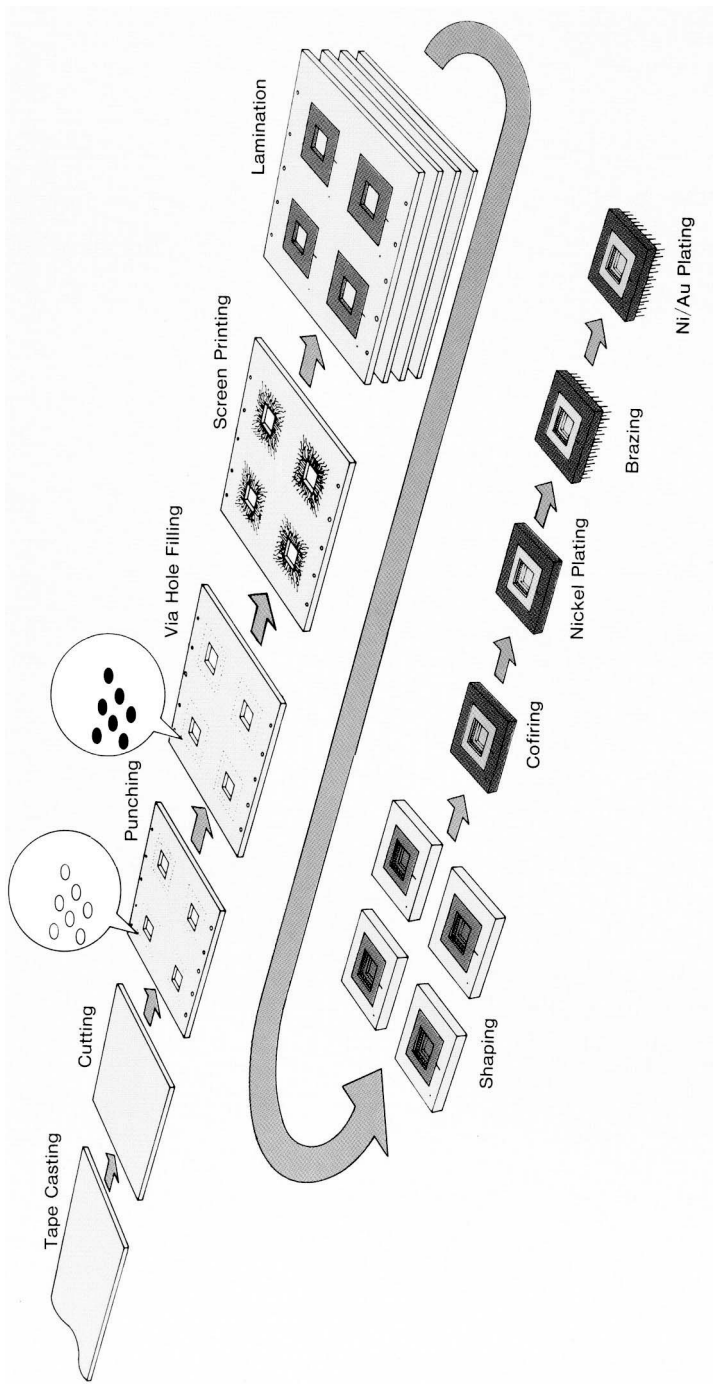
FIGURE 6.1
Production process for multilayer ceramics.

6.2   The Multilayer Ceramic Process

The multilayer ceramic process is fundamentally a parallel process in which each layer is fabricated separately and then combined to form a substrate. As illustrated in Figure 6.1, each layer begins its life as a roll of glass and/ or ceramic particles in a polymer matrix that has been tape-cast to a particular thickness on a plastic film. Depending on the foundry, this roll of material is blanked into individual tape sheets ranging in size from 75-mm (~3-in.) square to 200-mm (~ 8-in.) square. A substrate is then fabricated using 6 to 50 sheets of this material, depending on the complexity and thickness required for the final product. Generally, each tape layer contains a unique set of printed electrical traces on its surface, as well as electrically conductive holes (called *vias*) through that given layer. Through careful design of this combination of layers, traces, and vias, a three-dimensional block of ceramic is created with embedded electrical circuitry.

As shown in Figure 6.1, after blanking the tape to size, each layer is punched or laser-cut to form the vias and any desired cavities. The vias are filled with a conductive ink. Each layer is submitted to a screen-printing process to create the interconnects on the surface of the tape layers. At this point in the process, the layers are stacked up and aligned to each other. Once aligned, the assembly is laminated to bond the polymer components of adjacent layers. This stack of layers is still a flexible substrate that contains significant amounts of polymeric material. This polymeric component is burned off in a furnace as the first step in a firing cycle. The polymer component is converted to gas and vented from the furnace, leaving behind only the ceramic or glass as well as the metal traces and vias. This assembly is fired to sinter the ceramic or glass into a dense ceramic body that contains the desired metal interconnections. Each step of this process will be discussed in great detail in the following sections.

6.2.1   Tape Handling and Clean Room Environment

Multilayer ceramic tapes use many of the traditional processes that have been used for more than 50 years to produce thick-film circuits and components [11–13]. However, some special handling requirements are needed to deal with the tape layers while in the green unfired state. This requirement is because of the fragile nature of the tape layers in comparison to traditional thick-film prefired ceramics as well as the fact that the unfired tape layers are made flexible through the use of a polymer matrix. This polymeric portion of the tape can absorb moisture and therefore expand and contract with changes in humidity and temperature. As a result, control of the process environment as well as handling of the tape layers are key issues. The five general areas of concern are humidity control, temperature control, reduction

of particulate matter, and static control, as well as support and handling of the fragile tape layers.

Particulate control is generally handled using traditional clean room practices that include the use of air filtration systems to isolate and remove particulate matter from the air in the manufacturing environment as well through minimizing the amount of particulate matter that is introduced by personnel and production processes. This is important because any contamination, such as large particles of dust or fibers from clothing will generally burn out during the firing phase of the ceramic process, leaving behind an undesirable void and perhaps an electrical defect. Clean rooms are generally rated in terms of the number of particles larger than 0.5 µm that are allowed in a cubic foot of air within the room. These ratings range from class 10 to class 100,000 with the higher numbers indicative of higher particle counts. For example, a class 1000 clean room would be allowed to have no more than 1000 particles larger than 0.5 µm per cubic foot in any given sample of air taken from that room. As the features employed in most multilayer ceramic circuits are generally 25 µm or larger, ultra clean rooms such as those found in semiconductor device fabrication facilities are not required. Class 1000 or class 10,000 is generally adequate.

People are the greatest source of contamination introduced in a clean room environment and as a result clean room smocks, shoe covers, gloves, hairnets and, in some cases, face masks are employed to minimize the introduction of particles into the facility. Some of the processes employed in multilayer ceramic processing also generate particulate matter such as via punching. Care must be taken to remove these particles and clean the tape layers as necessary. Rollers coated with sticky adhesive are one popular way to collect these particles, as are vacuum systems. The adhesives on the sticky roller are just strong enough to retain loose particles without damaging or adhering to the tape layers or other surfaces.

Humidity control is important to preserve the stability of the tape layers prior to firing. The polymers that compose the binder in many tape systems are somewhat hydroscopic in nature and tend to absorb moisture. As they absorb moisture or release moisture in a very dry atmospheric condition, they tend to expand or contract slightly. For large feature sizes, this effect may be negligible; however, for fine features and tight layer-to-layer tolerances this effect can diminish yields. Generally, this problem is dealt with through adequate heating and ventilation systems that include humidifiers and dehumidifiers to control the natural humidity fluctuations from season to season. These systems also control the facilities temperature that can be critical to paste viscosity as well as the stability of the individual tape layers. As the viscosities of most via-fill and printed metallization inks are a strong function of the temperature, large variations in the temperature can affect print thickness and print resolution, as well as via-fill quality.

Static electricity can also create problems for some tape-handling systems. Whereas the substrates themselves are not static sensitive, such as in the case of many semiconductor devices, static can create undesired adhesion

between tape layers and plastic carrier layers. Generally, static can be controlled through proper humidity control and, in some cases, may require ionizing equipment and proper equipment grounding.

Tape handling is also an important aspect of the facilities used to produce multilayer thick-film circuits and packages. This problem is fundamentally different from prefired ceramics because, during most of the processing steps, the layers are flexible in nature. Two primary methods are used to handle tape layers: flexible plastic backing materials and metal frames. Both methods constrain the tape layers to prevent expansion and contraction during processing, as well as provide a mechanism for handling the fragile tape layers. It has been shown [14] that expansion and contraction can occur in unconstrained tape layers through various process steps. This effect is illustrated in Figure 6.2, in which the expansion or contraction of individual tape layers was recorded as the tape layers progressed through the substrate fabrication process flow. Note that the deviation from the initial dimension (150 mm) was less than 1 mil (25 µm) as long as the tape was constrained by the plastic film. Once the tape layer is removed from the carrier, as much as 2 to 3 mil of deviation was observed.

The use of frames, sometimes referred to as *framing*, allows for thin sheets of metal to constrain and support the tape layers. The frames are generally fabricated from thin stainless steel, nominally ~5 mil thick, with windows cut to the size of the blank tape format. Generally, these windows have a
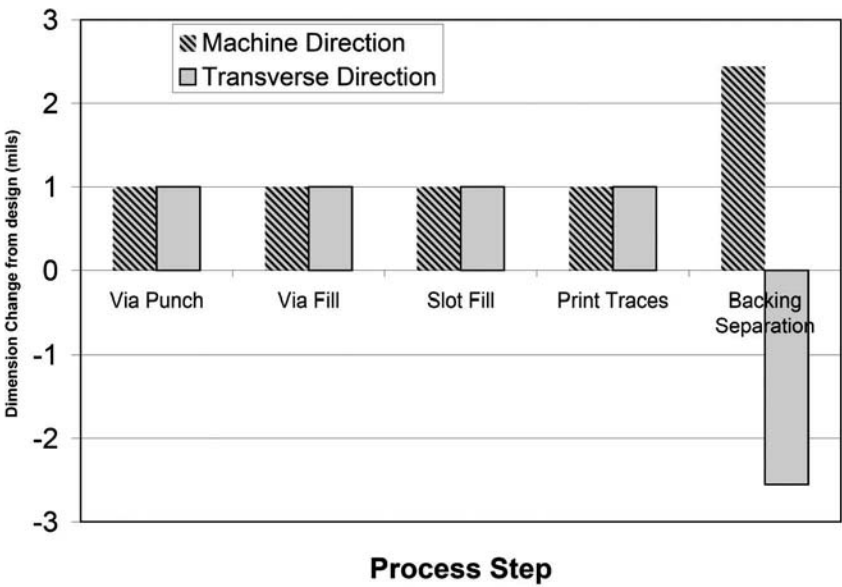
FIGURE 6.2
Dimensional change of LTCC samples as a function of the process including plastic carrier film separation.
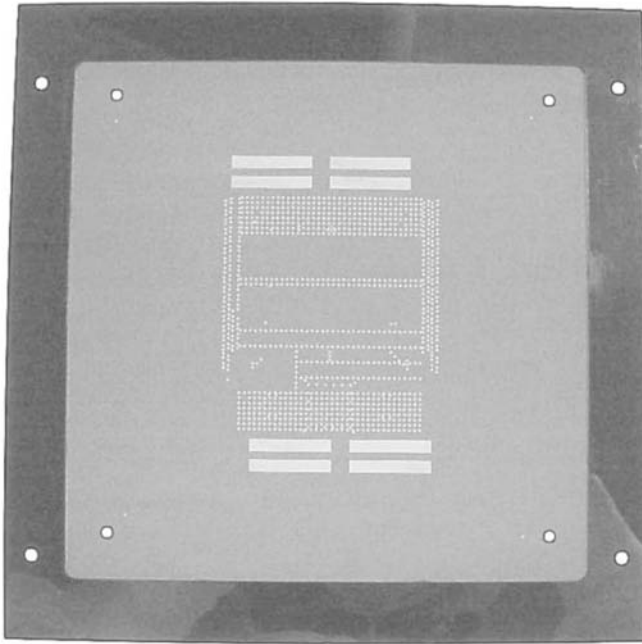
FIGURE 6.3
A framed piece of Dupont 951 LTCC after the via punch process. The holes in the tape, as well as in the stainless steel frame, are commonly used for registration of layers.

small recessed ledge that allows the tape layer to sit in with its surface flush to that of the metal frame, as illustrated in Figure 6.3. The tape layers are normally secured to the frame with adhesive or tape that effectively destroys the utility of the outer edge of the tape layer. This portion of the tape layer is cut away during the final processing steps to release the tape layer from the frame. The frames can then be reused.

Metal frames are sometimes also equipped with alignment holes that allow them to be precisely aligned within various pieces of equipment throughout the fabrication process. In some cases, alignment holes are not included, and machine vision systems are used instead to align printed features on the tape layer itself. The primary function of the frame is to facilitate handling as well as prevent the expansion and contraction of the unfired ceramic tape layers. Handling is enabled by a segment of frame material that extends out beyond the tape layer. The mechanical stability of the tape layer is retained because the metal frame does not expand and contract in response to moisture absorption or process operations.

Metal frames, though useful in many situations, can also create problems, particularly when used with thin tape layers. Also, an additional process step is needed to bond the tape to the frame, and the frames must be cleaned in order to be reused. For very thin tape layers, the frame must stretch the tape to control the expansion and contraction of a given layer throughout

the process steps required to produce a substrate. This tension often causes cracking or tearing in these thin tape layers. As thin tape layers (for example, DuPont 943C2, which has a 51-μm green thickness) are growing in popularity, many manufacturers are handling tape on plastic-film backing. These sheets of backing film come with the tape sheet, generally precut to the desired size, and are designed to offer low puncture resistance for high-speed via formation, stability, and support for the thin tape layers. Figure 6.4 illustrates a sheet of LTCC adhered to a sheet of carrier film prior to processing. In highly automated systems, vacuum is used to pick up and manipulate these unfired sheets of tape with the attached backing material.

6.2.2 Tape Casting

The first step in the production of multilayer ceramics — LTCC, MTCC, or HTCC — involves the casting of a thin ceramic–organic composite tape. There are a number of key parameters associated with the casting of these tapes [15]. They include:

- Composition
- Selection of powders
- Polymers and additives
- Mixing and milling
- Casting
- Inspection, quality control
- Tape handling

Ceramic substrates are typically composites of crystalline and noncrystalline phases. The composition of the substrate is, of course, a function of the inorganic (and organic) components incorporated as raw materials. Alumina multilayer ceramics are produced from mixtures of powders with controlled purity, homogeneity, surface and bulk chemistry and crystallography, particle size and particle size distribution, surface area and morphology, including agglomeration [16].

The earliest HTCC structures were produced using 92% alumina [17]. Today, this composition remains a "workhorse" material. As shown in Table 6.1, there is a variety of Al_2O_3 formulations in commercial production. Manufacturers tend to maintain some secrecy as to the specific ingredients; however, in addition to purity, the color of alumina ceramics is a distinguishing characteristic. Kyocera's "black" ceramic (90%) is actually a deep-red composition resulting from the inclusion of a small amount of Cr_2O_3. Other additives (W, Mo, and Ti) have also been included in HTCC to darken the ceramic. This opacification has no functional benefit although it eliminates the visibility of subsurface metallization. Ceramic vendors introduced this
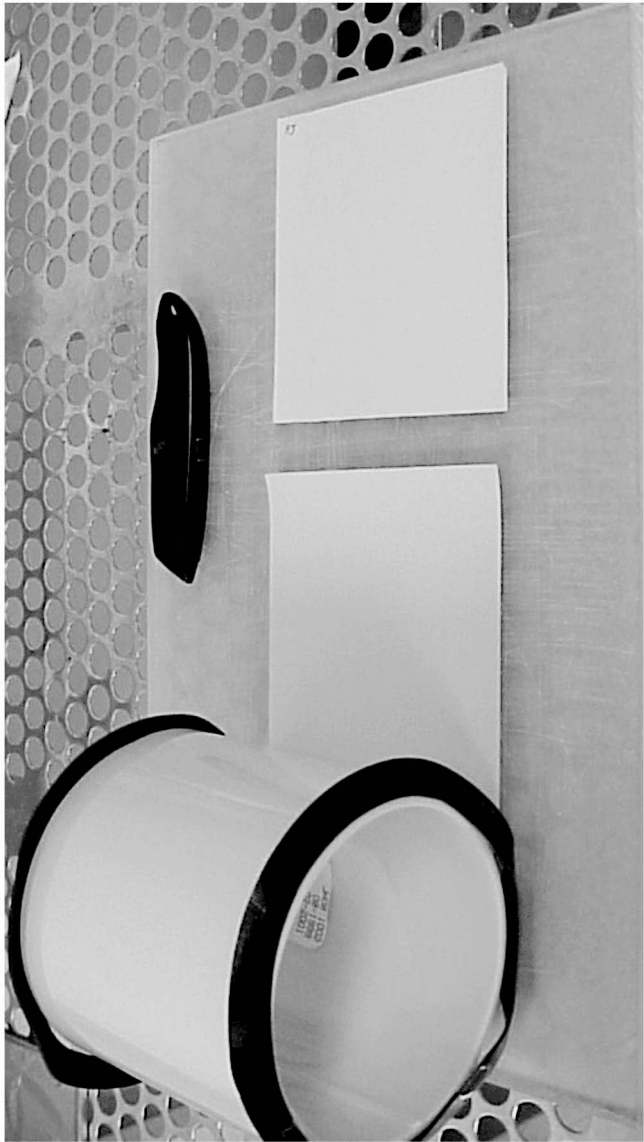
FIGURE 6.4
A 6 inch (150 mm) square sheet of unfired LTCC attached to a film carrier sheet. This sheet has been manually cut from a roll of tape that was cast and then trimmed to a width of 6 inches (150 mm) and a length of 50 feet (~15m).

TABLE 6.1

Exemplary Composition of Commercial Aluminum Oxide
Multilayer Ceramics

Purity (%)	Al_2O_3	SiO_2	CaO	MgO	Others	Color
99	99					White
96	96	3		1		White
94	94	5		1		White
92	92	7		1		White
90	90				Cr	Black

TABLE 6.2

Example of 90% Alumina Formulation (7d)

Component	Content (wt%)	<20	<15	<10	<8	<6	<4	<2	<1	<0.6	<0.4	<0.2
Al_2O_3 (A-14)	90	100	94.6	91.8	91.4	79.4	53.4	13.9	2.9	1.1	0.4	
Talc	6	100	95.5	93	91.3	89.3	85.7	80	40.9	21.3	12.8	6.6
Clay	4	100	99.7		99.1	98.9	97.8	95.4	75.1	53.1	43.3	13.5

feature as a means of improving the contrast for machine vision systems used to process the tape into substrates.

Commercial HTCC production is conducted on a very large scale that ensures uniformity of compositions and performance. A typical formulation for a 90% alumina composition is summarized in Table 6.2 [18]. This table summarizes the percentage of particles for all three main elements (talc, Al_2O_3, and clay) vs. the maximum particle size in microns. In this formulation, the three main inorganic components are alumina, talc, and clay. Often, alumina grades are mixed to provide an optimum particle size distribution, agglomeration, reactivity, and composition (purity) with a minimum cost, of course. The talc additive provides a source of silica (~60% SiO_2) and magnesia (~30% MgO) with the balance comprising oxides of Ca, Na, and K. Clays are mixtures of a number of minerals, including kaolinite, quartz, and feldspar and serve as sources of silica (~55%), alumina (30%), Fe_2O_3, TiO_2, CaO, MgO, etc. Whereas such compositions are suitable for standard HTCC packaging, in some applications, alpha-particle emissions arising from trace (ppm) concentrations of U and Th have been identified as sources of random bit or "soft" errors [19]. With a goal of ≤0.01 α/cm²h, high-purity alumina compositions and processing techniques have been developed [20].

Particle size is an important element in the performance of an HTCC system. Fine particle size enhances densification although submicron particles are often difficult to disperse effectively. A basic description of the effect of particle size on the sintering of particles is captured in Herring's scaling law that describes an exponential dependence of sintering time on particle diameter [21]:

$$t_2 = t_1 \, (r_1/r_2)^n$$

where t_1 and t_2 are the sintering times for identical powders with particle radii of r_1 and r_2, respectively. The exponent, n, varies according to the sintering mechanism: 1 for plastic flow, 2 for sublimation, 3 for lattice diffusion, and 4 for surface diffusion. A number of studies have shown that densification of alumina occurs via bulk diffusion and, thus, the appropriate Herring exponent is between 3 and 4 [22].

Whereas a submicron particle size distribution promotes rapid densification and can be an effective means of lowering sintering temperature or time at temperature, finer particles tend to form agglomerates. This tendency is associated with the term in the surface free energy inversely related to particle radius. In addition, they may be present in hard, aggregated structures. Agglomerates and aggregates function as large, primary particles, exhibiting correspondingly large pores and voids. This coarse microstructure leads to a net reduction in sintering efficiency. Prior to mixing, classification of powders has been employed as a means of rendering a more uniform particle size distribution, or to remove large agglomerates.

In multilayer production, inorganic powders are mixed with solvents, binders, dispersants, plasticizers, deflocculants, and other organic additives. This mixing process is conducted in large ball mills in which a considerable amount of particle size modification may occur. Thus, the particle size distribution is a function of both the constituent powders and the degree of particle size reduction that occurs in the milling process. Mixing and milling processes have been discussed extensively in the literature [23]. Generally, ball milling is employed in the tape-casting process. Other methods, including vibratory ball, attrition, ultrasonic, and jet milling have also been used. Typically, these processes precede the actual formulation of the tape compositions. Often, powder vendors supply several grades of the same raw material powder differing in the particle size distribution resulting from different grinding methodologies and efficiencies.

Tape casting of commercial alumina tapes is a high-volume operation conducted using tank-car quantities of ceramic powders, large ball mills, and multiple banks of tape casters, some of which may reach 30 m in length. Slip preparation entails two distinct steps: milling and mixing [24]. In the standard commercial process, ceramic powders, solvent, and dispersant are loaded into a ball mill. In this step, the dispersant acts to stabilize deagglomerated particles created by comminution in the mill. It has been shown that adding the dispersant in this first step results in superior viscosity, green density, and ultimately, fired density in an acrylic binder system [25]. The ball mill may be lined with rubber or ceramic, and the grinding media (balls) are typically high-density cylinders of a composition similar to that being prepared. This slurry is milled for 12–24 h until the desired degree of dispersion, reflected in the slip viscosity, is achieved.

In the second stage of slip preparation, the remaining organic components are added. A plasticizer imparts some flexibility to the tape whereas the

binder provides strength to the dried composite. These components may be added separately or together and are dissolved in the solvent. The slip is then milled for an additional 12–24 h, accompanied by a significant increase in viscosity, to ~1000 to 2000 cps. Tape-cast compositions have been developed for both aqueous and nonaqueous slurries. Environmental concerns favor aqueous systems although most commercial casting employs solvent-based slips.

The casting onto polymer carriers was first described by Park in 1961 [26]. Tapes are cast in uniform thicknesses, typically based on English units. For example, tapes as thin as about 0.002 in. and as thick as 0.025 in. are in commercial production. Thicker tapes, for example, 0.040 in., have also been demonstrated, although it is difficult to punch and laminate multilayer structures with such tape. In the casting process, control of tape thickness, belt speed, temperature, and drying atmosphere is critical [27].

6.2.3 Via and Cavity Formation

Once each of the blanked tape layers has been prepared for use in a substrate, the first process is normally via and cavity formation. In this process, the individual holes through each layer of the green ceramic are formed to allow electrical connections between layers in the vertical axis of the substrate. In addition, channels or cavities can also be punched or cut into tape layers to form a wide variety of unique electrical and mechanical features within a substrate. Traditionally, cavities have been used to recess integrated circuits into the ceramic to allow their surface to be flush with that of the ceramic or a wire-bond ledge. This approach is still popular and has a number of electrical and in some cases mechanical advantages when compared to placing the devices on the ceramics surface. In the past few years, these processes have also become very popular for the creation of unique electromechanical structures within the ceramic substrate such as those used for MEMS devices.

There are primarily two methods that are most commonly used for via and cavity formation: laser cutting and mechanical punching [28–30]. By far, mechanical punching is the most popular method for via formation due to the high-speed nature of this process as well as high quality of the resulting vias. Laser cutting of tape has its advantages in the formation of channels or cavities because arbitrary shapes can easily be created. In contrast, mechanical punches must use custom die or be programmed to nibble away the desired structure.

6.2.3.1 *Laser Processing*

Lasers have been used for decades to cut ceramics, both in fired and unfired states. These systems use a number of different laser types, though CO_2 and Nd:YAG lasers are perhaps the most common. The lasers are generally fixed in position because of their relatively large size, and the tape layer to be cut

is moved relative to the fixed laser beam. Alternatively, lenses are often used to move the point of impact of the laser beam across the surface of the tape. By moving the beam or the tape using one of these methods and employing shutters to regulate the beam, very complex vias and cavities can be cut into a tape layer.

The primary benefit of laser cutting is the ability to cut complex shapes with rounded or curved edges. For example, singulation of a large panel into small round substrates is impossible with a dicing saw but can easily be accomplished with a laser. Likewise, complex cavities can be nibbled out with a computer numerical control (CNC) mechanical punch; however, the edge quality tends to be poor, and the process is very slow. In contrast, a laser can easily and rapidly cut these types of features.

However, lasers generally do not cut vias as cleanly as a mechanical punch. As illustrated in Figure 6.5(b), the laser-cut vias tend to be conical in nature. This effect is created by the fact that the laser can generally only produce a small spot size with a shallow depth of focus. As the laser cuts into the green ceramic tape, the material is ablated, yet the laser begins to defocus slightly. The exact shape of the via depends on the thickness of the tape relative to the laser's depth of focus as well as the focal point of the laser relative to the top surface of the tape layer. In addition, the ablation process tends to leave debris on the tape's surface. This material consists of the tape material that was not completely ablated. The top surface of the tape also tends to exhibit a volcano-like lip around the vias. For many applications, these vias are acceptable; however, the vias produced by mechanical punching (Figure 6.5a) are fundamentally cleaner and approximate the ideal cylinder because the undesired tape is cut and removed by the punching system. Figure 6.6 compares the measured front side and backside dimensions of laser-cut and mechanically punched vias in LTCC sheets. These data were measured for a variety of tape layer thicknesses as indicated on the horizontal axis. As noted in Figure 6.6a, the laser-cut vias, with a nominal opening of 3 mil (75 μm), show a more than 20% decrease in diameter on the opposite side of the tape due to shallow depth of focus of the laser beam. In comparison, the difference in the entrance and exit size of the punched vias shown in Figure 6.6b is negligible because the deviation, at less than 1 μm, is within the measurement error.

6.2.3.2   *Mechanical Punching*

Mechanical punching methods can be separated into two broad categories: hard tooling and soft tooling. As the name implies, hard tooling generally consists of a dedicated die set that is designed to punch a large number of holes for a given design in a designated tape blank size. These tool sets are very fast because they punch all of the vias, cavities, and in some cases, cut the tape to size in one rapid step. As a result, hard tooling results in the lowest unit cost for large volume fabrication. The disadvantage of this approach is that the tooling is specific to one tape layer of one design, and
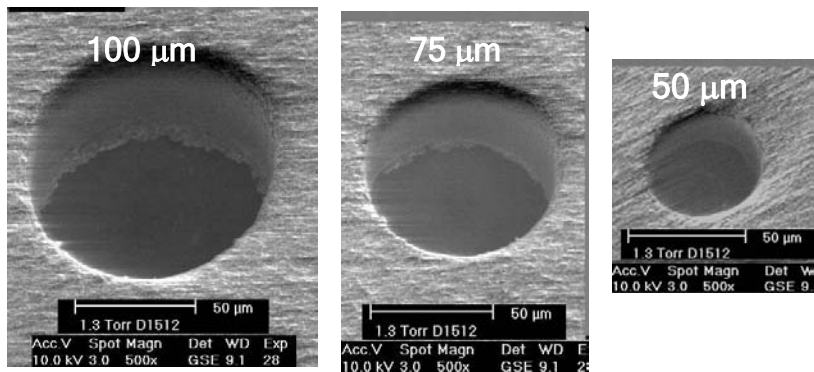
(a)
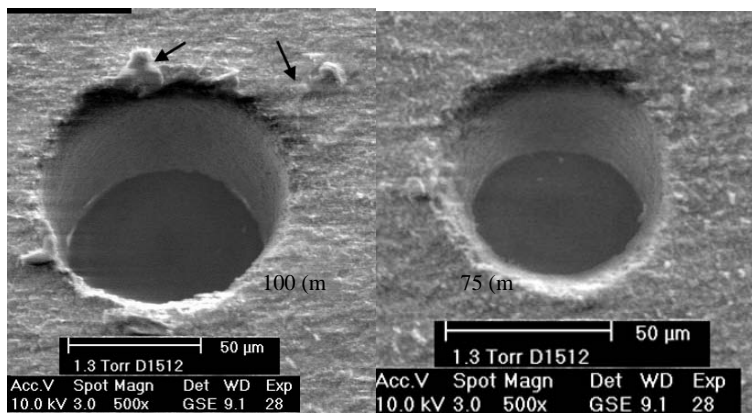
(b)

FIGURE 6.5
(a) Vias prepared in unfired LTCC by mechanical punching. (b) Vias prepared in unfired LTCC by laser cutting. 100 micron (left), and 75 micron (right). Note the debris around the laser cut vias and the rough "lip."

any design changes require a new tooling set. As these hard tooling sets are very expensive, they are generally only used for high-volume production in well-established designs. The cost of modifying these tool sets for a minor design change is simply too great for low-volume or prototype applications.

In contrast, soft-tooling methods use a computer-controlled punch and die, or a set of punches and die, and CNC. This approach allows for rapid design changes that only require the change of a computer file. These computer files, which are often referred to as *drill* or *punch files*, contain a set of *x*, *y* coordinates and a punch number for multiple punch machines. Computer programs are used to generate these files from CAD layout programs

(a)

Drilling side: 69.8±1.2 μm   Back side: 53.1±1μm

(b)

Top side: 77.8±1 μm   Back side: 77.8 ±2 μm
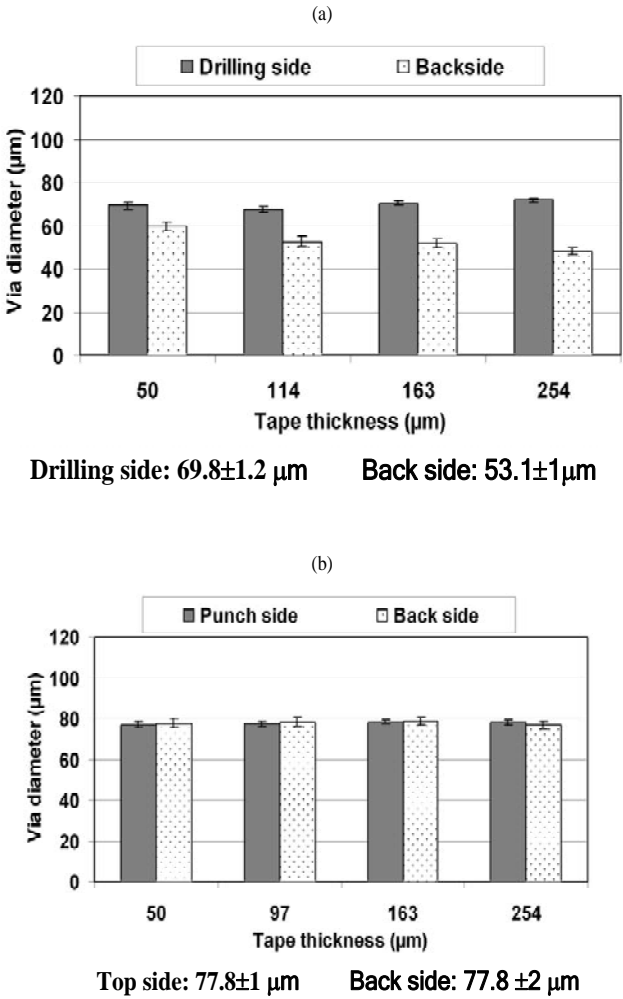
FIGURE 6.6
(a) Measured green diameter of laser cut vias for several tape thicknesses on the front and back side of the tape. (b) Measured via diameters for a set of punched 75 micron green vias for several tape thicknesses.

and to optimize the punching sequence for maximum speed. In contrast to hard tooling, these soft-tooling processes are slower but much more flexible in terms of their use for multiple designs or design revisions.

CNC mechanical punching systems, as shown in Figure 6.7, operate using the same basic principles as a paper hole punch. A punch is located above the desired hole location and a corresponding die is located below the desired location. In most cases, the tape layer is moved, and the punch and die are fixed with reference to one another. By accurately moving the tape

FIGURE 6.7
A CNC Punch System used to form vias in multilayer ceramic tape layers.

layer that is being punched, and repeatedly depressing the punch into the die at the desired location, a large number of vias can be fabricated very rapidly. In many cases, more than one punch may be used simultaneously to increase the speed of the process. These punches are often pneumatically or electrically activated and can be very fast, with one punching action requiring a fraction of a second.

The punch and die, as shown in Figure 6.8, are generally fabricated from carbide steel that is very hard but somewhat brittle. This material is necessary because most of the glass ceramics used in cast tapes are hard and abrasive and cause wear of the punch material. Generally a small clearance, on the order of 12 µm, is provided between the die and punch to ensure that they do not come into contact during the punching process. This clearance is generally achieved by slightly increasing the size of the die opening relative to the punch diameter. For example, a 4-mil (100-µm) punch will often work in concert with a 4.5-mil (~112-µm) die. This die-to-punch clearance is very
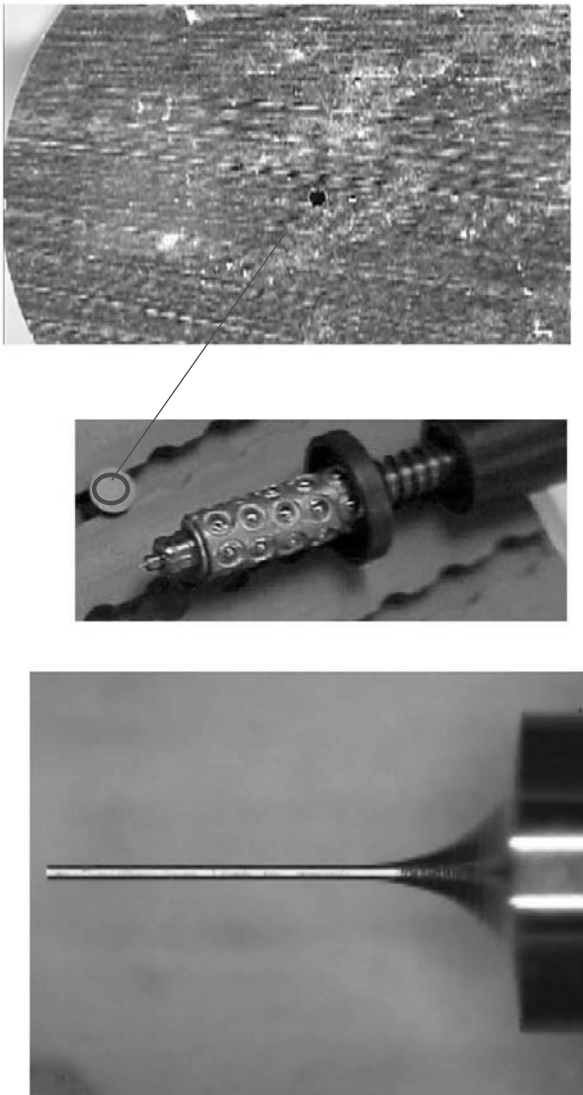
FIGURE 6.8
A 4mil (100 µm) Punch (bottom) and Die (top) that are used to form vias in green sheets of ceramics. The center image is a punch holder that is used by the punch system to hold the small via punch.

important to avoid premature damage of the punch and die caused by contact between the two. As the tape is rapidly punched and moved, the forces involved may cause the punch to deviate slightly from a strictly vertical trajectory. A tight die-to-punch clearance or an inadequate alignment
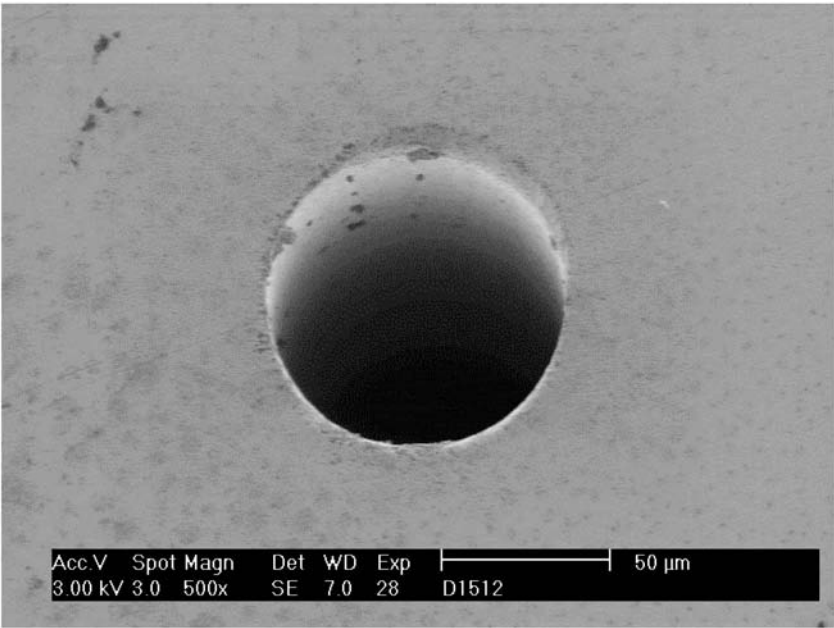
FIGURE 6.9
A worn 3 mil die (3.5 mil actual size) opening. Note the chipped "half moon" section in the upper right hand side of the die opening.

in the punching system can create contact between the punch and die that generally will damage both. As illustrated in Figure 6.9, the contact area will often cause chipping of the die opening. The punch may also be chipped, or in the case of very small punches, it may break completely. If the punch does not break incompletely, cut vias may result as illustrated in Figure 6.10a. The site of the punch and die damage generally leave a small flap, as shown in Figure 6.10b, of uncut material, which may or may not lead to defects in the substrate depending on the tape thickness and via size, as well as the design rules used for the substrate in question [14,30].

Punch and die sets are available in both round and square versions. Round dies are most common because of their ease of alignment relative to one another. Square punches must be accurately aligned both in their center location relative to the die, as well as the rotation of the punch relative to the die. In spite of this additional complexity, square punches are employed in cases in which very precise square cavities are required.

As the punch pierces the tape material, a round or square section of the tape is cut free and must be removed as a waste product of the process. In many cases, the dies are hollow, as shown in Figure 6.11, and vacuum is applied to the base of the die to extract this unwanted material. Some high-end punching systems also effectively float the tape to be punched on a
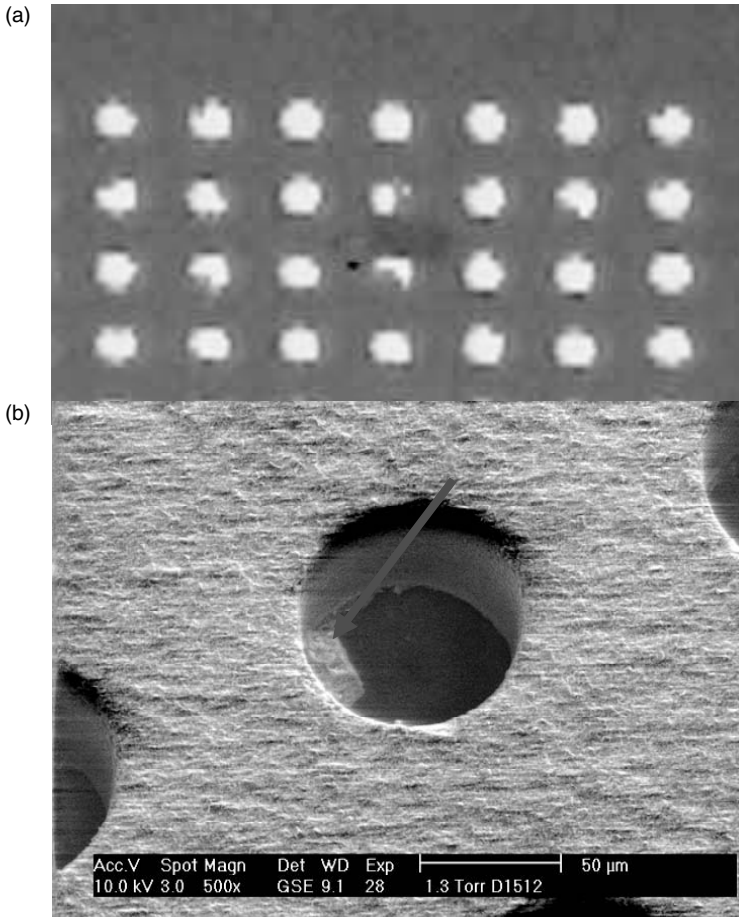
FIGURE 6.10
(a) A back illuminated set of empty vias in a punched LTCC layer. Note the small pieces of debris left in the vias due to a damaged punch and die. (b) SEM micrograph of a partial cut via caused by a damaged die. Note the small flap of uncut ceramic tape material.

stream of air. This airflow helps to avoid contact between the base of the tape layer and the punch machine, and produces a cleaner punched sheet.

Multiple punch systems are often referred to as *gang* punch systems. These machines are commonly configured for a particular part and panel size. For example, a 150-mm panel width and a 10-mm square component size arranged in a 15 × 15 matrix can be rapidly punched by simultaneously activating one punch for each of the 225 component locations. The tape layer can then be moved to the next desired via location and all 225 punches (1 per 10-mm component area) are then activated simultaneously to form 225 vias in the time that would normally be required to form 1 via in a standard CNC punching system. Obviously, this approach dramatically improves the speed of the via-formation process in a given layer. However, some flexibility
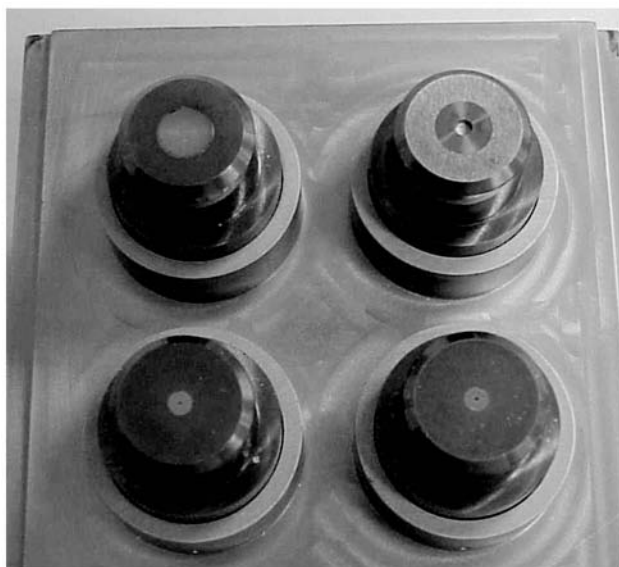
FIGURE 6.11

A die holder for a low volume CNC via punch system. This system is capable of simultaneously holding four via punches. Note the "slug" of cut tape material visible in the hollow center of the top right die.

is lost in that any change in a component size or in the panel size is not easily accommodated without new tooling. In comparison, a single punch system can accommodate these changes with a simple modification to the punch data file.

6.2.4 Via Fill

The via-formation process, although an important step, simply creates a hole in the individual tape layers. These holes provide a break in the dielectric isolation between the circuit layers but are not yet circuit interconnects. To create a low-loss electrical connection in these areas, the via hole must be filled with conductive metal. This process is generally done by injecting a thick-film ink into the holes with either stencil-printing or a bladder-fill operation. The ink used for this process is generally more viscous than that used for screen printing because it is designed to fill a 4- to 12-mil (75- to 304-μm) via hole and not run or sag prior to drying. As the ink has been dried and fired inside the ceramic substrate, the solvent and binder in the ink are burned off and a solid metal plug remains. These plugs not only coat the sidewalls, as would be the case in a plated through-hole of a printed circuit board (PCB), but ideally fill the entire via hole, creating a low-resistance electrical connection from one side of the tape to the other, as specified by the designer.

6.2.4.1   Stencil-Filled Vias

The stencil-fill process is very similar to conventional screen printing; however, most foundries use a metal stencil rather than a mesh screen. These stencils are generally either laser-cut or chemically etched with via holes in locations identical to those in the individual LTCC tape layer. The stencil is mounted in a screen printer that is usually configured in contact mode. The contact mode provides for zero snap-off distance during the printing cycle so as not to deform the stencil. This is a key difference between stencil printing and screen printing, primarily due to the inability of the stencil to stretch without deformation, which a screen can easily accommodate. A suitable via-fill ink is applied to the stencil, and the printing process is then activated to fill the vias in a particular tape layer all in one pass. Generally, a large quantity of tape is filled and then the printer can be reloaded with a new stencil that has been cut for the next design layer in the substrate. This process is repeated for each of the design layers in a given substrate to produce a sufficient quantity of each layer for the desired number of substrates.

Figure 6.12 illustrates a typical stencil used for a via-fill process. The key components of the stencil are the aluminum frame, the stainless foil that forms the stencil, and a suitable mounting material. The stainless foil is generally ~5 mil in thickness, but this thickness may be adjusted to optimize the fill quality for a given application. Stainless steel is preferred due to its corrosion resistance and ease of cleaning. Whereas most LTCC panels are generally 6- to 8-in. square or smaller, a 12-in.-square stencil, or larger, is generally used. The larger stencil area is generally required to provide adequate space for squeegee travel beyond the printed area and screen snap-off (in the case of a screen) at the end of the print cycle. The openings in the stencil are generally the same size as the vias to be filled but, in some cases, may be cut slightly smaller or larger for a given application.

6.2.4.2   Bladder-Filled Vias

The bladder-fill process is somewhat similar to the stencil-fill process in the sense that both techniques use a stainless steel "mask," the stencil, to inject the ink through. However, the injection processes are fundamentally different, in the sense that the bladder-fill injection system uses a rubber bladder and compressed air instead of the shear force of the squeegee as in stencil printing. Figure 6.13 illustrates the basic concept of the bladder-fill process. An unframed stencil, as illustrated in Figure 6.14, is used instead of the standard frame used for stencil printing. This stencil is normally 4–6 mil (100–150 µm) in thickness and includes not only the via holes, which are identical in number and location as the vias in the tape layer, but a series of "tooling" holes that are used to align the stencil in the bladder-fill system. The paste to be injected is spread across the surface of the stencil, and then a clean rubber bladder is placed on top of the ink. This combination of stencil, ink, and bladder is loaded into the machine. A tape layer to be filled is placed on the stage of the machine, and then the machine is cycled to fill the tape
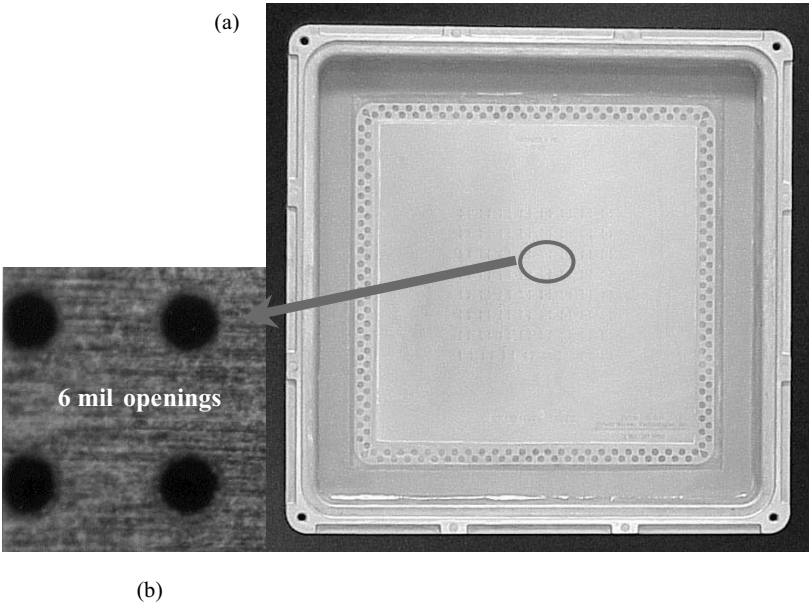
FIGURE 6.12
(a) Stainless steel stencil mounted in an aluminum frame for a via fill process. (b) An magnified view of a small portion of the stencil illustrating the small via openings.

FIGURE 6.13
A bladder-fill system with the stainless steel stencil mounted and silver ink applied to the stencil.

(A)

(B)
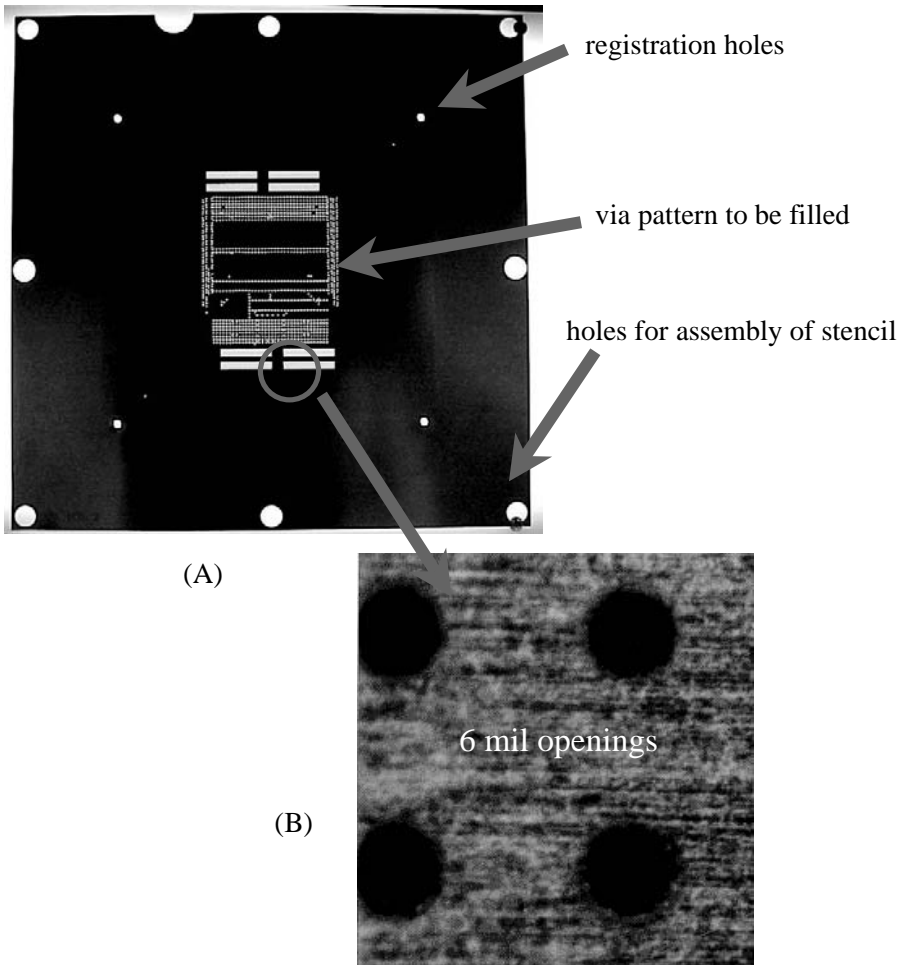
FIGURE 6.14
(a) A stainless steel stencil used for the bladder-fill process. (b) A magnified image of a few of
the holes in this stencil.

layer. During this process cycle, the bottom of the stencil is brought into
alignment with the tape layer using mechanical pins or machine vision to
register the two components accurately. Pressure is then applied to the stencil
or bladder assembly to maintain contact between the two and form an air
tight seal. Pressure is applied to the rubber bladder, which then forces the
ink through the stencil and into the empty vias. This process only requires
a few seconds, and the result is a tape layer with metal-filled vias. Generally,
a stencil will be loaded into a machine for a given design layer, and a large
number of parts for the design layer will be filled in a consecutive manner.
It is common practice to use this method to fill thousands of vias in a given
tape layer in one rapid process.
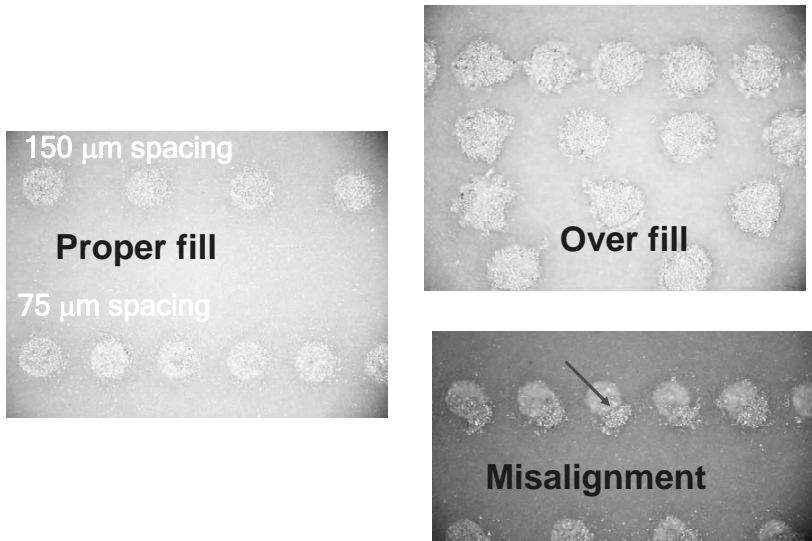
FIGURE 6.15
Filled 75 micron vias in LTCC prior to firing.

Figure 6.15 illustrates a typical set of filled vias after this process. The quality of the fill is important because an under-filled via may result in an incomplete contact between the printed ink on that layer and the via metal. This results in open interconnects within the substrate. At the other extreme, over-filled vias may result in smearing of the ink across the surface of the tape during subsequent processing, which generally results in undesired short-circuit connections between interconnects. In both via-fill processes the ink viscosity, solids content, stencil openings, and process settings can be adjusted to accomplish the desired fill.

6.2.5   Screen Printing

Once the vias have been created and filled, the traces on each layer must be screen printed to create the horizontal interconnects across the surface of each layer in the substrate. These interconnects are generally created with screen printing or photo-defined techniques, which will be described in Chapter 7. Hundreds, or in some cases, thousands of individual interconnects can be created in one rapid process with screen printing based on the physical layout provided by the substrate designer.

Traditional screen-printing technology serves as the basis for HTCC and LTCC technology through the creation of metal circuit traces, capacitor dielectrics, and a variety of other films. The printing method builds on the nearly 50 years of industrial experience in the use of this technique on prefired substrates such as alumina. However, there are some unique aspects

of the process as it relates to printing on tape materials. In general, the process may be used to print inks onto the fired top and bottom surfaces of an LTCC substrate, to print films onto the unfired surface of a green tape layer, or to fill vias with conductive ink. The first of these processes proceeds in an identical manner to a traditional process used for an alumina substrate. The other two processes, which are depositing ink into or onto unfired green sheets of ceramic, require some unique tape-handling methods to ensure that the fragile unfired ceramic sheets are not damaged during these process steps.

Whereas the process is generally referred to as *screen printing*, in fact, both screens and stencils are generally used for different kinds of applications. As shown in Figure 6.16 and Figure 6.12, the primary difference between the two is that the stencil is a sheet of stainless steel, whereas the screen is a stainless steel mesh. The stencil is generally composed of stainless steel a few mils in thickness that has been mounted to a rigid aluminum frame. Holes are cut through the stencil in the location of each desired via. The reader may also be familiar with the use of similar stencils for solder deposition in the PCB industry. In contrast, the stainless steel screen is a weave of fine wires that are also mounted to a rigid aluminum frame. Photo emulsion, a photosensitive polymer coating, is used to selectively block regions of the mesh and allow ink to flow only through desired areas to form a pattern on the substrate.
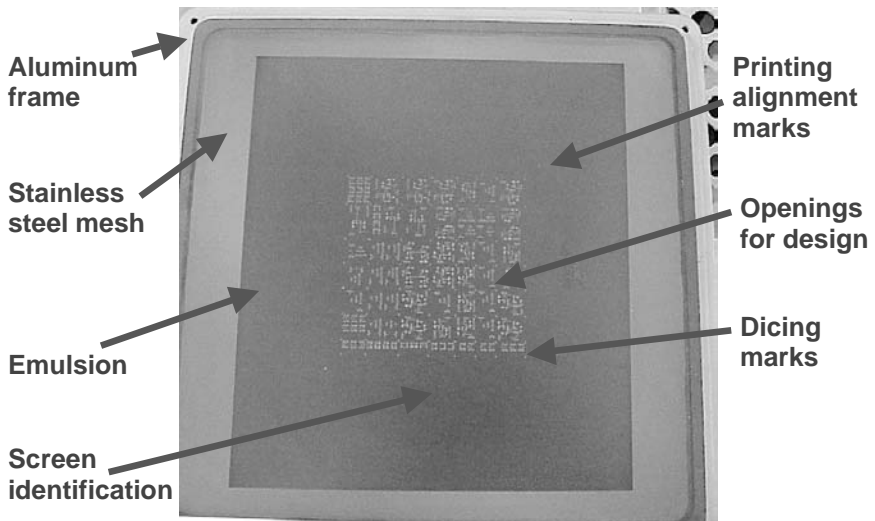
FIGURE 6.16
Typical stainless screen used for screen printing.

Screens are generally specified in terms of the wire count or number of wires per inch, wire diameter, the angle at which the wires intersect with the frame, and the thickness of the photo emulsion. All these parameters can be adjusted to create different ink depositions with variable thickness and line resolutions. The wire count is perhaps the simplest of these screen parameters because it simply expresses the size of the screen mesh opening. A screen door or window screen used in residential or commercial buildings is normally composed of 16 to 18 wires per inch. In contrast, the screens used for electronics are normally in the range of 200 to 400 wires per inch, with a value of 325 as perhaps the most common. Lower values are sometimes used for printing thick ink depositions or for coarse-line features such as solder, whereas finer mesh screens are growing in acceptance for fine-line depositions; the wire diameter is also relatively straightforward with values in the range of 0.9–1.2 mil in common use. In general, higher mesh counts use finer wire diameters and are capable of producing smaller printed features.

The angle at which the wire intersects the frame also impacts the quality of the print, and is normally either 45° or 90°. For two otherwise identical screens, one with 45° mesh and the other with 90° mesh, the 45° screen provides a superior line quality because the openings in the 90° screen are more difficult to align to the desired pattern. Chapter 5 describes the screen parameters and printing process in detail, and Equation 5.1, can be used to calculate the opening size for a given set of screen parameters. Generally, two to three mesh openings are needed for a given printed line to create acceptable print quality. Finally, the photo emulsion impacts the resulting wet-film thickness and therefore the final fired-film thickness, as well as the resolution of the printed ink.

Figure 6.17 illustrates graphically the basic screen-printing process steps. The screen is generally separated from the tape layer or substrate to be printed by a small gap that is commonly referred to as the *snap-off distance*. Ink is applied to the screen and a squeegee, a hard rubber blade, is forced down onto the screen and moved across the screen's surface as shown in Figure 6.17b. This force causes the ink to be transported in front of the squeegee, as well as the screen, to deflect and make contact with the substrate. This contact occurs along a band in the vicinity of the squeegee and perpendicular to the direction of the squeegee travel as illustrated in Figure 6.17c. This squeegee force causes the non-Newtonian ink to decrease in viscosity and easily flow into the openings in the screen as well as across its surface. As this band of contact progresses across the screen, ink is deposited onto the substrate through any openings in the photo emulsion. As the squeegee moves past an area, the screen snaps back to the original gap — hence, the term *snap-off distance*. The result is that the pattern of openings in the screen is transferred to the substrate or printed tape layer, as illustrated in Figure 6.17d. Once the ink makes contact with the substrate, the shear force created by the squeegee is removed, and the ink viscosity increases. This increased viscosity is important to minimize the flow of ink once it has
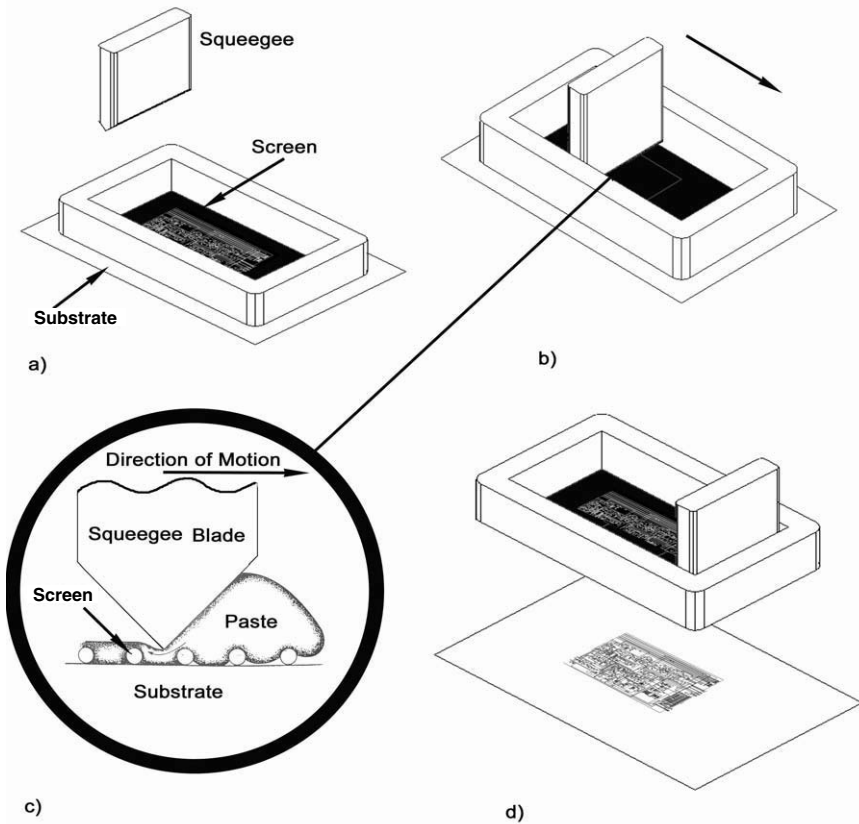
FIGURE 6.17
(a) A schematic representation of the screen-printing process. (b) Once the paste has been applied to the screen the squeegee applies pressure and moves across the screen's surface. (c) This squeegee pressure decreases the ink viscosity and forces it through the openings in the screen or stencil. (d) Once the squeegee stroke is complete the screen snaps back leaving the printed image on the tape layer.

been deposited on the substrate, thereby retaining the pattern created in the screen's photo emulsion.

Stencil printing is very similar to this process except that it is normally conducted with zero snap-off distance, i.e., with the stencil's bottom surface in contact with the tape layer. Also in the case of stencil printing, higher squeegee speeds are used in the via-filling process to provide increased ink shear forces, thereby facilitating the flow of ink into the vias.

A low-volume prototype screen- and stencil-printing machine is shown in Figure 6.18. This machine is equipped with a porous stone vacuum chuck that is specifically designed for handling tape layers. Unlike a prefired ceramic substrate, the green sheets of LTCC, HTCC, or MTCC are fragile and must be handled with care; however, adequate force must be applied
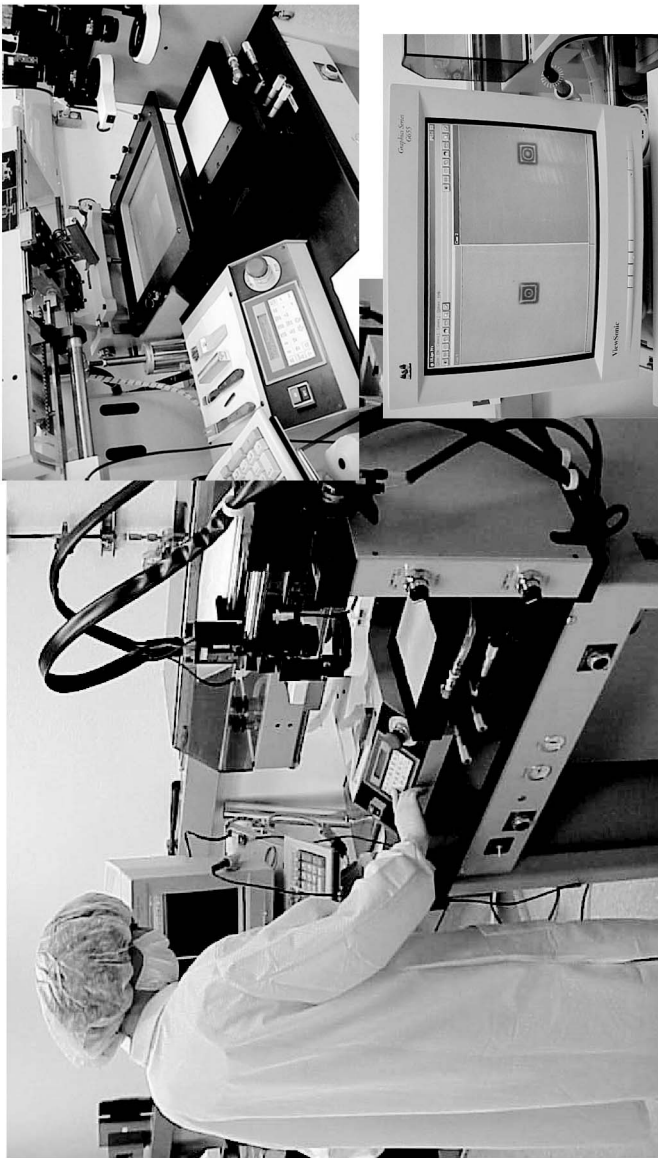
FIGURE 6.18

A typical low-volume printer configured for printing green sheets of LTCC. This unit is equipped with machine vision to assist in aligning the print with the vias that have been created in the tape layers.

to hold the sheet on the printer stage throughout the process. The porous stone chucks, which include a very large number of small holes and porous pathways, have traditionally been used to solve this problem. By drawing a vacuum on the backside of the stone, the tape layer is effectively held in place by hundreds or perhaps thousands of small vacuum ports. This distributed force allows the tape to resist without damage the adhesion created by the ink and the screen during the snap-off portion of the print cycle. Unfortunately, these stone surfaces may introduce contaminate particles, and care must be taken to ensure that ink is not allowed to enter the porous structure. Ink contamination will slowly clog the chuck and reduce its effectiveness. As a result, many of the newer printing systems now use a large number of very small drilled holes in a flat metal plate as the vacuum chuck. These metal chucks contribute no particle contamination and are far easier to clean.

6.2.6   Inspection

As the fabrication process for LTCC and HTCC is fundamentally parallel, inspection plays an important role. Defective layers are ideally identified as early as possible so that additional value is not added to a layer that will ultimately be discarded as scrap. In addition, once a layer is committed to a substrate stack and that stack has been laminated, a defect in a single layer can lead to a scrapped substrate. As a result, inspection is normally performed on a sample or 100% basis throughout the process. These inspection steps generally include verification of via creation, via fill, and comparison of the screen-printed metallization to the design. This process can be as simple as an operator working with a microscope, but automated systems are also available.

An example of an automated system for verification of punched vias and printed traces is illustrated in Figure 6.19. This system is loaded with the artwork files for the layers in a substrate and then compares an image generated by a camera system to the design. By backlighting the tape layer under inspection, a large visible contrast can be created between the vias prior to the fill process and the LTCC material. This contrast is easily recorded with a computer-controlled camera system that then compares the via locations relative to the CAD design. This inspection process allows for the detection of missing vias and partial-punched or cut vias, as well as verification of the size and precise location of each via in a given design. These automated inspection systems can also compare a known good layer to questionable layers by recording an image of the good layer and then comparing it optically to the subsequent layers. This approach eliminates the need for the generation of templates from the CAD data, but in some cases, it is difficult to obtain a known good sample with 100% certainty.

Many inspection systems are available that can compare unfilled vias, filled vias, and printed traces to CAD data or known good samples. The operator

FIGURE 6.19
A machine vision inspection system designed to identify errors in via formation, via fill, and print quality.

generates a template from the CAD data for every layer in a given substrate. The system is used to compare these templates to an image of the tape layers. This template contains an inner and outer threshold that can be selected by the operator. Ink that is observed to be outside the outer threshold is flagged as an overprint or a smear that may create a short, whereas the absence of ink within the inner threshold is flagged as a potential open circuit. By adjusting the inner and outer thresholds, the yield vs. the precision of the required layers can be balanced. This balance is important because some applications require great precision to meet the electrical specifications, whereas other applications have far less stringent requirements. This template method can also be applied to find unfilled vias, partially filled vias, or overfilled vias.

6.2.7   Tape Layer Collation

The process up to the layer collation is fundamentally parallel in nature, in that each layer in a given substrate is blanked, filled, screen printed, and then inspected. However, to create the final substrate, the appropriate layers must be stacked in an intimate way so that they sinter together during firing and create a solid block of ceramic and metal that contains the circuitry of interest. The first step in this process is often referred to as collation or *stack and tack*, because tape layers — one, two, three, through *N* — are each selected in order and temporarily bonded to the next layer to form the substrate. This process has two key requirements: a strong temporary bonding between the layers and precise layer-to-layer alignment.

The alignment requirement arises from the fact that each tape layer may contain thousands of vias and traces that must all align from one layer to the next. Generally, this means that a misalignment of no more than 50 μm may exist between any two adjacent layers, and in some cases, the requirement may be much more stringent. The required tolerance is a function of the feature sizes that are used in the design. Designs with 250-μm space and trace rules are far easier to align than designs that use 50-μm design rules. Accommodating this kind of tight tolerance is not trivial, because two thin and flexible sheets of material must be precisely aligned to within >0.03% of the overall panel dimensions for a 150-mm tape blank and >0.02% for a 200-mm tape blank. Two principal methods are used to achieve this alignment: optical alignment with machine vision and pin-alignment fixtures. The pin-alignment fixtures generally are composed of stainless steel or similar metal and have four pins located at the corners of the tape blank, as shown in Figure 6.20. These pins are inset from the edge of the tape layer a small distance and correspond to punched or cut holes in the tape layers. By slipping a tape layer over the pins and then down on the metal plate the tape layer is located as shown in Figure 6.20. The next tape layer in the substrate is then placed over the pins in an identical manner. By locating each successive tape layer with respect to the pins and the identical punched holes, the tape layers can all be precisely aligned to the pins and therefore each other. This fixture is normally used to locate the tape layers throughout the lamination step to ensure that the alignment is maintained. In this way, the layers are not really "tacked" or bonded together but merely held in alignment by the fixture. The principal limitation of this approach is that the tape layers tend to stretch and, in some cases, the holes in the tape are slightly deformed by the pins. As a result, alignment errors less than 50 μm are very difficult to obtain with this method. In addition, this process is difficult to automate and generally requires a skilled technician, resulting in variability in layer alignment between one technician and another.

Optical alignment based on camera systems and computer-based machine vision is a far superior method that can minimize alignment errors down to 10 μm in some cases and can easily be automated. This is critical for very small features used in advanced design rule sets. In a fully automated

FIGURE 6.20
An alignment fixture used to register individual tape layers to each other for lamination. One sheet of LTCC has been placed on the lower (left hand plate).

process, a machine picks up the first tape layer using vacuum, and then a set of cameras will identify punched or printed structures on the tape layer. The next tape layer is picked up, and identical alignment features are identified on this tape layer. The machine then moves one of the tape layers until they are precisely aligned. The two layers are brought into contact with each other to complete the alignment process. However in this case, the layers must be bonded in some temporary manner until lamination. This step is necessary because no fixture is used to maintain the alignment. The temporary bond is achieved through heat and pressure, which bonds the polymeric binders in the LTCC material to each other. The next layer is then picked up by the machine and aligned to the combined first two layers using the same camera and computer system. This layer is bonded or "tacked" to the first two layers. The process continues in this manner until all the layers have been aligned and temporarily bonded. Figure 6.21 illustrates a typical low-volume stack-and-tack system.
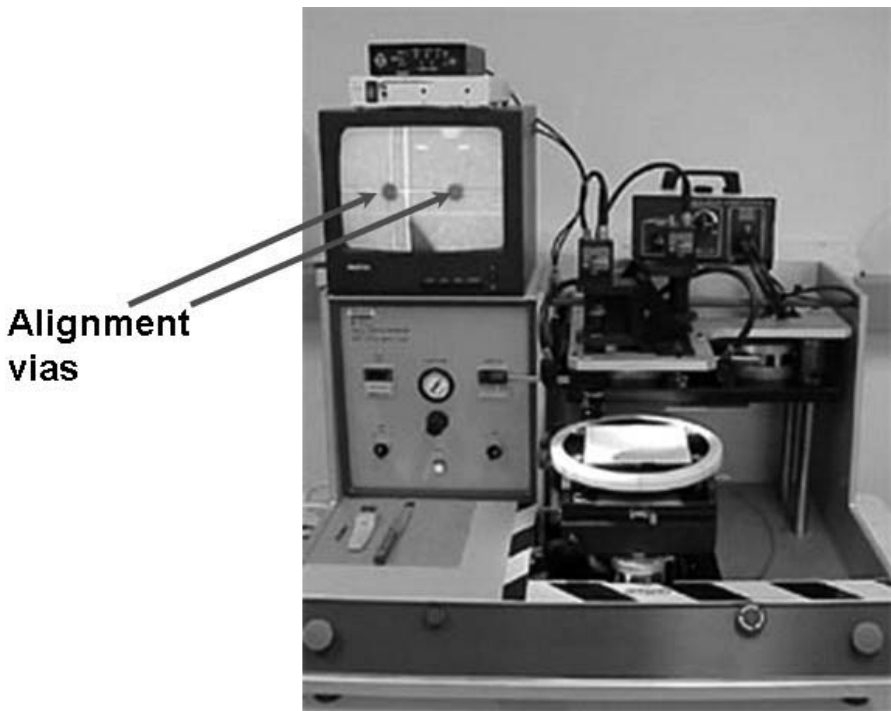
FIGURE 6.21
A low-volume stack- and tack-system designed to align 6-inch (150 mm) blanks of LTCC.

Tacking of the layers to form the temporary bond can be performed in several different ways, with either a full tack of the layers or a tack only at the edges. Some equipment manufacturers have chosen to apply pressure and temperature to the entire tape blank, thereby bonding the layer to each other over the entire surface area. Other manufacturers bond a few locations at the edge or a seam around the edge of the panel. The full tack approach suffers from a requirement for much higher pressure than the other methods. In addition, this approach may potentially deform the tape layers.

Not only is the final layer-to-layer alignment limited by operator or equipment but the green ceramic layers themselves may also contain some amount of alignment error relative to the design. These errors may be caused during the punching or printing processes; however, the largest contribution may be caused by expansion and contraction of the ceramic material itself. One goal of the conditioning process is to stabilize the tape to minimize this expansion and contraction. In addition, framing or plastic sheet backing materials may be used to help constrain the tape.

6.2.8 Lamination

Once the layers have been collated or stacked, a more permanent bond is required prior to firing. The particles within adjacent layers must be in intimate contact during the firing process or voids, and delaminations may form in the final substrate. The process used to ensure this tight bond is lamination. Whereas the exact pressures and temperatures used depend on the material composition, 3000 psi at 70°C for 10 min are common process conditions. This high pressure and elevated temperature softens the polymer matrix of the green ceramic and facilitates good adhesion and coalescence of adjacent layers. After lamination, the layers are very difficult to separate, and the substrate is ready for the firing process. Two principal methods are used for lamination: isostatic lamination and uniaxial lamination.

Uniaxial lamination is performed in a press that is equipped with heated plates. The part to be laminated is often placed inside a metal fixture, which is then placed in the laminator. This metal fixture is usually the same one that is used in the collating step to align the layers to each other. The laminator applies heat and pressure to the fixture, which then transfers the heat and pressure to the ceramic tape layers. This process has the advantage of speed and simplicity, and several manufacturers offer automated systems for relatively high-volume production based on this method. The disadvantage of this approach is the inherent difficulty in establishing perfect parallel lamination plates. The result is some variability in the pressure across the plates and thus some variability in pressure across the laminated ceramic layers. This is a critical issue because the lamination pressure, time, and temperature affect the density of the laminated substrate. This green density, in turn, affects the shrinkage and final density of the fired substrate. As a result, variability in the pressure can create variability in the shrinkage of

the parts. In some cases, this may lead to a large enough variability that the yield is decreased.

In contrast, isostatic lamination uses a water-filled pressure vessel to apply heat and pressure to the ceramic layers, as illustrated in Figure 6.22. This process is more complex because contact between the water and unfired ceramic must be avoided. The pressure and temperature uniformity across the part, however, is superior to most uniaxial lamination systems. The tacked layers to be laminated are vacuum bagged to prevent introduction of water into the substrate, and metal plates may be used on either or both sides of the tape layers. A base plate is used to support the tape layers, whereas a second metal plate on top is referred to as the *cover plate*. Cover plates serve to distribute the pressure uniformly over the substrate, but may be omitted in some cases. As can be seen in the upper left-hand inset of Figure 6.22, the vacuum-bagged parts are often stacked inside the laminator on multiple shelves. Many parts can be laminated in one batch lamination cycle with this approach.

6.2.9   Firing

Once the individual layers of green ceramic tape have been prepared and laminated together, the substrate must be fired to create the desired dense ceramic. This process can be performed as a batch process in a box furnace, such as the low-volume unit illustrated in Figure 6.23 or in a continuous belt operation. In either case, the green multilayer ceramic substrates must be placed on a setter during this firing cycle because many of these materials will conform to the surface on which they are fired. Different setter materials may be used, depending on the firing temperature and composition of the ceramic tape in question. Setters are generally very flat and must be kept very clean. Irregularities in the surface or contamination may be transferred into the substrate in the form of an inclusion, a bump, or a dimple in the material. The planarity of the setter is also very important because camber in the setter may easily transfer into substrate camber.

The advantages of utilizing a box furnace include improved control over the temperature uniformity and, in many cases, gas flow, as well as low price and small foot print. These factors are important because variations in the temperature across the top of a substrate or from the top to the bottom of the substrate during firing may cause the substrate to shrink in a nonuniform manner. Clearly, the major limitation of box furnaces is the low-fabricated part throughput. A given substrate profile may take many hours in a box furnace. The majority of modern box furnaces offer computer control or an integrated microcontroller that can be programmed for a given temperature profile. A typical LTCC profile is illustrated in Figure 6.24. The first part of the profile is a rapid temperature rise to 350°C, followed by a 1-h soak at that temperature. This portion of the profile is often referred to as an *ash* because the organic components within the substrate are burned off, leaving

FIGURE 6.22

An isostatic lamination system capable of laminating multiple multilayer ceramic substrates in one rapid process. As shown in the upper left inset, these substrates are normally vacuum bagged and stacked on shelves that are lowered into the pressure vessel of the machine. (Courtesy of Avure Autoclave Systems, Inc.).

behind the inorganic materials that will form the final substrate. During this portion of the profile, the substrate evolves a large quantity of gas that must be removed from the furnace and vented. Once the ash phase of the process

FIGURE 6.23
Typical small volume box furace with embedded microcontroller. The white setter visible on the upper shelf is used to support the blue substrate during firing.

is complete, the substrate is very fragile because the polymeric binders that rendered the material flexible have been removed. The substrate is then heated to the firing temperature and held for a few minutes. During this

In a Box Furnace

Co-fire, 875°C, 15min

5°C/min

Cooling
in the furnace

450°C

Ash, 350°C, 60min

3.3°C/min

6°C/min

6-layer substrate less than

4.5"x4.75" in area
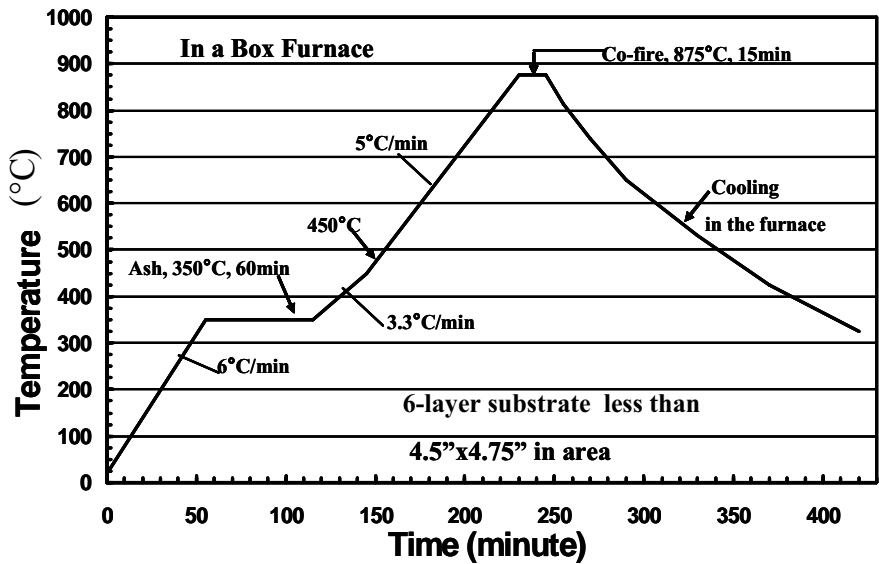
FIGURE 6.24
A typical LTCC firing profile.

second portion of the process, the materials in the substrate react, or sinter, to form the solid ceramic block that is the desired result. During this process, the powders that constitute the ashed substrate pack more closely together, resulting in shrinkage of the substrate in most material systems. This shrinkage generally occurs in all directions and ranges from 10 to 20%, depending on the material and the direction. The key for most applications is controlling or predicting this shrinkage so that the parts end up with the desired physical dimensions. Finally, the substrate is cooled to room temperature.

In contrast, belt furnaces offer much greater throughput because a continuous flow of substrates may be fired in this type of operation. The modern belt furnaces now offer very good control of process gases and temperature uniformity, thanks in large part to sophisticated computer control systems. Generally, these systems are very large and may be more than 20 ft in length because of the need for a large number of heated zones to ensure adequate temperature control. Whereas the firing process employed in the belt furnace is fundamentally different than the box furnace, the heating profiles may be very similar. In general, a belt furnace is capable of far greater heating and cooling rates than most box furnaces. This is because the box furnace must heat and cool the large amount of material that lines the furnace as well as the substrates to be fired with each cycle.

In either case, the proper furnace profile is important to achieve the desired final substrate density, as well as the desired mechanical and electrical properties. The substrate camber is also strongly affected in some material
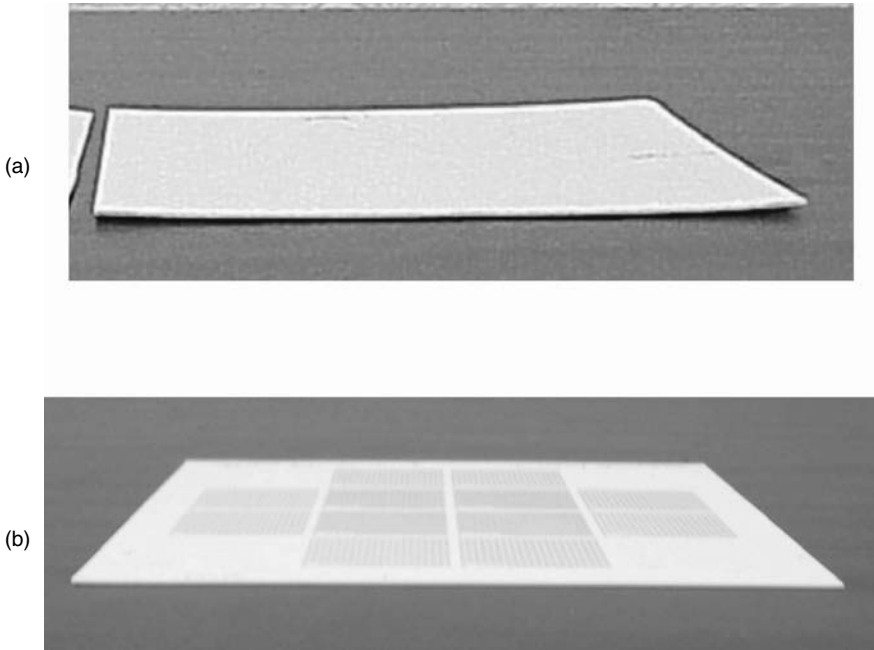
FIGURE 6.25
(a) An inappropriately fired LTCC substrate with significant chamber. (b) An identical substrate from the same material lot and design fired in an appropriate manner.

systems by the firing process. As shown in Figure 6.25a, inappropriately fired substrates can exhibit significant camber. However, when fired properly, the final substrates are generally very flat with a smooth surface finish as shown in Figure 6.25b.

6.2.10   Postprocessing

6.2.10.1   *Postfired Materials*

For any of a number of reasons, it may be necessary to add additional metallization to HTCC or LTCC packages. Such applications include those in which dimensional tolerances require postfire machining or polishing. Although a refractory tungsten metallization may be used for HTCC, the "moly manganese" process is commonly employed to apply conductors to these surfaces. MoMn can be applied using standard screen-printing techniques although, in certain applications, it may be applied by skilled technicians using manual painting. Image sensor substrates, as an example, may include large silicon arrays. To maintain precise optical alignment, the package must be very flat, often to less than 25 μm/in. These packages may be

cofired, polished to the requisite flatness, and then metallized with MoMn. These MoMn inks typically comprise roughly 10% Mn. This composition is screen printed onto an HTCC substrate and fired at a temperature of 1350–1400°C in moist-forming (dew point = 25°C) gas (75% H_2/25% N_2). Mn is an essential component of this metallization, serving as a flux for the diffusion of oxide phases from the base alumina ceramic into the Mo conductor [31]. Although the MoMn firing process is conducted at temperatures approximately 200°C below the HTCC firing temperature, distortion of the substrate may occur. Careful consideration of firing fixtures, temperature cycle, metal loading, etc., can minimize any warpage during MoMn firing. MoMn metallization may be plated with either electroless or electrolytic plating technologies and brazed to standard metals (FeNiCo, alloy 42, etc.).

Likewise, a number of applications require postprocessing of thick-film inks on LTCC. The most common postfired inks used in this manner are gold and gold–platinum compositions that are intended for wire bonding or brazing.

6.2.10.2 Substrate Machining

It is unusual for a panel of cofired ceramic to consist of only a single part. Generally, each substrate contains a number, perhaps hundreds, of individual, identical packages or components. As a result, a key step is the machining or singulation of this panel into the component parts. Two principal techniques are most commonly used; postmachining and premachining.

In many cases, the simplest machining solution is to premachine the parts while still in the green state. The advantages of this approach are the speed and simplicity of the operation because the ceramic is still very soft in its unfired state. An example of a low-volume hot-knife cutting system is illustrated in Figure 6.26. These systems generally use a heated stage and a heated carbide blade to cleanly slice through the polymer matrix that binds the unfired multilayer ceramic substrates. Machine vision is commonly used to locate the blade relative to punched or printed features on the substrate and thereby ensure accurate cuts. In some cases, lasers may also be used to premachine a cofired substrate. Clearly, the hot-knife systems can only perform straight cuts; however, lasers can be used to easily make intricate or round cuts.

Premachining, though generally easier to perform, has one major disadvantage in that it is not as accurate as postmachining. As the name implies, postmachining occurs after the substrate has been fired and the shrinkage has occurred. In many cases, a laser or diamond saw is the preferred method for dicing substrates after the firing process. A diamond-impregnated blade is required to cut these ceramics because many of them are very hard and would rapidly destroy a metal blade. Dicing saws, much like those used in the semiconductor industry for dicing silicon wafers, are commonly used.
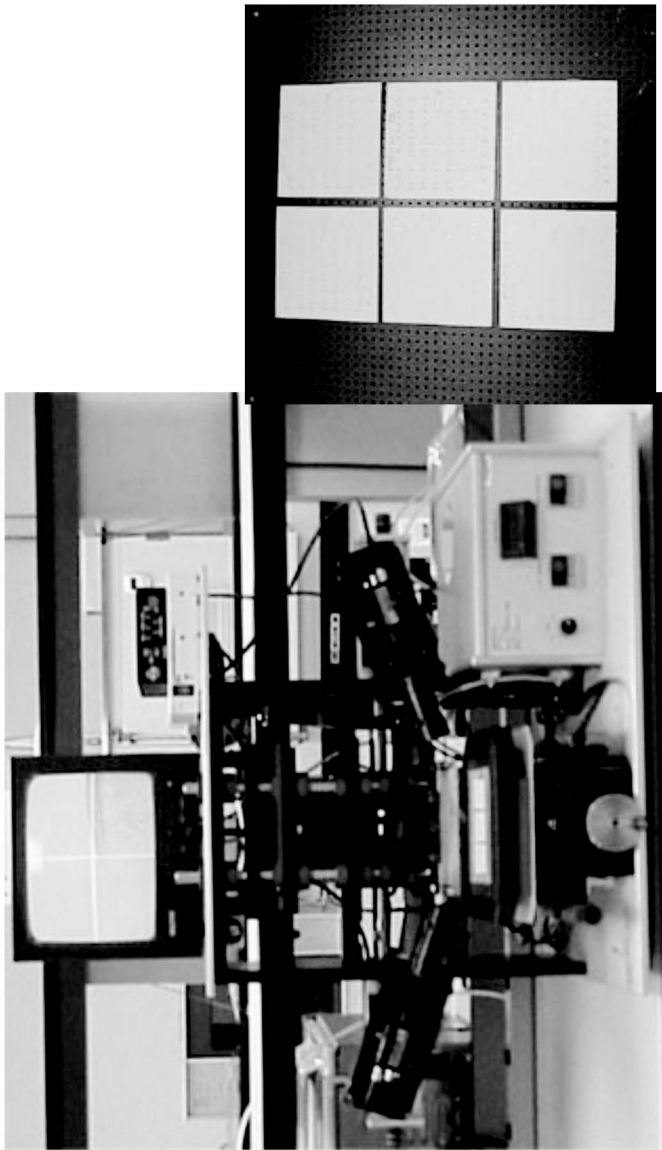
FIGURE 6.26
(Left) A typical low-volume green cutting system. This unit utilizes a heated stage and heated blade as well as machine vision to precisely cut green multilayer ceramic substrates. (Right) A pre-machined substrate produced with this system.
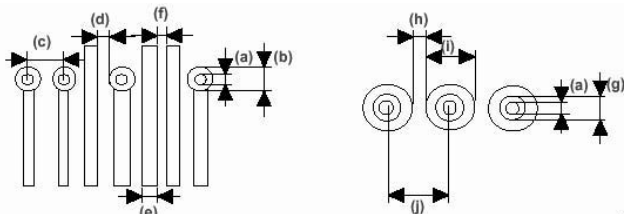
6.3   Design Considerations

The intrinsic multilayer approach of cofired ceramic offers many advantages to designers. Whereas it is possible to take a standard FR-4 design and build it in ceramic, in many cases, this approach misses many opportunities for reduced cost and improved performance. For example, blind and buried vias, which are not standard processes in low-end PCB designs, are very easy to implement in ceramic. In addition, there are a number of simple design rules that can radically improve the yields in the multilayer ceramic technology. For example, the use of via cover dots or capture pads, which are simply printed metal dots on top of each via in a given tape layer, are a common design feature. These capture pads are generally slightly larger in size than the vias and allow for a small amount of layer-to-layer misalignment without compromising the electrical integrity of the substrate.

6.3.1   Design Rules

Each manufacturer publishes a set of design rules, describing geometries and limitations achievable by their technologies. Typically, there are "standard" and high-precision technologies. For example, a set of design rules is displayed in Table 6.3. These capabilities are directly related to the

TABLE 6.3

Design Rules

unit : mm / inch

ITEM	CC200	CC100	CC075	CC050
(a).Via Hole Dia.	.203/.008 "	.102/.004 "	.076/.003 "	.050/.002 "
(b).Via Cover Dot Dia.	.381/.015 "	.152/.006 "	.127/.005 "	.102/.004 "
(c).Via Center Spacing	.635/.025 "	.254/.010 "	.203/.008 "	.152/.006 "
(d).Via Cover Dot to Line Clearance	.254/.010 "	.127/.005 "	.076/.003 "	.050/.002 "
(e).Line Width	.127/.005 "	.102/.004 "	.076/.003 "	.050/.002 "
(f).Line to Line Clearance	.127/.005 "	.102/.004 "	.076/.003 "	.050/.002 "
(g).Via Cover Dot Dia (on Plane)	.381/.015 "	.152/.006 "	.127/.005 "	.102/.004 "
(h).Line Width (on Plane)	.203/.008 "	.102/.004 "	.076/.003 "	.050/.002 "
(i).Clearance Dia.	.991/.039 "	.457/.018 "	.279/.011 "	.203/.008 "
(j).Via Pitch (on Plane)	1.118/.044 "	.559/.022 "	.356/.014 "	.254/.010 "

manufacturers' control of raw materials, tape casting, processing, and firing. Key features that are generally indicated in these design guides include: via size, via cover dot sizes, via spacing, space and trace restrictions for printed interconnects, and via clearance diameters for vias that pass through but are not electrically connected to ground planes. It is also common to specify the available tape thickness because several are often available in a given material system, as well as cavity sizes and spacing restrictions from the edge of the substrate. In many cases, these guidelines may specify the minimum as well as the maximum sizes that can easily be achieved in the manufacturing process. Whereas deviations from these design guidelines are sometimes possible, it is important to consider the yield ramifications for any such deviation. Chapter 2 and Chapter 3 provide a detailed discussion of design considerations from both an electrical and a thermal point of view.

6.3.2   Shrinkage Control

Shrinkage of the cofired ceramic due to the sintering process is occasionally cited as a problem with this technology. The key is to understand and control the process and material variables that lead to uncertainty in the shrinkage. This is highly dependent on the tape system in question; however, there are some design guidelines that can help minimize the effect of shrinkage variability. For example, balancing printed metal and via densities throughout a design can significantly reduce the potential for camber or a lack of uniformity in the shrinkage because the metal density affects the shrinkage of many of the material systems. In addition, tight material and process controls are very important because variations in the material composition, as well as process parameters, such as lamination pressure, can have a strong effect.

6.4   Cofired Materials

6.4.1   Cofired Inks

Two basic concepts for conductors in multilayer ceramics were developed: noble and refractory metals. Noble metals (Pt and Pd) are relatively expensive but may be fired in an air atmosphere. Refractory metals (W and Mo), on the other hand, must be fired in a reducing atmosphere to prevent oxidation. As recently as 1971, an industry-wide decision as to which concept to adopt had not been reached [32]. Initial cofired metallization at IBM comprised MoMn-based metallurgies [33] and these refractory metals are still in common use in the HTCC and MTCC technologies. However, the LTCC technology is now largely dominated by gold, silver, and copper. These metals are compatible with the low-firing temperatures of the LTCC systems

and offer superior electrical conductivity. Gold finds major use in aerospace and high-reliability applications due to its stability and oxidation resistance. Silver is much lower in cost and can be fired in air, making it very attractive for more cost-sensitive markets. Copper is also inexpensive but because of its strong affinity for oxygen, special inert firing atmospheres are required.

Silver tends to suffer from electromigration and therefore has not been widely adopted in most high-reliability applications even though it is far less costly than gold and, unlike copper, can be fired in air. To alleviate this problem, several material suppliers have developed mixed metal systems that allow the use of silver inside the cofired ceramic and gold on the external surfaces. By effectively encapsulating the silver in the ceramic the impact of electromigration is reduced.

Regardless of the metal selected, the inks used in these systems are not identical to those used on prefired alumina. These ink compositions must be tailored to be chemically compatible with the tape dielectrics during the sintering process and must offer the correct viscosity for the intended application. Generally, the material systems are offered with a range of inks for different applications, such as internal interconnects or via fill. For example, via-fill inks are generally more viscous than inks intended for printing interconnects, and ink designated for ground planes are sometimes lower in viscosity than those used for printing interconnects.

6.4.2 Dielectric and Metal Properties

6.4.2.1 Medium-Temperature Cofired Ceramics (MTCC)

In an attempt to marry the best characteristics of HTCC and LTCC, Kyocera has developed an intermediate-firing cofired ceramic, designated as *A0600*. This alumina material employs copper-based conductors. Thus, this composition enjoys the low electrical resistivity of Cu metallization along with the superior mechanical and thermal properties of alumina. A "broad-brush" comparison of this material to standard 92% alumina and a generic LTCC formulation is presented in Table 6.4.

TABLE 6.4

Comparative Properties of Alumina HTCC, MTCC, and LTCC

Properties	HTCC	MTCC (A0600)	LTCC
Base material	Polycrystalline Al_2O_3	Al_2O_3	Glass
Conductors	W	Cu/W	Cu, Ag/Au
Firing temp (°C)	1600	1350	900
Conductor resistivity (mΩ/sq)	10	3	3
Thermal conductivity (W/m·K)	20	16	2
Flexural strength (MPa)	400	400	200
Brazeability	Yes	Yes	No, yes

Consolidation of HTCC Al_2O_3 requires temperatures of approximately 1550°C. Pure copper melts at 1085°C and is therefore incompatible with HTCC firing temperatures. In the development of A0600, inclusion of refractory particulates within the metallization was found to significantly reduce the volatilization of Cu at temperatures above the melting point. At the same time, a sintering additive composition, resulting in a reduction of the Al_2O_3 sintering temperature to less than 1400°C, was identified.

6.4.2.2 Silicon Nitride

Silicon nitride (Si_3N_4) is a dielectric ceramic typically used as an amorphous passivation coating in wafer processing [34]. Monolithic, crystalline Si_3N_4 has also been applied to structural parts demanding high mechanical strength in demanding environments, such as those found in automotive and large engine turbines [35]. It has been investigated, however, as a substrate in electronic applications, because of its high strength and high fracture toughness. In contrast to the homogeneous microstructures of AlN and Al_2O_3, sintered β- Si_3N_4 exhibits elongated grains reflecting the preferred growth in the [001] direction. This microstructure promotes enhanced fracture toughness due to crack deflection and bridging.

Preparation of Si_3N_4 ceramics requires careful selection of raw powder, sintering additives, green fabrication methodology, and consolidation [36]. Densification is enhanced with the use of submicron (<0.5 μm) and high surface area (>10m^2/g) powders. In addition, raw powders comprising primarily α- Si_3N_4 lead to structures with the desirable acicular β-phase microstructure [37]. Si_3N_4, like AlN, is densified via a classic liquid phase sintering process. There is a considerable variety of sintering formulations used to prepare Si_3N_4 substrates. Most commercial versions, however, involve additions of Y_2O_3 and Al_2O_3 that combine to form a Y-Si-Al-O liquid phase during sintering. Consolidation is typically conducted at temperatures in excess of 1600°C in the presence of mechanical (hot pressing) or gas pressure (pressure-assisted sintering). As Si_3N_4 decomposes at high temperature, the use of high nitrogen pressures has been employed to suppress this dissociation.

Si_3N_4 parts may be fabricated by any of the standard green-forming techniques. Tape casting can lead to preferred orientations in fired structures [38]. This orientation results in nonuniformity of not only the mechanical properties of Si_3N_4 but also the thermal conductivity. High thermal conductivity Si_3N_4 has been demonstrated in tape-cast substrates, although the thermal processing required to produce these parts is rather onerous and probably not practical for electronic substrates [39,40]. After processing substrates containing 5 wt% Y_2O_3 at 2500°C for 2 h in 200 MPa of N_2, substrates with a thermal conductivity in excess of 150 W/m·K in the casting direction were demonstrated. Nonoriented, pressureless-sintered, electronic substrates, however, typically exhibit thermal conductivities of approximately 60 W/m·K.
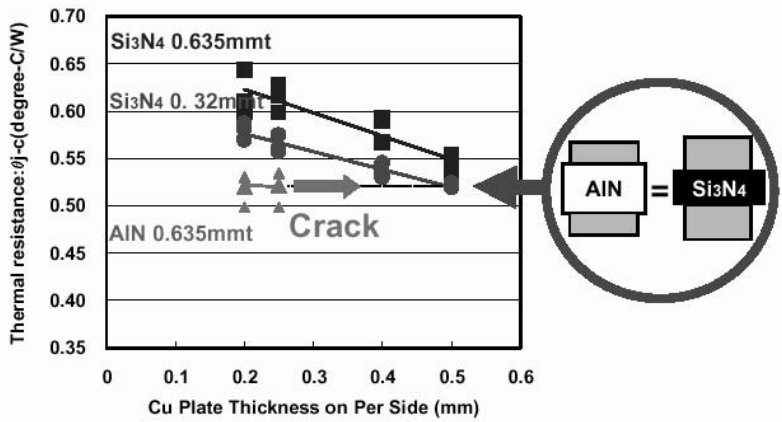
FIGURE 6.27
Thermal performance of Si_3N_4 and AlN active-metal brazed structures. With copper metallization above 0.25 mm in thickness, the AlN laminates fail as a result of the CTE mismatch and the lower flexural strength compared to Si_3N_4.

Cofired Si_3N_4 has not been described in the literature; however, multilayer structures (Cu- Si_3N_4) can be produced via active-metal brazing (AMB) technology. For high current-carrying applications, AMB on Si_3N_4 can offer improved thermal performance compared to higher thermal conductivity materials. Figure 6.27 compares the thermal resistance of AMB structures on AlN and Si_3N_4. The higher strength of Si_3N_4 allows the use of thicker bonded copper, improving both the current-handling capability and the thermal performance of the laminate.

6.4.2.3 BeO

Beryllium oxide (BeO) is, in many ways, a superior substrate for electronics. It possesses a high thermal conductivity, good mechanical and dielectric properties, and can be reliably metallized and brazed. It is available as tape-cast, dry-pressed, and hot-pressed substrates. In development, multilayer BeO has been demonstrated [41]. This potentially interesting material has not been introduced commercially, however. Production of tape-cast BeO substrates is similar to that employed in other HTCC substrates [42]. High-purity BeO (99.8%), with an average particle size of 1–2 μm is mixed with SiO_2 sintering aid and MgO as a grain-growth inhibitor, milled and tape-cast in standard processing equipment. However, inhaled BeO powder is toxic to susceptible individuals. Thus, special precautions must be adopted to prevent exposure to workers [43]. BeO is fired in a refractory metal furnace in a H_2-containing atmosphere at 1600–1800°C. Densities approaching 97% of theoretical can be readily achieved with tape-cast substrates.

BeO substrates are available with thin-film (TiW/Ni/Au) and refractory (MoMn) metallizations. Metallization–adhesion strengths are generally lower with refractory metallization: 134 MPa (tape-cast) and 115 MPa (dry-pressed) vs. 160 MPa (tape) and 150 MPa (pressed) observed with thin-film metallization [42]. BeO can be brazed to a variety of heat sink, lead, and seal ring materials, including both metals and ceramics.

6.4.2.4　Multilayer Aluminum Nitride

AlN is a synthetic material first produced in the late 1800s. Interestingly, one of its first commercial applications was as a fertilizer [44]. It was not until the late 1980s that AlN was first demonstrated as a viable and useful electronic substrate [45]. AlN has an excellent set of dielectric properties; the key one among these is its thermal conductivity. Development of a high thermal conductivity structure depends on three factors: high-quality raw powders, optimized sintering aid formulations, and specialized firing conditions [46,47]. Monolithic AlN, with a thermal conductivity as high as 285W/m·K, has been reported [48]. Achievement of ultrahigh thermal conductivity in multilayer packages, however, is not practical.

Cofired AlN involves similar green processing to HTCC alumina. As noted above, the use of a high-purity powder (low O, Si, and Fe) and sintering aids with a high affinity for oxygen (lanthanum-group [Y_2O_3] or alkaline earth [CaO] oxides) is necessary to achieve high thermal conductivity. Unlike alumina, AlN is densified via a liquid-phase sintering process. The sintering aids react with oxides on the particle surfaces to form aluminates, (e.g., yttrium or calcium aluminate), which promote densification, beginning with rearrangement at ~1350°C followed by diffusion-controlled densification upon formation of the sintering liquid — 1760°C in the case of yttrium aluminate [49]. The "purification" process in which oxygen and impurity atoms diffuse to the grain boundary regions is necessary for high-thermal-conductivity parts and typically requires high temperature and long sintering times. The yttrium aluminate second phases are located in the grain boundary regions. The chemistry and distribution (triple grain junctions, wetting angles, etc.) are both reflective and related to the thermal conductivity of the ceramic.

Tungsten metallization, with appropriate particle size and additives to control shrinkage rate and temperature, is employed for buried, surface, and via conductors. Typically, binder burnout and sintering are conducted in separate process steps. As AlN is susceptible to hydrolysis, binder burnout does not involve the use of moist atmospheres to facilitate binder removal. Thus, trace amounts (0.2%) of residual carbon may be retained in the ceramic prior to sintering. This carbon has both beneficial and deleterious effects. It acts to remove oxygen through the carbothermal reduction of aluminum oxides, increasing thermal conductivity. At the same time, excess carbon can impede sintering by chemically reducing the sintering aid aluminates that are essential for densification. Futhermore, carbon can react with the W
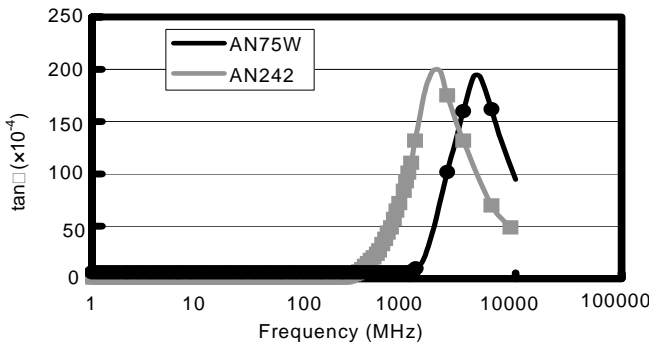
FIGURE 6.28
Frequency dependence of dielectric loss in multilayer AlN substrates.

metallization to form WC compounds that decrease the electrical conductivity of the conductor metallization [50].

Multilayer AlN is consolidated either by pressureless sintering or hot pressing. Hot-pressed parts use CaO-based sintering aids and are pressed in a boron nitride-coated graphite die. After sintering, the surfaces are ground and thin-film metallization is applied [51]. Pressureless sintered AlN multilayers are fired in refractory metal furnaces at approximately 1800°C. The parts must be enclosed in setters, either AlN or tungsten, to preserve an atmosphere that stabilizes the aluminate sintering liquid.

Multilayer AlN packages are available from a number of vendors. The thermal conductivity of these materials varies from 75 to around 200 W/m·K. The refractory metallization can be plated and brazed with high reliability. However, reliable postfire metallization is limited to thin-film and noble-metal compositions. Good refractory (W or Mo-Mn) metallizations have been promoted by several suppliers.

The use of AlN in high-frequency (>1GHz) applications is somewhat limited. One reason is the unusual piezoelectric behavior of polycrystalline AlN, which depends on the average grain size in the fired ceramic [51]. As shown in Figure 6.28, this resonance results in a significant spike in the observed dielectric loss for two commercial AlN compositions. The finer-grained AN75W exhibits a loss peak at 2 GHz whereas the coarser-grained AN242 exhibits its peak at about 8 GHz.

6.5 Future Trends

Some of the general trends in substrate technology are toward finer lines and spaces as well as the desire for nontraditional structures such as those

used in MEMS devices. One of the drivers behind these trends is the need for higher levels of electrical functionality within the same or smaller product form factors. These applications demand finer lines and traces because the interconnect density is inversely related to the size of the interconnects in both the horizontal plane (printed traces) as well as the vertical planes (vias). Another is the emergence of a larger number of applications in the micro-wave and millimeter bands. Interconnects, dielectric layers, and vias must be significantly smaller, often ten or more times smaller, than the wavelength of the signal of interest. At the high end of the microwave and in the milli-meter band, smaller interconnects with tighter tolerances are required. In addition, some of the MEMS structures require fluid channels and other exotic structures that have not traditionally been created in ceramic sub-strates. Finally, modern ceramic packages demand integration, requiring the inclusion of standard electrical functions such as resistors, inductors, and capacitors. A number of suppliers are developing high-k materials that can be embedded in these packages. These components offer the flexibility of integration functionality that can be used to create filters, baluns, couplers, diplexers, and a variety of other components into the multilayer ceramic material.

However, multilayer ceramics are well poised to provide solutions to these problems because of the intrinsic three-dimensional nature of this technol-ogy, the stable dielectric properties relative to frequency changes, and the ability to easily integrate fluidic and mechanical structures within the dielectric.

For example, the development of high-mesh-count screens and microvias in multilayer ceramics has recently allowed for much higher densities of interconnects than was traditionally the case [52–54]. These same technolo-gies also enable the tight tolerance fine lines that are required by high-frequency designers [53–55]. Finally, there has been tremendous activity in the last few years regarding the use of microfluidic and MEMS-based devices based on multilayer ceramic materials [57,58].

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7

Photo-Defined and Photo-Imaged Films

William J. Nebe and Terry R. Suess

CONTENTS

7.1 Introduction

A major fraction of ceramic devices containing small-diameter dielectric vias and/or fine-line conductors are prepared using the screen-printing process. Screen-printing technology, as applied to image generation, is an ancient art. This technology, which in many respects still remains an art today, has numerous applications, ranging from electronics to the preparation of multicolored, artistically beautiful images, to T-shirts that advertise most facets of human activities. The generation of patterned ceramic images for electronic applications using screen-printed thixotropic pastes of varying conductivities is a significant technological development of the past century.

This methodology for electronic pattern preparation, where conductor line widths of 4–10 mil and dielectric via diameters of 6–10 mil are possible, has resulted in a new generation of sophisticated electronic devices. However, as with all electronic applications, the desire and need for additional miniaturization has necessitated the search for narrower conductor line widths and reduced via diameters. This quest is hindered by the limitations of screen-printing technology. Clearly, the wire diameter and integrity of the screen limit the line widths and, especially, via diameters, which can be obtained using a thixotropic paste (Figure 7.1).

Screen Printing Diagram

- Squeegee moves ink across and through screen mesh
- Emulsion defines and gaskets printed pattern
- Mesh count, wire diameter, and emulsion affect deposit
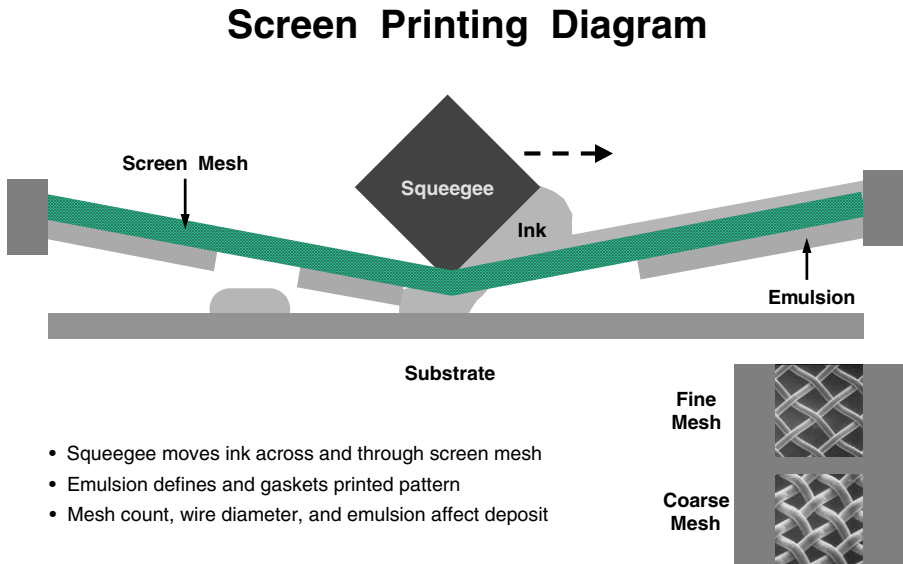
FIGURE 7.1
Screen printing. (Figure courtesy of DuPont and Co.)

The recent combination of screen printing and photolithography using photosensitive pastes has resulted in increased image resolution and acuity, giving conductor line widths of ≥35 μm and dielectric via diameters of ≥50 μm. As will be discussed in detail, this technology entails the application of a photosensitive paste to a ceramic substrate by screen printing (doctor-knife application is used in some cases), followed by photographic generation of the desired image. The screen-printing method of application involves coating the entire substrate with a photocurable paste having Newtonian or mildly thixotropic rheology [1]. The resulting coating, after leveling and drying to remove the solvent, yields a smooth, tack-free film that can be imaged and developed. The normal screen-printing mesh marks of a highly thixotropic paste are not present. This technology has found extensive use in electronic and display applications. As illustrated in Figure 7.2, the use of a photo-curing step dramatically improves image quality vs. screen printing. One of the primary differences seen in Figure 7.2, is the very precise edge quality provided by the photo-curing process as compared to traditional screen printing.
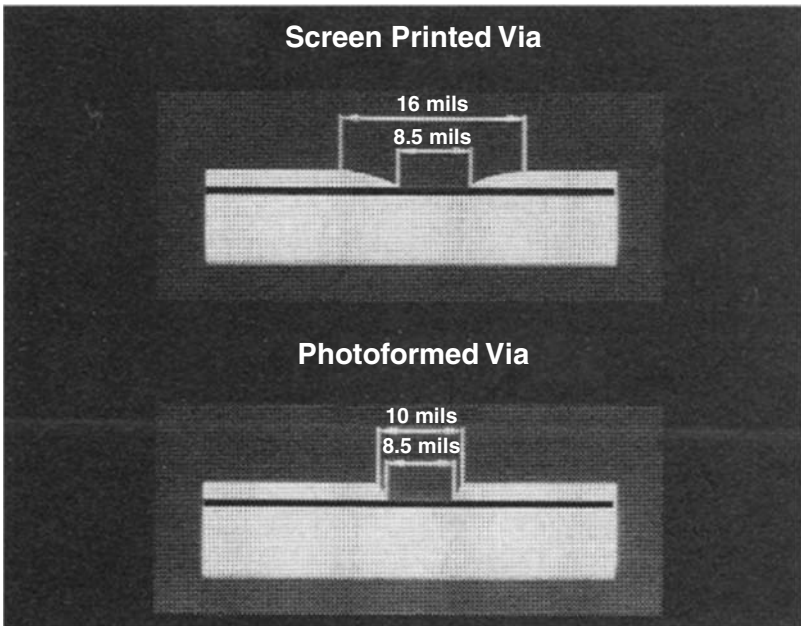
FIGURE 7.2
Screen printed vs. photoformed vias. (Reprinted from The American Ceramic Society, www.ceramic.org. With permission. Copyright 1990. All rights reserved.)

7.2 Photo-Imaged Ceramic Processes

As discussed in Section 7.1, the combination of ceramic technology with imagewise photopolymerization can be used to prepare electronic devices with high resolution.

Ceramic processes such as thermal sintering have been known and practiced since antiquity. By comparison, photopolymerization is a relatively modern technique, although the first products using this technology were introduced more than 50 years ago. The combination of ceramic and photopolymerization technologies in modern electronic applications is more recent. As this combination of photochemistry and, in particular, photopolymerization with ceramics is relatively new, a brief discussion of the application of photochemistry as used in photopolymerization is in order.

Photochemistry is probably the most essential process for life as we know it. At the risk of gross impertinence, one of the first references to illumination is from the book of *Genesis*, "And God said 'Let there be light' and there was light. And God saw the light, that it was good" [2].

Light energy is a critical ingredient in some of the most important natural and modern technological processes. Among these are photosynthesis, cosmic studies, vision, photography, xerography, biological studies, television, and photopolymerization.

The science of photochemistry [3] entails the molecular absorption of electromagnetic radiation of wavelengths ranging from approximately 1,500 to 10,000 Å, and the subsequent reaction or decomposition of the resulting excited molecules (Figure 7.3). The fate of the excited molecules may follow a number of paths:

$$h\upsilon + S_0 \longrightarrow S_1 \qquad \text{Exitation}$$
$$S_1 \dashrightarrow S_0 + heat \qquad \text{Internal Conversion}$$
$$S_1 \dashrightarrow T_1 + heat \qquad \text{Intersystem Crossing}$$
$$T_1 \dashrightarrow S_0 + heat \qquad \text{Intersystem Crossing}$$
$$T_1 \longrightarrow S_0 + h\upsilon \qquad \text{Phosphorescence}$$
$$S_1 \longrightarrow S_0 + h\upsilon \qquad \text{Fluorescence}$$
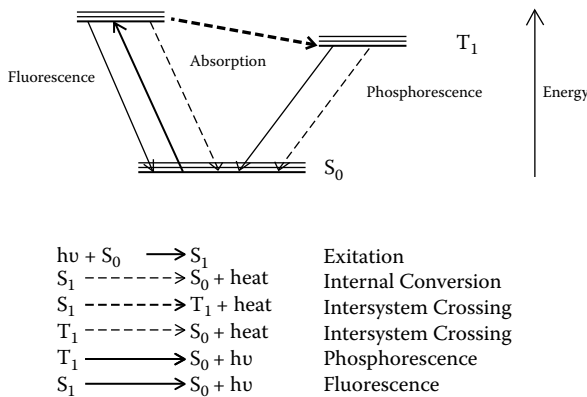
FIGURE 7.3
Excited state photochemistry. (Reprinted from The American Ceramic Society, www.ceramic.org. With permission. Copyright 1990. All rights reserved.)

1. An excited molecule can emit energy from its singlet state as it returns to its ground state by losing energy in the form of heat, internal conversion, and/or light fluorescence.

2. The excited molecule can cross over to its triplet state (intersystem crossing), and from its triplet state, lose energy in the form of heat (internal conversion) and/or light phosphorescence, as it returns to its ground state.

3. The excited singlet or triplet molecule can break a chemical bond (photolysis) (Figure 7.4), in turn reacting with another molecule, as will be discussed in Section 7.3.

4. An excited molecule can also transfer its energy to another molecule (sensitization), as will also be discussed in Section 7.3.

There are numerous examples of fluorescence and phosphorescence resulting from the UV light excitation of materials. Among these are the visible light emitted by many minerals when exposed to UV light, and the use of UV light to detect traces of blood in forensic investigations at crime scenes. One of the more esoteric examples of this photochemical characteristic is the location of scorpions at night. They emit strong visible light when exposed to ultraviolet light. Because of the risks involved, the authors do not recommend scorpion location as a test of this photochemical phenomenon.
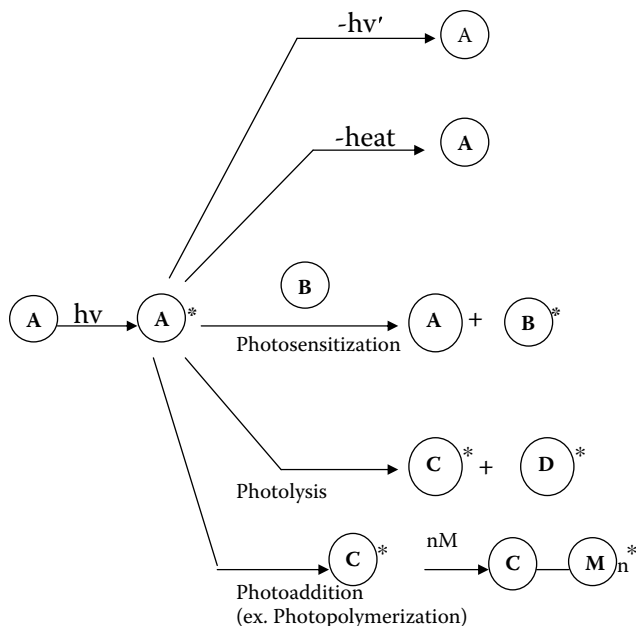
FIGURE 7.4
Photochemical reaction and excitation pathway.

A unique feature of photochemistry is that energy put into a molecule can be controlled by selection of the wavelength of the irradiating light. Many photosensitive materials have excellent shelf life. The activating agent, light, can be readily excluded until reaction is initiated by irradiation. The application of photochemistry to generate an excited molecule, which subsequently breaks into radicals and reacts with monomers to start a chain polymerization, is the basis of photopolymer chemistry. The many pathways and forms of energy dissipation from the excited molecules are because of its structure and environment and are beyond the scope of this discussion.

7.3   PhotoPolymerization

The mechanism of photopolymerization in many application, generally involves the light-induced activation of a sensitizer material, such as an aromatic ketone, for example, Michler's ketone or a polyaromatic, to its singlet state, followed by crossover to form its triplet-excited state, followed by energy transfer to an initiator. The activated initiator usually splits into two radicals, one or both of which react with the monomer causing polymerization to occur. Norrish type I and type II reaction mechanisms are examples of this science [3]. Acrylates and methacrylates are commonly the monomers of choice because of their high polymerization rate, low cost, and acceptable toxicity (Figure 7.5). Additionally, acrylates and methacrylates

Sensitization	$S \xrightarrow{hv} S^* \xrightarrow{I} S + I^*$
Initiation	$I \xrightarrow{hv} I^*$
Radical Formation	$\mathbf{I^* + RH \longrightarrow IH\bullet + R\bullet}$
Chain Propagation	$R\bullet + nM \longrightarrow R(M)_n\bullet$
Termination	$R(M)n\bullet + R(M)m\bullet \longrightarrow R(M)n+mR$
Inhibition	$R(M)n\bullet + O_2 \longrightarrow R(M)n\ OO\bullet$
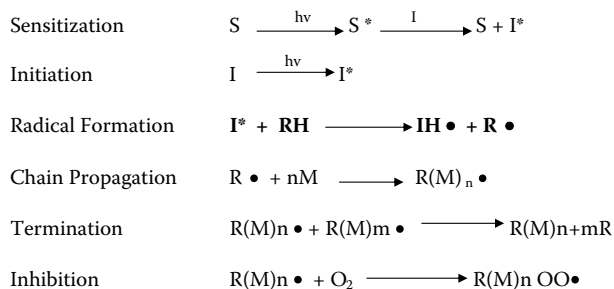
S = sensitizer, ex: Michler's Ketone
S* = photoactivated sensitizer
I = initiator, ex. Benzophenone
I* = photoactivated initiator
RH = radical source, after loss of hydrogen radical will become R• radical
M = monomer, ex: acrylate or methacrylate
R(M)n• = intermediate polymer chain with live radical end
R(M)n+mR = completed polymer
R(M)nOO• = unreactive peroxy radical which inhibits further polymerization

FIGURE 7.5
Mechanism of photopolymerization.

$$I\bullet \;+\; \underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{\displaystyle H\quad\; H}{C=C}}_{H} \longrightarrow I-\underset{H}{\overset{H}{C}}-\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{H}{C}}\bullet$$

$$I-\underset{H}{\overset{H}{C}}-\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{H}{C}}\bullet \;+\, n\,\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{H\quad\; H}{C=C}}_{H} \longrightarrow I-\underset{H}{\overset{H}{C}}-\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{H}{C}}\!\!\left(\!C-\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{C}\!\right)_{\!n-1}\!\!\underset{H}{\overset{H}{C}}-\underset{\underset{\displaystyle O}{\overset{\displaystyle \|}{COR}}}{\overset{H}{C}}\bullet$$
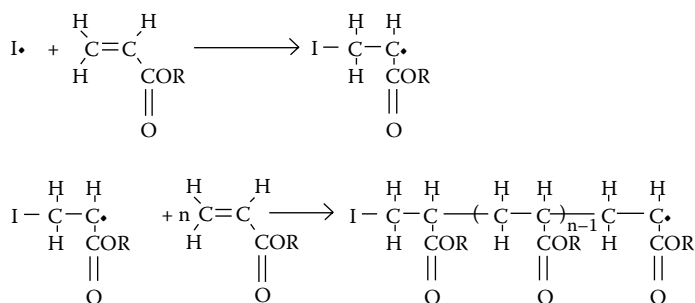
FIGURE 7.6
Mechanism of radical polymerization of acrylates. (Reprinted from The American Ceramic Society, www.ceramic.org. With permission. Copyright 1990. All rights reserved.)

readily and cleanly degrade to gaseous products under low-oxygen firing conditions when the photopolymer composition is used in a thick-film formulation (Figure 7.6). Epoxides, vinyl ethers, and acrylamides are also cured by photopolymerization; however, none of these have the advantages discussed earlier for acrylates and methacrylates.

Photopolymerization compositions generally contain preformed polymers, known as binders, which are used to give the unexposed composition higher viscosity and other desired physical characteristics. The binders, in combination with the polymerized monomer give desirable property changes in the exposed material, such as differential solubility, which permits development of the exposed substrate, durability, and adhesion to the substrate. Common binders are polyacrylic and polymethacrylic acids, poly-acrylates, polymethacrylates, polyethers, polydienes, polyacetals, polystyrene, and copolymers of these materials. Photopolymerizable compositions also contain stabilizers to prevent polymerization before exposure. Common stabilizers, such as the hindered phenols, 4-methoxyphenol, and 2,6-di-*t*-butyl-4-methylphenol, give a shelf life from 1 to 2 years. Additionally, plasticizers, surfactants, antifoam agents, colorants, insoluble organic or inorganic fillers, olfactants, etc., are also employed.

The photopolymerizable compositions used to prepare electronic devices are exposed using UV light (Figure 7.7). UV light-sensitivity allows handling of these materials in short-wavelength visible light environments, e.g., yellow light. This is more convenient than the darkroom conditions, e.g., red light, needed for visible light sensitive materials such as silver halide compounds. Wavelengths of between 2500–4000 Å are normally used as these are readily available from mercury or mercury/xenon lamps and UV lasers.

The efficiency of the rate of a free-radical polymerization is markedly and adversely affected by the presence of oxygen. This is because of the ability of oxygen to act as an excellent free-radical trap, reacting with sensitizer, initiator, monomer, and polymer radicals, giving a stable and therefore unreactive peroxy radical. The peroxy radical, because it is unreactive, stops the polymerization. Only when the oxygen has been consumed by reaction with

EXPOSURE **The monomer forms a 3-dimensional crosslinked polymer network in the areas exposed to light. This network encapsulates all other components.**

PHOTOMASK

PASTE
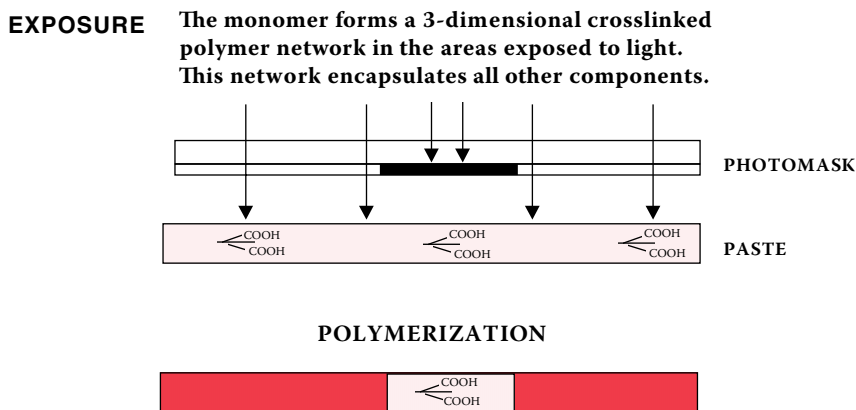
POLYMERIZATION

FIGURE 7.7
Exposure process. (Figure courtesy of DuPont and Co.)

the sensitizer, initiator, or other radicals can polymerization proceed uninhibited (Figure 7.8). Because of this oxygen-generated induction period, the photographic speed of free-radical polymerization is slower than a silver halide imaging system. The induction effect, plus the UV sensitivity of the compositions as discussed in the previous paragraph, permits processing of photopolymerizing compositions in yellow light ($\geq$4000 Å) of intensity comparable to normal room light. This facilitates handling of these compositions under near-normal working conditions. These photopolymerizable compositions are normally developed using an organic or basic aqueous solvent, depending on the formulation of the imaged material. In addition to solubility changes, other photopolymer systems may be patterned by changes in tackiness, adhesion, diffusion, refractive index, and other properties. Figure 7.8 shows the effects of different physical property changes vs. extent of polymerization.

The combination of photochemistry and polymerization science has resulted in the development of photopolymerization technology. The additional combination of photopolymerization and optics (photomasks) permits the generation of polymeric material in specific patterns. With the aid of photomasks, lenses, lasers, etc., photopolymerization can be induced in specific patterns, allowing generation of an image. The ability to selectively change materials, particularly to cause irradiated material to become insoluble, is the basis of the present discussion [5–7]. The combination of photopolymerization chemistry with thick-film ceramic technology is used to produce fine-line conductors and small-diameter dielectric vias, which can be used in conjunction with microchip packaging and printed circuit board manufacture [8].
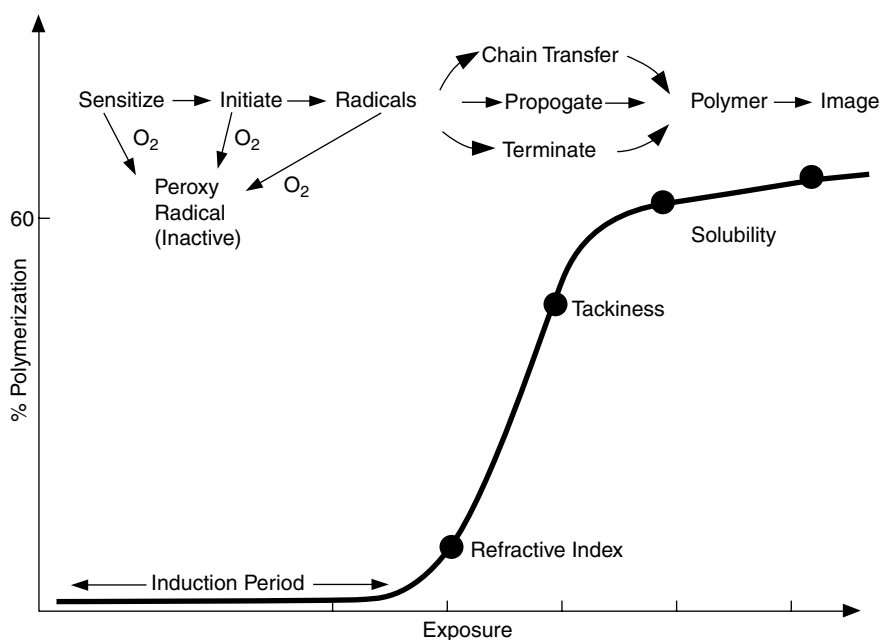
FIGURE 7.8
Physical changes as determined by extent of photopolymerization after oxygen depletion. (Reprinted from The American Ceramic Society, www.ceramic.org. With permission. Copyright 1990. All rights reserved.)

7.4 Photo-Formed Ceramic Compositions, Developed Using Organic Solvents

A description of the application of ceramic and photopolymer technologies to achieve high-resolution electronic patterns follows. The first section discusses ceramic dielectric vias, and the second, conductive circuitry. Improved photosensitive ceramic coating compositions and more particularly, compositions that function as precursors to fired dielectric ceramics, are mainly useful in preparation of multilayer thick-film substrates.

This work describes a photosensitive ceramic coating composition [9] that can be fired in either an oxidizing or a nonoxidizing atmosphere. The composition includes: (1) finely divided particles of high-melting ceramic solids having a surface area-to-weight ratio of less than 10 m^2/g, the majority of the particles having a size of 1–10 µm and (2) finely dispersed particles of an inorganic binder, such as a glass frit, having a similar surface area-to-weight ratio and particle size. The weight ratio of inorganic binder to the ceramic solid is generally in the range of 0.6–2. These materials are dispersed

in an organic medium composed of an organic polymeric binder selected from a group consisting of homopolymers and copolymers of alkyl acrylates, alkyl methacrylates, and α-methylstryrene. Additionally, homopolymers and copolymers of alkyl mono-olefins and homopolymers, and copolymers of alkylene oxide and mixtures can be used. Compositions of binders in the range of 5–25 wt% basis of the total inorganic solids (e.g., ceramic and glass frits) are effective. A photoinitiation system dissolved in a photohardenable monomer and volatile nonaqueous organic solvent is also present in these compositions that are designed for screen printing.

The formulation is processed by screen printing the composition to a ceramic substrate, removing the solvent by drying, followed by exposure to imagewise actinic radiation, to effect hardening of the exposed areas of the film. A developer solvent, such as 1,1,1-trichloroethane, is used to remove unexposed areas of the film, followed by firing in a substantially oxidizing or nonoxidizing atmosphere to effect volatilization of the organic medium and sintering of the inorganic binder and ceramic solids.

A major disadvantage of this procedure is that the formulations use a chlorinated organic solvent to develop the material after imagewise exposure to actinic radiation, i.e., an organic solvent removes areas of the composition that have not been exposed to actinic radiation without removal of areas that have been exposed. Although this technology yields a marked improvement over screen printing, the use of the chlorinated organic solvent is environmentally undesirable.

7.5   Aqueous Developable Formulation

An improvement on the organic development technology described earlier uses aqueous development [10]. As with the organic developable compositions, it includes a mixture of finely divided particles of high-melting ceramic solids having a surface area-to-weight ratio of no more than 10 m^2/g and at least 80 wt% of the particles having a size of 1–10 μm. Additionally, the composition contains finely divided particles of an inorganic glass frit binder having a glass transition temperature in the range of 400–825°C, a surface area-to-weight ratio of no more than 10 m^2/g, with at least 90 wt%, of the particles having a size of 1–10 μm. The weight ratio of inorganic binder to ceramic solids in general ranges from 0.6 to 2. These inorganic materials are dispersed in an organic medium including an organic polymeric binder and a photoinitiation system, photohardenable monomers, and a volatile organic solvent. Additional materials such as surfactants, colorants, and antifoam agents can also be used.

The organic portion of the composition constitutes an organic polymeric binder containing a copolymer or interpolymer of an alkyl acrylate or alkyl methacrylate, styrene, substituted styrene, or combinations of these

materials. The binder, or binders mentioned earlier, contain carboxylic acid functionality to allow development in basic aqueous solution. In these compositions, the carboxylic acid containing portions of the polymer is at least 15% of the total polymer composition, and may be as much as 30 wt%. It is advantageous that the weight-average molecular weight of the binder be less than 50,000. The composition, upon imagewise exposure to actinic radiation, is developable in an aqueous solution containing ≤ 2 wt% weight sodium carbonate. The use of an acid-containing binder, which during development in aqueous base forms the water-soluble salt, results in environmentally desirable development. The technology also yields improved resolution vs. systems designed to develop in organic solutions.

As discussed in earlier text, the aqueous developable formulation is similar to the organic developable formulation in that both contain ceramic materials and glass frits. This is necessary to achieve the required electronic, thermal, and physical properties of the electronic devices being prepared. The major difference is the aqueous base soluble binder, which allows aqueous development (Figure 7.9) [11,12].

7.5.1 Ceramic Solids: Filler

Ceramic solids are employed in many high-melting inorganic materials used in electronics. They are particularly suitable for making dispersions of dielectric solids, for example, alumina, titanates, zirconates, and stannates. They are also applicable as precursors of solid materials, which upon firing, are converted to dielectric solids and to mixtures of any of these. Among the many dielectric solids that are likely to be used are Al_2O_3, $BaTiO_3$, $CaTiO_3$, $SrTiO_3$, $PbTiO_3$, $CaZrO_3$, and $BaZrO_3$. It is desirable that the ceramic solids not have swelling characteristics in the organic dispersion because this would significantly alter the rheological properties of the dispersion.

Generally, the dispersion should contain no solids having a particle size of less than 0.2 μm, to obtain complete burnout of the organic medium when the coatings are fired. Firing removes the organic materials and permits sintering of the inorganic binder and the ceramic solids. Best firing performance is achieved when the ceramic solids do not exceed 20 μm and at least 80 wt% of these solids have a size of 1–3 μm. Clearly, when the formulation is prepared to make a thick-film paste applied by screen printing, the maximum particle size must not exceed the thickness of the screen or the open mesh size. When the dispersion is used to make a dry photosensitive film, the maximum particle size must not exceed the thickness of the film. Generally at least 80 wt% of the ceramic solids fall within the 1–10 μm size range.

The surface area/weight ratio of the ceramic particles should not exceed 10 m^2/g, as smaller particles tend to adversely affect the sintering characteristics of the accompanying inorganic binder. Ceramic particles having a surface area-to-weight ratio of 1–5 m^2/g are generally considered optimum.

PROCESSING SEQUENCE

PASTE
APPLICATION
SCREEN PRINT/
DRY (80°C)

COATING

SUBSTRATE

LENS

EXPOSURE

COLLIMATED U/V LIGHT

PHOTOMASK

CONVEYORIZED DEVELOPER SYSTEM

DEVELOPMENT
(1% Na$_2$CO$_3$)

VIAS

FIRING
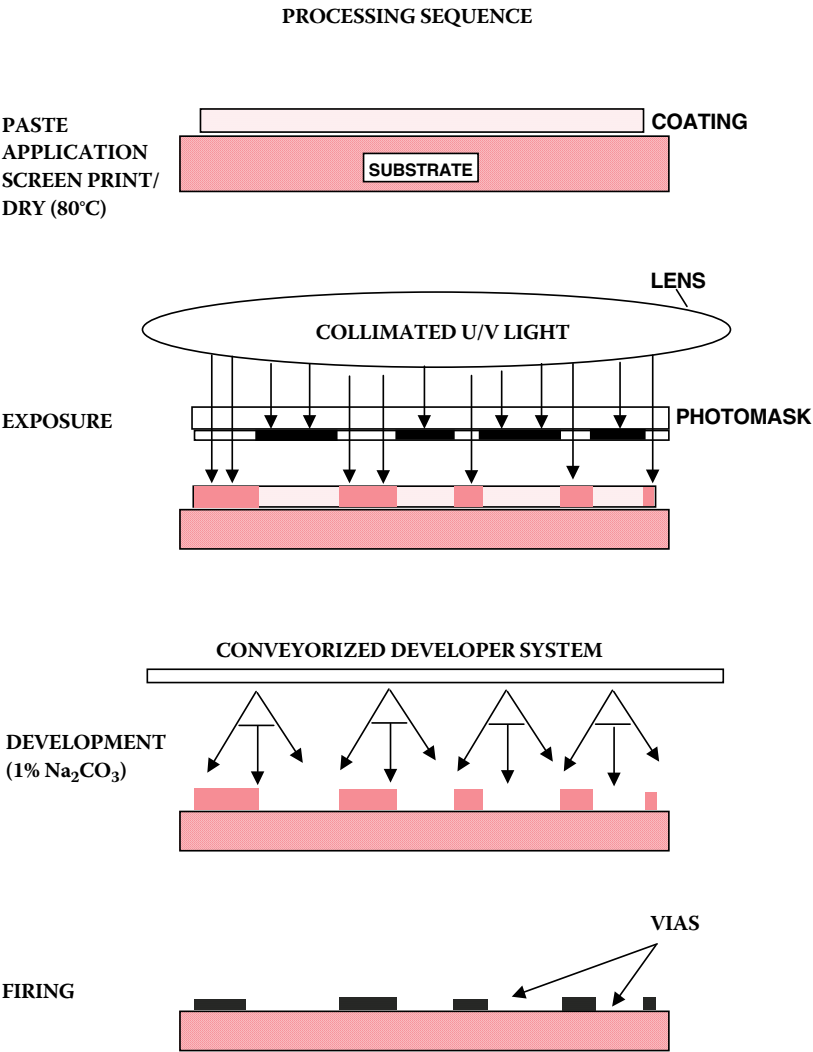
FIGURE 7.9
Processing sequence. (Figure courtesy of DuPont and Co.)

A widely used ceramic material for dielectric applications is alumina. The alumina may be milled and passed through a fine mesh screen (i.e., 400 mesh) to remove large particles. It can also be passed through a magnetic separator to remove all magnetic conductive materials, which would increase the conductivity of the final dielectric product.

It is of critical importance to achieve an agglomerate-free ceramic solid composition. Normally in the case of wet milling, after milling a ceramic to achieve the desired particle size distribution, the milling solvent is removed by either vacuum-assisted heating or heating in an air stream. This technique

can result in some of the ceramic particulates becoming agglomerated. Agglomerates may cause large particulate clusters or blisters after firing. Freeze-drying the wet milled ceramic solids eliminates this disadvantage. The mild conditions of freeze-drying minimize the probability for agglomeration that can result when powders are heated (Figure 7.9) [9].

A colorant may be added to the dielectric composition. This yields a paste that is much easier to process (i.e., coat, expose, develop, and fire) than a clear paste. Many inorganic pigments may be employed for this purpose.

Ogata et al. [13] suggest that matching the refractive index of the inorganic powders, including filler and glass frit, to the refractive index of the photosensitive organic components is critical to achieve a ceramic package with a high aspect ratio. They suggest a simple formula to calculate the required refractive index matching: $-0.005 \leq N_2 - N_1 \leq 0.10$. In this formula, $N1$ represents the average refractive index of the organic components of the formulation and $N2$ represents the average refractive index of the inorganic powders. Refractive index matching of all the components in the formulation will reduce light scattering, providing a higher aspect ratio in the photo-imaged pattern. This may be especially important for photosensitive ceramic green sheets, the subject of the Ogata patent.

7.5.2 Inorganic Binder: Glass Frit

Glass frit aids in sintering the mixture of inorganic crystalline ceramic particulates, forming a hermetic ceramic body. The frit must have a melting temperature below that of the peak firing temperature to achieve adequate hermeticity. A glass transition temperature (T_g) of the inorganic binder frit between 475°C and 750°C is recommended for a firing temperature of 850–900°C. A melting point below 450°C usually causes the organic material to be encapsulated, resulting in blisters forming in the dielectric layer as the organics decompose. A glass transition temperature above 825°C can result in poor adhesion to the substrate, when fired at 850–900°C. Products designed for lower firing-temperature applications need to use glass frits with glass transition temperatures 50–75°C below the peak firing temperature.

Borosilicate glasses, such as lead borosilicate, barium, calcium, bismuth, or other alkaline earth borosilicate frits are desirable because they can be efficiently processed and sintered in the temperature range of 475–750°C. Preparation of the glass frit consists of melting mixtures of the constituents of the glasses as their oxides and quenching the molten composition to form the frit. Frits are typically quenched in a water bath or on chilled rolls. The melt ingredients may be any compound that yields the desired oxides under the conditions of frit preparation. For example, boric oxide will result from boric acid, barium oxide from barium carbonate, etc. The glass is then milled to reduce particle size and obtain a frit composition of substantially homogeneous size.

The frit is processed in a manner similar to that discussed for the ceramic solids. It can be sieved through a fine mesh screen to remove large particles to assure the formulation is agglomerate-free. As with the ceramic solids, the inorganic binder or glass frit should have a surface area-to-weight ratio of no more than 10 m^2/g, with at least 90 wt% of the particles having a particle size between 1 and 10 µm.

Optimum results are obtained where the d50 (d50 indicates equal parts by weight of both larger and smaller particles) of the frit is equal to, or less than, that of the ceramic solids. Therefore, for a given particle size of ceramic solids, the inorganic binder/ceramic solids ratio required to achieve hermeticity will decrease as the inorganic binder size decreases. If the ratio of inorganic binder to ceramic solids is significantly higher than that required to achieve hermeticity, the fired dielectric will be porous and not hermetic.

Given these particle size and surface limits, it is best that the inorganic binder particles be 0.5–6 µm in size. Smaller particles have a higher surface area, which tends to absorb the organic materials, especially during the presintering stage and thus impedes clean decomposition. Larger-size particles tend to have poorer sintering characteristics.

7.5.3 Photoinitiation System

The technology elements discussed in the previous section, ceramic solids and inorganic binder, are necessary to achieve the needed hermetic, electrical, and other physical properties required for electrical applications. These elements are common to screen-printed and photo-defined ceramics. Photoinitiators and their attendant sensitizers, etc., are required to achieve adequate patterning resolution for new electronic applications. Suitable photoinitiation systems are those that are thermally inactive, having a shelf life of at least 1 year, but which generate free radicals upon exposure to actinic light. As already mentioned in the discussion on photochemical mechanisms, adequate shelf life of the formulation before the impingement of light is an extremely important characteristic of this technology. Thermal stability of the preirradiated formulation is a necessity. Thermal stability of the formulations containing photoinitiators, at temperatures up to 180°C, is preferable. However, thermal stability at temperatures as low as 85°C is adequate under normal storage conditions. The photoinitiator or photoinitiator system is usually present in the range of 0.1–10% by weight based on the total weight of the dry photopolymerizable layer. Examples of photoinitiators and photosensitizers that have the desired thermal stability characteristics include substituted 9,10-anthraquinones as listed in Table 7.1.

Other photoinitiators that are also useful, although some may be thermally active at temperatures as low as 85°C, are the vicinal ketaldonyl alcohols such as benzoin, pivaloin, and acyloin ethers. Examples of these include benzoin methyl and ethyl ethers, and α-hydrocarbon-substituted aromatic acyloins, including α-methylbenzoin, α-allyl-benzoin, and α-phenylbenzoin.

TABLE 7.1

Anthraquinone Photoinitiators and Photosensitizers

2-*tert*-Butylanthraquinone	Octamethylanthraquinone
2,3-Naphthacene-5,12-dione	2-Methyl-1,4-naphthoquinone
2,3-Dimethylanthraquinone	2-Phenylanthraquinone
2,3-Diphenylanthrquinone	7,8,9,10-Tetrahydronaphthacene-5,12-dione
Retenequinone	1,2,3,4-Tetrahydrobenz[*a*]anthracene-7,12-dione

Photoreducible dyes and reducing agents are also suitable photoinitiators. Examples include the dyes of the phenazine, oxazine, and quinone classes, Michler's ketone, benzophenone, and 2,4,5-triphenylimidazolyl dimers with hydrogen donors, including leuco dyes and their mixtures. Sensitizers may also be used with many of these photoinitiators [10].

7.5.4 Aqueous Binder: Acid Polymer

The use of an acidic organic polymer is the crucial element for the aqueous developable formulation. The aqueous soluble binder polymer, which facilitates aqueous processability and results in high resolution, generally contains a copolymer or interpolymer of a C_1-C_{10} alkyl acrylate, C_1-C_{10} methacrylate, or a substituted or unsubstituted styrene, and an ethylenically unsaturated carboxylic acid containing moiety that is at least 15 wt% of the total polymer weight. An example of an effective substituted styrene is α-methylstyrene. Suitable copolymerizable carboxylic acids include ethylenically unsaturated monocarboxylic acids such as acrylic, methacrylic, and crotonic acids and ethylenically unsaturated dicarboxylic acids such as fumaric, itaconic, citraconic, vinyl succinic, and maleic acids, as well as their half-esters, and where appropriate, their anhydrides, and mixtures of these materials. As discussed earlier, methacrylic polymers are generally more desirable than acrylic polymers because they are cleaner burning. With the previously described limits for the nonacidic comonomers, it is generally optimal that the alkylacrylate or methacrylate constitutes at least 50–85 wt% of the polymer.

Other polymers and copolymers may be used at levels as high as 50 wt% of the organic polymer. It is critical that the total organic unpolymerized photomonomer and polymer or copolymer binder be soluble in the development solution. Acrylate or methacrylate acid containing binders are desirable because of their ease of solubility in basic aqueous development solution and their low cost. The acid-containing acrylate or methacrylate polymers can be prepared by conventional solution polymerization techniques. This is generally accomplished by combining an α-, β-ethylenically unsaturated acid with one or more copolymerizable vinyl monomers in a relatively low boiling (75–150°C) organic solvent to obtain a 10–60% solution of the monomer mixture. A polymerization catalyst is added and heat applied resulting in polymerization. After the polymerization reaction is essentially complete,

the resulting acid polymer solution is cooled to room temperature, and samples are removed to determine the viscosity, molecular weight, acid equivalent, etc., of the polymer. The polymer may then be isolated by precipitation or solvent evaporation.

As discussed earlier, the presence of the acidic monomer component of the polymer is critical to this technology. The acid functionality ensures developability in aqueous base such as a 1% solution of sodium carbonate. Concentrations of acid below 15% are difficult to wash out in aqueous base, and concentrations above 30% generally are unstable under humid conditions and partially develop in the imaged areas. The hydrophilicity of the polymer may also be increased by the use of monomers containing alcohol (-OH) functionality [14]. Generally, it is desirable to keep the molecular weight of the acid-containing binder-polymer less than 50,000 average molecular weight, as high-molecular-weight polymers develop slowly or incompletely in the basic development solutions.

Although there are limits to the range of acid level and molecular weight of the binder, there is room for considerable variation of these two parameters within a binder molecule while still achieving acceptable developability. The glass transition temperature of the binder polymer should be ≥100°C, as the paste is dried at temperatures up to 100°C. A glass transition temperature below 100°C generally results in a very tacky composition.

7.5.5 Photocurable Element

The photocurable element of the formulation is composed of at least one addition polymerizable monomer or oligomer. Generally, these materials contain ethylenically polymerizable functionalities, such as acrylate or methacrylate moieties that are capable of forming high polymers by a free radical-initiated, chain-propagating addition polymerization. Epoxy and vinyl ether monomers, initiated by photogeneration of acid catalysts, are applicable [15] where acrylates are unacceptable because of cost, physical properties, or environmental reasons. However, the acrylates are generally most effective (Figure 7.10). Preferred monomeric compounds are nongaseous, that is, they have a normal boiling point above 150°C. Clearly, a monomer with a high boiling point and low vapor pressure is required for shelf life, compositional consistency of the formulation, and environmental reasons.

It is also desirable that the monomer acts as a plasticizer for the polymeric binder. A critical necessity of the polymerized monomer, as with the remaining unpolymerized monomer, is that they readily decompose to gaseous products when the cured formulation is fired during the sintering step. Otherwise, the partially degraded polymer will cause the formation of blisters in the sintered material, resulting in poor hermeticity and other defects. Suitable monomers that can be used alone, or in combination with other monomers, include acrylates and methacrylates as shown in Table 7.2 [10].

$$CH_2 - O\overset{\overset{\displaystyle O}{\|}}{C} - CH=CH_2$$

$$CH_3CH_3C - CH_2 - O - \overset{\overset{\displaystyle O}{\|}}{C} - CH=CH_2$$

$$C - CH_2 - O\overset{\overset{\displaystyle O}{\|}}{C} - CH=CH_2$$

TMPTA

$$C_6H_5 - O - \overset{\overset{\displaystyle O}{\|}}{C} - C=CH_2$$
$$CH_6CH_3$$

PEA

$$CH_2=C - \overset{\overset{CH_3}{\overset{\displaystyle |}{}}}{\underset{\underset{\displaystyle O}{\|}}{C}} - O - (CH_2 - CH_2 - O)_4 - \overset{\overset{CH_3}{\overset{\displaystyle |}{}}}{\underset{\underset{\displaystyle O}{\|}}{C}} - C=CH_2$$

TEDMA
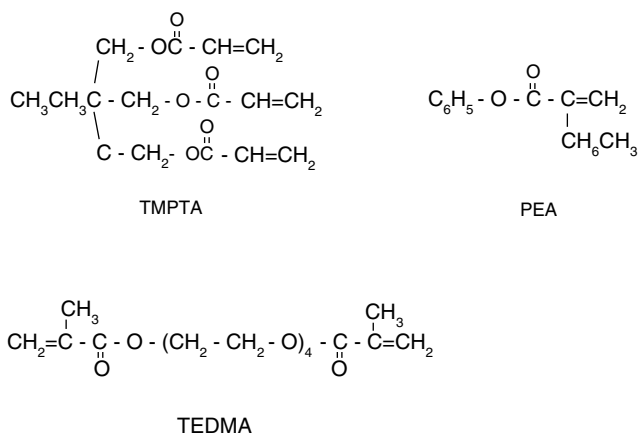
FIGURE 7.10
Widely used acrylic monomers.

Ethylenically unsaturated compounds having a molecular weight of at least 300, for example, alkylene or a polyalkylene glycol diacrylate prepared from an alkylene glycol of 2–15 carbons, or a polyalkylene ether glycol of 1–10 ether linkages, and those having a plurality of additional polymerizable ethylenic linkages, particularly when present as terminal linkages, are also useful. Monomers such as polyoxyethylated trimethylolpropane triacrylate, ethylated pentaerythritol triacrylate, dipentaerythritol monohydroxypentaacrylate, and 1,10-decanediol dimethylacrylate are particularly effective. The unsaturated monomeric component is present in an amount of 5–45 wt% based on the total weight of the dry photopolymerizable layer.

The functionality of the photocurable element and the acid-containing polymer binder can be combined into a photocurable or reactive binder polymer or oligomer, and is widely reported in the patent literature [16–18]. Generally, these reactive binder polymers or oligomers are formed by the addition reaction of a glycidyl-containing, ethylenically unsaturated compound or a chloride acrylate with the carboxyl groups on a preformed acrylic polymer binder. An overall acid number for the reactive polymer or oligomer of 80–140 is still desirable for adequate solubility in aqueous development solution. Therefore, the glycidyl-containing ethylenically unsaturated molecule or a chloride acrylate is reacted with the 0.05–0.8 mole equivalents of the carboxyl groups in the preformed acrylic polymer. Although the photocurable binder polymer or oligomer could be used with no additional photocurable monomer, the majority of reported examples include both the photocurable polymer and some additional photocurable monomer. The major benefit of the reactive polymer cited in the published examples is an improvement in the development latitude — an ability to withstand extended development times or harsh development solutions — of the formulations.

TABLE 7.2

Photocurable Monomers

1,5-Pentanediol diacrylate and dimethacrylate	Decamethylene glycol diacrylate and dimethacrylate
N,N-Diethylaminoethyl acrylate and methacrylates	Glycerol diacrylate and dimethacrylate
Ethylene glycol diacrylate and dimethacrylate	Glycerol triacrylate and trimethacrylate
1,4-Butanediol diacrylate and dimethacrylate	Polyoxyethylated triethylolpropane triacrylate
Diethylene glycol diacrylate and dimethacrylate	Pentaerythritol triacrylate and trimethacrylate
1,3-Propanediol diacrylate and dimethacrylate	Tripropylene glycol diacrylate and dimethacrylate
1,4-Cyclohexanediol diacrylate and dimethacrylate	Trimethylolpropane triacrylate and trimethacrylate
t-Butyl acrylate and methacrylates	2,2-Dimethylolpropane diacrylate and dimethacrylate
Triethylene glycol diacrylate	2,2-Di-(*p*-hydroxyphenyl)-propane dimethacrylate
Triethylene glycol dimethacrylate	Di-(2-methacryloxyethyl) ether of bisphenol-a
Diallyl fumarate	Di-(2-acryloxyethyl) ether of bisphenol-a
1,4-Benzenediol dimethacrylate	1-Phenyl ethylene-1,2-dimethacrylate
1,4-Diisopropenyl benzene	Polyoxypropyltrimethylol propane triacrylate
1,3,5-Triisopropenyl benzene	Butylenes glycol diacrylate and dimethacrylate
Styrene	1,2,4-Butanetriol triacrylate and trimethacrylate
Di-(3-methacryloxy-2-hydroxypropyl) ether of bisphenol-A	
Di-(3-acryloxy-2-hydroxypropyl) ether of bisphenol-A	
Di-(3-methacryloxy-2-hydroxypropyl) ether of 1,4-butnediol	
2,2,4-Trimethyl-1,3-pentanediol diacrylate and dimethacrylate	
2,2-Di(*p*-hydroxyphenyl)-propane diacrylate and tetramethacrylate	
Polyoxyethylated trimethylolpropane triacrylate and trimethacrylate	

7.5.6   Organic Medium

The organic medium serves as a vehicle for dispersion of the finely divided solids in such form that the composition can readily be applied to a ceramic or other substrate base. Thus, the organic medium must primarily be one in which the solids are dispersible with an adequate degree of wettability and the organic materials are soluble. Secondly, the rheological paste properties must be such that they lend good application properties to the dispersion.

When the dispersion is to be made into a film, the organic medium (in which the ceramic solids and inorganic binder are dispersed) consists of the polymeric binder, monomer, and initiator (which are dissolved in a volatile

organic solvent) and, optimally, other dissolved materials such as plasticizers, release agents, dispersing agents, stripping agents, antifouling agents, and wetting agents.

The solvent component of the organic medium, which may be a mixture of solvents, is chosen so as to obtain complete solubilization of the polymer and other organic constituents. The solvent should also be of sufficiently high volatility to enable it to evaporate with the application of relatively low levels of heat at atmospheric pressure. In addition, the solvent must boil well below the boiling point and decomposition temperatures of any other materials contained in the organic medium. As discussed earlier, the boiling point or, more precisely, the temperature used to remove the organic medium must be below the decomposition temperature of the photosensitizer. Thus, solvents having atmospheric boiling points below 150°C are used most frequently. Such solvents include acetone, methanol, ethanol, methylethyl ketone, ethyl acetate, amyl acetate, 2,2,4-triethyl pentanediol-1,3-monoisobutyrate, toluene, and ethylene glycol monoalkyl and dialkyl ethers such as ethylene glycol mono-*n*-propyl ether, and α- and β-terpenes.

The organic medium may also contain plasticizers that act to lower the glass transition temperature of the binder polymer. Such plasticizers help to assure good lamination to ceramic substrates and enhance the developability of unexposed areas of the composition. The use of such materials should be minimized to reduce the amount of organic materials, which must be removed when the composition is fired. The choice of plasticizers is, of course, determined primarily by the polymer that must be modified. Among the plasticizers that have been used in various binder systems are diethyl phthalate, dibutyl phthalate, alkyl phosphates, polyalkylene glycols, hydroxy ethylated alkyl phenol, triethyleneglycol diacetate, and polyester plasticizers. Dibutyl phthalate is frequently used in acrylic polymer systems because it can be used effectively in relatively small concentrations.

It has been found [19] that the weight ratio of the inorganic ceramic and glass frit to organics is within the range of 2.6–4.5. A ratio of no more than 6.0 is necessary to obtain adequate dispersion and rheological properties. With a ratio below 2.5, the amount of organics that must be burned off is excessive, and the quality of the final layers suffers. The ratio of inorganic solids to organics is dependent on the particle size of the ceramic and frit, the organic components, and the surface pretreatment of the inorganic solids. It is desirable to use a lower level of organics to minimize firing defects. When the particles are treated with organosilane coupling agents, the ratio of inorganic solids to organics can be increased. Organosilanes suitable for this technology are those corresponding to the general formula $RSi(OR')_3$, in which R′ is methyl or ethyl, and R is selected from alkyl, methacryloxypropyl, polyalkylene oxide, or other organic functional groups that interact with the organic matrix of the film. When the dispersion is to be applied as a thick-film paste, conventional thick-film organic media are used with appropriate rheological adjustments and the use of lower-volatility solvents.

As discussed in earlier text, the paste is formulated to have near-Newtonian rheology to allow it to level after passing through the screen. This is important for the usefulness of this technology, as the leveled paste shows no marks from the screen printing, but is smooth and level. The final circuit pattern is created by photo imaging and development. Although the rheological properties are of primary importance, the organic medium is formulated to give appropriate wettability of the solids and the substrate, good drying rate to remove the organic solvent, sufficient dried-film strength for handling, and good firing properties. In view of all these criteria, a wide variety of liquid materials can be used in the organic media. The organic medium for thick-film compositions is typically a solution of resin or polymer in an appropriate solvent. The solvents usually boil within the range of 120–175°C and are removed during drying of the coated paste at temperatures below 100°C to avoid decomposition of the photosensitizer. The most widely used solvents for thick-film applications are terpenes such as α- or β-terpinol, which yield excellent wetting behavior and display the desired rheology.

The ratio of organic medium to inorganic solids in the dispersions varies considerably depending on the manner in which the dispersion is to be applied and the organic medium used. Normally, to achieve good coverage, the dispersions will contain 50–90% by weight solids and 10–50% organic medium. Such dispersions are usually of semifluid consistency and are referred to commonly as "pastes."

The viscosity of the pastes is typically within the range of 25–200 Pa-sec. The amount and type of organic medium used is determined mainly by the final desired formulation viscosity and print thickness.

7.5.7 Dispersant

A dispersant ensures thorough wetting of the inorganics by the organic polymers and monomers and is a critical component of the formulation. A well-dispersed inorganic is necessary for the preparation of photocurable pastes with the required properties for efficient screen printing, leveling, imaging, and burn-out characteristics. The dispersant allows the polymeric binder to wet the freeze-dried inorganic solids, giving an agglomerate-free formulation. The dispersants of choice are the A-B dispersants as described by Jakubauskas [20] and Ashe [21].

7.5.8 Additional Components

Small amounts of additional components may be used in the photopolymerizable compositions. Dyes, thermal polymerization inhibitors, pigments, adhesion promoters, such as organosilane coupling agents, and plasticizers are often employed. Coating aids, such as polyethylene oxides may also be

TABLE 7.3

Composition of Dielectric Paste

Inorganics	
Glass frit	Lead borosilicate glass of a particle size range d50 of 2.3–2.7 μm
Alumina	Aluminum oxide (Al_2O_3); particle size d50 of 2.4–2.6 μm, surface area of 3.5–4.5 m^2g
Pigment	Cobalt aluminate ($CoAl_2O_4$)
Polymeric Binders	
Binder	Copolymer of 75% methylmethacrylate and 25% methacrylic acid, Mw 7000, Tg 120°C, Acid No. 164
Monomers	
Monomer I	Polyoxyethylated tri-methylolpropane triacrylate
Monomer II	Monohydroxy polycaprollactone monoacrylate, Mw 458
Solvents	β-Terpineol (1-methyl-1-(4-methyl-4-hydroxycyclohexyl)ethane
Initiators	
BP/MK	Benzophenone/Michler's ketone
Stabilizer	
Antioxidant	2,6-Di-*tert*-butyl-4-methylphenol
Dispersant	A-B dispersant

employed. It is important that these materials do not degrade the patterning, exposure, and aqueous development characteristics of the formulation.

The ceramic, glass frit, organic monomer, polymeric binder, photoinitiator, and dispersant in Table 7.3 [10] are among those discussed earlier. Such a formulation was used to prepare dielectric vias as shown in Figure 7.11.

7.5.9 Preparation of Organic Vehicle

The vehicle is formulated under yellow light conditions to prevent exposure to UV light, which could cause polymerization during paste preparation. The solvent, polymeric binder(s), dispersant, and other nonphotoinitiator organic compounds are mixed and heated (to 100°C), with stirring, until all organic components are completely dissolved. The solution is cooled to 80°C, and the initiator and stabilizer added and the mixture stirred until the solids have dissolved. The 80°C stirring temperature during photoinitiator addition vs. the 100°C temperature during polymer addition prevents thermal decomposition of the photoinitiators. After the organic solids have dissolved, the solution is filtered.

7.5.10 Preparation of Dielectric Inorganics [19]

7.5.10.1 *Glass*

The glass frit is milled to a d50 of 2.3–2.7 μm by slurry milling in water with alumina-milling media. The mixture of frit, water, and milling media is screened to remove milling media and large particles and passed through a

DEVELOPMENT   **Dissolution and removal of paste**
                    components in the unexposed areas.
                    1) Neutralize surface --COOH groups
                    $$R\text{-COOH} + Na_2CO_3 \rightarrow R\text{-COO}{\oplus}Na{\oplus} + NaHCO_3$$
                    2) Hydrate ionic materials, swelling with H_2O
                    3) Dissolve or physically remove swollen material

COONa
COOH
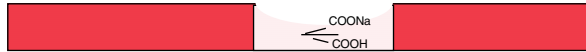
Exposed areas resist swelling and removal
of material because of encapsulation by the
crosslinked polymer network.

FIGURE 7.11
Development. (Figure courtesy of DuPont and Co.)

magnetic separator to remove conductive impurities. The water–glass slurry is freeze-dried to prevent agglomeration of the inorganics.

There are many glass frits that are applicable to this technology. It is important that the frit sinters between 475 and 750°C without decomposition and can be easily milled to the particular size and distribution.

7.5.10.2 Ceramic

The alumina is milled to achieve a d50 of 2.3–2.7 μm. As with the glass frit, the slurry is screened and passed through a magnetic separator to remove conductive impurities. The filler is freeze-dried in the same manner as the frit. The colorant may be processed with the frit, the filler, or in a stand-alone mode.

7.5.11 Paste Formulation

The paste examples in Table 7.4 and Table 7.5 are prepared by combining the organic vehicle, monomer, and dispersant in a mixing vessel. The frit and alumina/cobalt aluminate mixture is then added and the entire composition is mixed. After aging for 12–24 h to allow thorough wetting of the inorganic by the organic vehicles, the mixture is roll-milled using a three-roll

TABLE 7.4

Dielectric Formulation 1

Component	Parts
Alumina/cobalt aluminate	20–40
Glass frit	20–40
Binder	30–50
Solvent	
β-Terpineol	35–60
Initiator	
TBAQ	3–8
Antioxidant	
Ionol®	0.1–0.5
Monomer	
TEOTA	5–15
Dispersant	
A-B dispersant	1–3
Results	
Resolution	3-mil (75-μm) vias
Photo speed	50–90 mJ/cm²
Development	1% Aqueous sodium carbonate

TABLE 7.5

Dielectric Formulation 2

Component	Parts
Alumina/cobalt aluminate	20–40
Glass frit	20–40
Binder	30–50
Solvent	
β-Terpineol	35–60
Initiator	
Benzophenone	2–8
Michler's ketone	4–12
Antioxidant	
Ionol®	0.1–1.0
Monomer	
TEOTA	5–20
Results	
Resolution	2-mil (50-μm) vias
Photo speed	50–90 mJ/cm²
Development	1% Aqueous sodium carbonate

mill. After milling, the paste is screened. The paste viscosity is adjusted by the addition of solvent to 80–120 Pa-sec. The paste formulation is best performed in a class 100 clean room to prevent contamination.
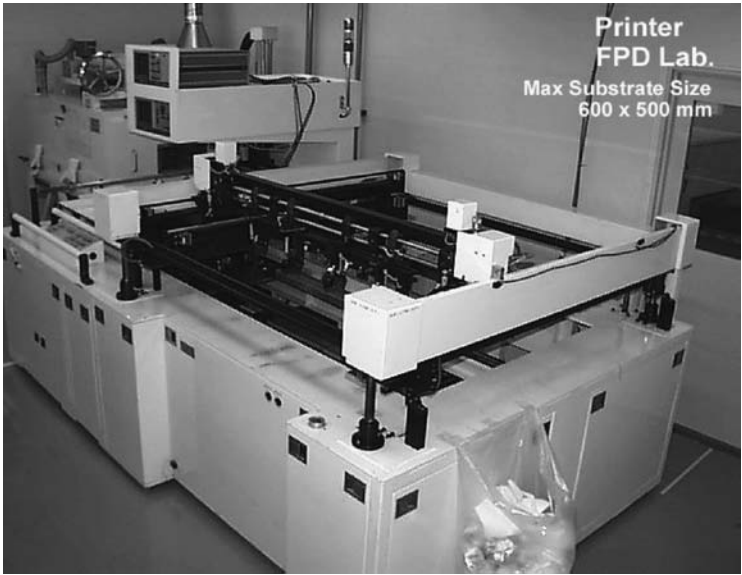
FIGURE 7.12
Processing equipment — printer. (Photograph courtesy of DuPont and Co.)

7.5.12   Processing

The photosensitive ceramic-coating formulation is applied to a substrate by screen printing, as shown in Figure 7.12. Typical process parameters are also given in Table 7.6. In some cases, doctor-knife application may be acceptable. Following a short leveling period, the screen-printed substrate is dried in a forced-air oven to remove the organic solvent. The result is a dry, smooth coating that is nontacky and easily handled.

TABLE 7.6

Processing Conditions

Printing	200-Mesh stainless steel screen
	Single wet pass at 1–2 in./sec
Leveling	5–10 min at room temperature
Drying	20–30 min at 80°C
Exposure	18–35 mJ/cm^2
	(1.5–3.0 sec with 1-kW lamp)
Development	2.0 × TTC[a] with 0.8–1.0% Na_2CO_3 at 30°C
Firing	60-min profile
	10 min at 850°C peak

[a]   TTC is the time to clear.

FIGURE 7.13
Processing equipment — exposure. (Photograph courtesy of DuPont and Co.)

The parts are exposed by UV light, through a photomask in contact with the coating. UV radiation sources with mercury or mercury–xenon collimated light are preferred, using equipment such as that shown in Figure 7.13. The optimum exposure energy is determined from an exposure-time series that yields the correct size vias or photoformed holes in the dielectric after development (Table 7.6).

The exposed parts may be developed using a standard spray developer containing aqueous sodium carbonate as the development solution, as illustrated in Figure 7.14. The temperature of the developer may be varied from 25 to 45°C.

The developed parts are dried and then fired in a furnace, as shown in Figure 7.15. The furnace profile usually consists of a firing segment at temperatures between 300 and 450°C to burn off the organic materials, followed by firing between 800 and 900°C over approximately a 2-h cycle to sinter the alumina–frit mixture (Table 7.7) (Figure 7.16). This processing sequence yields dielectric vias as small as 3 mil, or 75 μm (Figure 7.17).

An example of product properties for the fired dielectric is taken from U.S. Patent 4925771 (Table 7.8) [19]. This product yields dielectric via diameters of 2–3 mil, after coating, drying, exposing, and firing.

A majority of commercial applications of aqueous developable ceramic compositions use acid-containing polymer binders and dilute aqueous base as a development solution. However, a totally aqueous development system can be formulated with the use of water-soluble polymer binders [22]. Ogawa proposes the use of nonionic water-soluble polymers, such as the cellulose ethers: methyl cellulose, hydroxy methyl cellulose, hydroxy ethyl cellulose, and hydroxy propyl cellulose, as the polymeric binder. Molecular weights in the range of 30,000 to 1,000,000 are preferred in these compositions. When
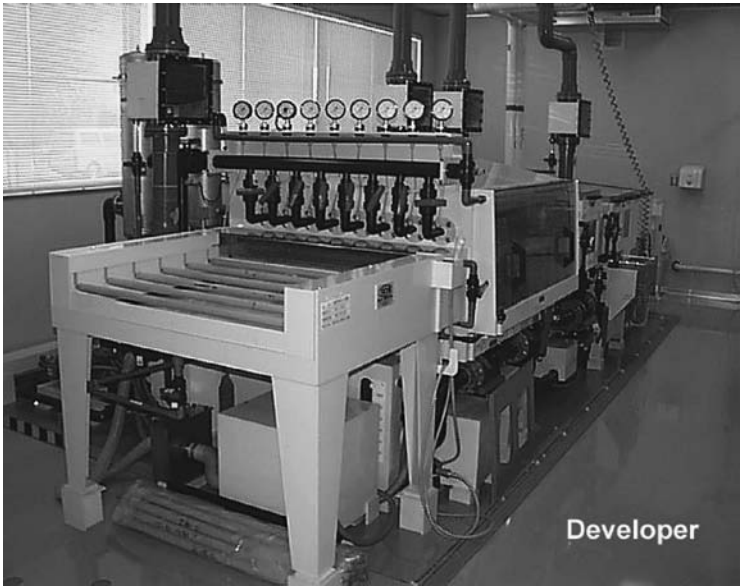
FIGURE 7.14
Processing equipment — developer. (Photograph courtesy of DuPont and Co.)

FIGURE 7.15
Processing equipment — belt furnace. (Photograph courtesy of DuPont and Co.)

TABLE 7.7

Processing Sequence to Obtain 40–45
μm Fired Thickness

Print/dry/print/dry/expose/develop/fire
Optional via fill/dry/fire
Print/dry/print/dry/expose/develop/fire
Via fill/dry/fire
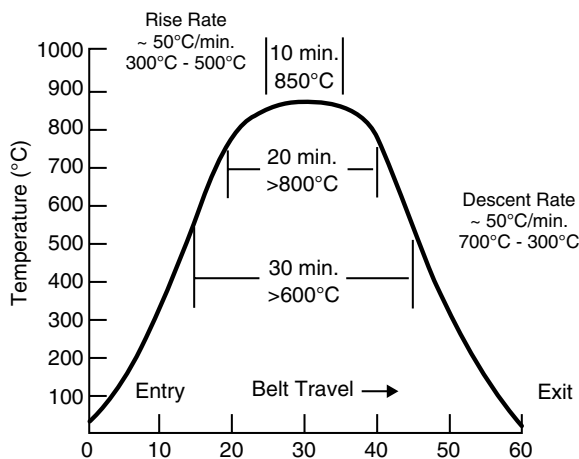
FIGURE 7.16
Recommended firing profile. (Figure courtesy of DuPont and Co.)

these polymers are combined with the monomers, photoinitiators, and inorganic materials commonly used in formulations designed for development in dilute aqueous base solutions, a completely water-developable formulation can be achieved.

7.6 Photocurable Conductive Pastes: Background

The following discussion is directed to the preparation of photoformed 2-to 3-mil metal conductor circuits. The previous analysis, regarding the use of screen-printed dielectrics to prepare circuits, was presented in detail and also applies to the preparation of conductive circuitry. The need for increased circuit density clearly applies to gold, copper, silver, and other conductors. The screen-printed pastes contain conductive metals and glass frits vs. the dielectric paste, which generally contains a dielectric and a glass frit.

Standard thick-film conductor pastes are very important in the electronics industry. However, when applying these materials in patterns by screen
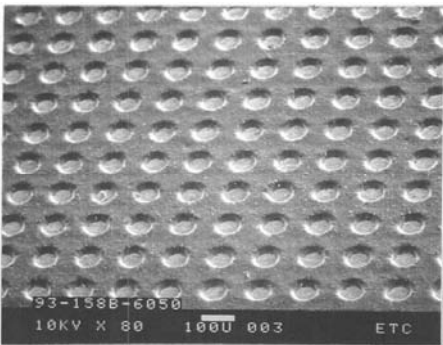
3 mil Vias, 80 X
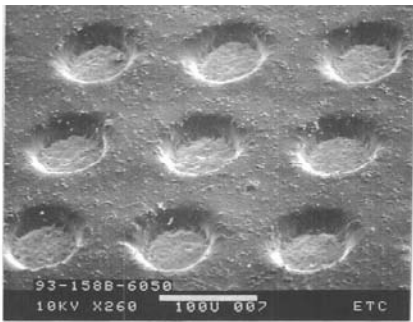
3 mil Vias, 260 X

FIGURE 7.17
Enlarged via images. (Photograph courtesy of DuPont and Co.)

TABLE 7.8

Dielectric Performance Properties

Viscosity	50–100 Pa-sec
	HBTD, #14, 10 r/min, 25°C[a]
Via resolution	3 mil @ 45 μm thick
Fired thickness	40–45 μm
Breakdown voltage	1600–2900 VDC/mil
Insulation resistance	2.7–2.5 × 10^{11} Ω
Dielectric constant	7.0–8.3
Dissipation factor	0.4–0.5%

[a] Viscosity meter configuration used for the measurement.

Source: From Yoshimura, A. et al., Japanese Patent Application 05-287221, November 2, 1993. With permission.

printing, it is difficult to obtain the necessary fine-line and space resolution. It is essential that all the screen-printing variables such as screen quality, squeegee hardness, print speed, dispersion properties, etc., be carefully controlled and constantly monitored to obtain good product yields. Photolithography provides a new approach for increased resolution with conductive thick-film materials. Photosensitive, conductive thick-film pastes are applied to a substrate, dried, exposed to actinic ultraviolet radiation, and then developed by aqueous solution to remove unexposed portions of the material. The developed part is then fired to remove the organics and to sinter the conductive particles, forming an electrically conductive circuit trace.

The theory and practice of the photocurable-conductor formulation (monomer, organic and inorganic binders, photoinitiator) and the processing procedure are generally similar to the formulation and processing of the dielectric materials discussed previously. These aspects will not be discussed at length in this section. However, because the conductor paste contains metal particles, differences between the dielectric and conductive materials will be explained in some detail [23].

7.6.1 Conductor Paste Formulation

The metal powder, which, in the conductive paste, is used in place of the alumina in the dielectric paste, is a finely divided metal having a surface area-to-weight ratio of less than 20 m^2/g with more than 80 wt% of the particles having a size of 0.5–10 μm. Various forms or shapes of metal powder, including spherical particles, flakes, rods, cones, and plates are employable. Spherical metal particles are most efficient with sizes of greater than 2 μm. Pastes with particle sizes larger than 20 μm are difficult to adequately coat by screen printing and can result in poor surface smoothness in the coated film. Best results are obtained when 80 wt% of the metal powder falls in the range of 0.5–10 μm. This particle size range minimizes blistering during burnout (sintering) of the paste and facilitates coating.

Other metal powders, such as palladium and platinum may be added to conductor compositions to improve the properties of the conductor. The palladium powder, in the form of spherical-shaped particles of 0.1–10 μm in diameter is desired.

Copper oxide can improve adhesion of the fired metal conductor to ceramic substrates. Copper oxide with particle sizes of 0.5–5 μm is generally optimum. Copper oxide concentrations between 0.1 and 3% by weight of the total composition provide the desired adhesion. Although the copper oxide may be necessary for adhesion, an adverse effect of this material is chelation with the organic binder. The copper oxide can form a chelate with the organic acid-containing binder, causing a paste viscosity increase, resulting in poor shelf life. The addition of 0.2–0.5% benzotriazole may prevent this reaction [24].

TABLE 7.9

Gold Formulation 1

Component	Parts
Gold powder (spherical gold, particle size 1.7–2.7 µm)	70–90
Palladium (surface area 6.1–9.6 m²/g)	0.1–1.0
Cuprous oxide (surface area 1.3–3.2 m²/g)	0.2–1.5
Glass frit	1.0–3.0
Organic binder	6.0–15.0
Solvent	
Carbitol acetate	5.0–12.0
Initiator	
Benzophone	0.4–1.5
Initiator/sensitizer	
Michler's ketone	0.1–1.0
Antioxidant	
Ionol	0.1–1.0
Stabilizer	0.3–3.0
Monomer	
TEOTA	1.0–10.0
(polyoxyethylated trimethylolpropane triacrylate, Mw 1162)	
TMPTA (triethylolpropane triacrylate)	1.0–10.0
Results	
Resolution	1 mil
Photo speed	960 mJ/cm²

The glass frit has a glass transition temperature from 475 to 825°C, a surface area-to-weight ratio of less than 10 m²/g and 90 wt% of the particles have a size of 1–10 µm. The weight ratio of glass frit to gold may be in a range of 0.0001 to 0.25 and is dispersed in the organic medium. The organic medium is similar to that used with the dielectrics, as shown in Table 7.9 to Table 7.11.

At this point the reader may be curious about the mechanism by which UV radiation is able to photocure a composition containing metal particles. Clearly the metal particles are opaque to UV radiation wavelengths. This subject is of considerable practical interest, as metal-containing pastes, and indeed, other photoactive pastes containing opaque materials can be hardened when exposed to UV radiation.

A detailed examination of this area of interest is beyond the scope of this text. Briefly however, the current view of this phenomenon is that during the polymerization step, areas exposed to UV light are rendered insoluble by two processes. First, the metal-containing paste is not completely opaque as the metal volume is 40–60%. The interstices between the particles can provide an avenue for light penetration of the coating. Particle size and shape is a major factor for interstice formation. Clearly, spherical particles will allow more penetration of light through the coating than large platelet-shaped particles, based upon the packing density and particle overlap. Careful examination of the patent literature will demonstrate that most photocurable, metal particle-containing conductor compositions do contain

TABLE 7.10

Gold Formulation 2

Component	Parts
Gold powder (spherical gold, particle size 1.7–2.7 μm)	70–90
Palladium (surface area 6.1–9.6 m²/g)	0.1–1.0
Cuprous oxide (surface area 1.3–3.2 m²/g)	0.2–1.5
Glass frit	1.0–3.0
Organic binder	6.0–15.0
Solvent	
Carbitol acetate	5.0–12.0
Initiator	
Benzophone	0.4–1.5
Initiator/sensitizer	
Michler's ketone	0.1–1.0
Antioxidant	
Ionol	0.1–1.0
Stabilizer	0.3–3.0
Monomer	
TEOTA	1.0–10.0
(polyoxyethylated trimethylolpropane triacrylate, Mw 1162)	
TMPTA (triethylolpropane triacrylate)	1.0–10.0
Results	
Resolution	1 mil
Photo speed	960 mJ/cm²

TABLE 7.11

Gold Formulation 3

Component	Parts
Gold powder (spherical gold, particle size 1.7–2.7 μm)	70–90
Palladium	0.1–1.0
Cuprous oxide	0.2–1.5
Glass frit I	0.5–4.0
Glass frit II	0.2–2.0
Organic binder	6.0–15.0
Solvent	
Carbitol acetate	5.0–12.0
Initiator	
Benzophone	0.4–1.5
Initiator/sensitizer	
Michler's ketone	0.1–1.0
Antioxidant	
Ionol	0.1–1.0
Stabilizer	0.3–3.0
Monomer	
TEOTA	1.0–10.0
(polyoxyethylated trimethylolpropane triacrylate, Mw 1162)	
TMPTA (triethylolpropane triacrylate)	1.0–10.0
Results	
Resolution	1 mil
Photo speed	900 mJ/cm²

spherical or nearly spherical metallic particles. In addition to direct-light penetration, metal particles can scatter light of all wavelengths. The amount of light scattering from a metal particle is dependent upon the size, shape, and reflectivity of the particle. There is sufficient light penetration in the conductive paste to cause polymerization, although the light penetration is not as effective as with a material containing no opaque particles.

In the second process, the unpolymerized monomer can migrate or diffuse to areas where polymerization is occurring or has occurred during polymerization. The migrating monomer can, in turn, polymerize. In many cases, the monomer acts as a plasticizer for the organic binder. As the monomer migrates from an area of high concentration (an unpolymerized area), to an area of lower concentration (a polymerized area), its ability to plasticize the binder is reduced. The nonplasticized organic binder is generally less soluble in the development solution, when compared to the fully plasticized material. This results in insolubilization of the metal-containing paste in areas very near the exposed regions of the composition, even though light has not penetrated this region. This effect appears to only occur on the microscale in which metal particle sizes of 1.7–5.0 μm are present. Because the image can be developed to a resolution of <2-mil line widths, it is clear that, if the above theory is correct, the monomer in the exposed regions only migrates short distances; otherwise there would be insolubility in broader nonexposed regions, causing poor image resolution. Monomer migration or diffusion into the polymerized area has been thoroughly documented in the case of organic solvent developable compositions. Evidence for this mechanism is not so clear for compositions designed for development in basic aqueous solutions.

7.6.2   Gold Paste Preparation

The vehicle and conductive paste are prepared by the same procedures used to prepare the dielectric-paste materials. The paste is applied by screen printing to a substrate, leveling, drying, exposing to UV light, and developing in basic aqueous solution. The paste is then fired to sinter the metal particles, forming a conductive circuit pattern (Figure 7.18).

7.6.3   Process

Figure 7.19 and Figure 7.20 show line resolution vs. drying temperature and time for a processed gold conductor paste example. These figures not only illustrate that drying conditions will affect the ultimate resolution and line acuity, but also indicate that line resolution of approximately 1 mil (25 μm) is achievable with this technology. Properties of the exposed and unexposed paste and the electrical properties of the fired paste are described in Table 7.12.
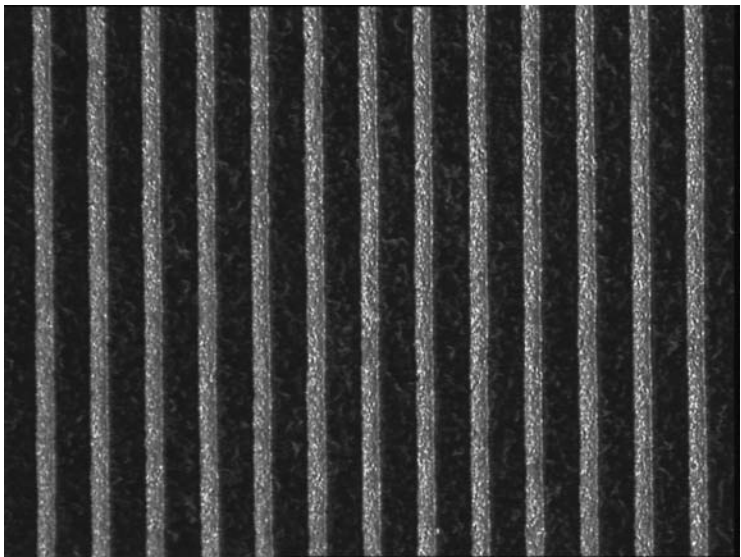
FIGURE 7.18
Forty-micron conductive lines and spaces. (Photograph courtesy of DuPont and Co.)

Oven Drying Study
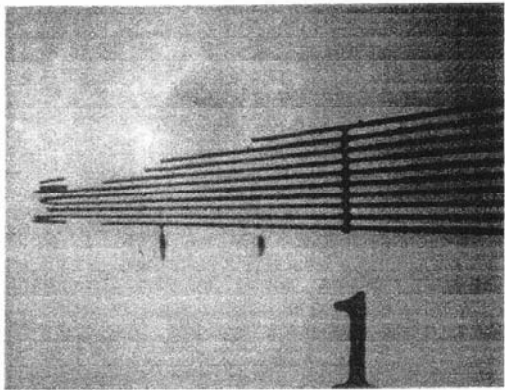
80°C, 20 minutes

FIGURE 7.19
Oven drying study — 20 min. (Photograph courtesy of DuPont and Co.)

In addition to the gold technology circuitry discussed in this section, other metals may be employed, such as copper [24] and silver [25]. As with the dielectrics, these are being extensively studied, and commercial products are being manufactured, e.g., DuPont Fodel®, with many variations remaining

Oven Drying Study
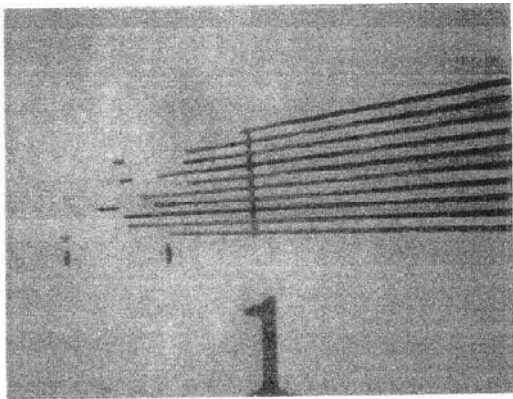
80°C, 30 minutes

FIGURE 7.20
Oven drying study — 30 minutes. (Photograph courtesy of DuPont and Co.)

TABLE 7.12

Au Conductor Performance

Viscosity	35–90 Pa-sec
	HBTD, #14, 10 r/min, 25°C[a]
Resolution	1.5-mil line
	2.0-mil space
Thickness	15–17 μm dry
	7–8 μm fired
Wire bonding	40-g 2-mil Au wire
	9.5-g 1-mil Au wire
	11.5-g 1-mil Al wire
	≥6.6-g 1-mil Al wire
	Aged 1 h, 300°C
Resistivity	≤6.6 mΩ/□

[a] Viscosity meter configuration used for the measurement.

Source: From Yoshimura, A. et al.., Japanese Patent Application 05-287221, November 2, 1993.

to be developed. Although the use of other metals in these photocurable compositions remains relatively unexplored, there is reason to expect that numerous elemental metals, alloys, metal salts, and other opaque materials will yield photocurable products.

The researcher should, however, remember that acrylate monomers and acid-containing binders will react with many metals causing polymerization

and/or cross-linking resulting in poor shelf life. Most acrylates will poly-merize in the presence of an alkaline environment and are therefore not acceptable because of poor shelf life. Additionally, acid-containing binder polymers will cross-link in the presence of some oxide levels of metals, again causing cross-linking and unacceptable shelf life.

Notwithstanding this and other hindrances, it is doubtless possible to generate numerous other photocurable electronic pastes. The discussion in this paper has been directed to the use of acrylate monomer and polymer binders. However, other monomers and nonacrylate binders may have excit-ing potential applications.

7.7   Other Applications of Photocurable Paste Technology

In addition to the use of this technology for the preparation of dielectric and conductive photoformable pastes, the technology is also applicable for the preparation of high-resolution resistor patterns. Of course, in the case of resistors, the appropriate concentration of dielectric and conductive materi-als are required to achieve the desired conductivity target.

The increase in resolution achieved through the use of photocurable pastes where line resolutions of 2–3 mil are obtained vs. the 4–8 mil from screen printing is not the highest-achievable resolution level. The possible methods of increasing resolution of future formulations will, of course, require smaller and more homogenous particle volumes and shapes for the inorganic mate-rials. Additionally, and probably more importantly, increased resolution and acuity will require optimization of the organic monomers and binders to yield a more distinct difference between the exposed and unexposed mate-rials — development latitude. It is possible that this may be achieved through proper choice of the molecular weight and acid number of the binder, as well as the comonomer ratios. The use of shorter-wavelength UV radiation is also known to yield higher resolution.

Although not included in this discussion, these compositions may be for-mulated to be developed in what is known as a semiaqueous solvent [26], where an organic solvent, such as butanol, at levels between 5 and 20%, is present in the aqueous developer. Formulations developed in this manner have been shown to have resolution equivalent to the all-aqueous developers with, in some instances, superior adhesion to the substrate.

A more recent application for formulations containing the aqueous devel-oped conductors is the production of displays such as plasma high-definition television panels. The line resolution and placement accuracy of the photo-curable pastes in this application can be used to generate more pixels per square unit of panel, resulting in improved picture quality.

Acknowledgments

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8

Copper Interconnects for Ceramic Substrates and Packages

Al Krum

CONTENTS

8.1   Introduction: Why Use Copper?

Copper metallization on ceramic substrates and packages is used because of two key physical parameters and one economic parameter: low electrical resistivity, high thermal conductivity, and low cost. In addition to these key parameters, copper has several characteristics that make it easy to use. These include excellent solderability, ease of applying electroplating finishes, good corrosion resistance, and readiness to form patterns through machining or chemical etching.

8.1.1   Electrical Resistivity

Of all the metals used for interconnections on electronic packages and substrates, copper has the second lowest electrical resistivity at 1.72×10^{-6} Ω·cm. Silver, with a resistivity of 1.59×10^{-6} Ω·cm [1], has the lowest resistivity but suffers from the potential problem of silver migration [2]. This low resistivity (or high conductivity) makes copper the second highest on a volume basis. For low-current applications where high interconnect density is required, this equates to a higher density of interconnections. Low electrical resistivity is a key parameter in determining efficiency and propagation delay. The electrical resistivity of a conductor also determines the amount of self-heating. Therefore, to minimize self-heating, the conductor's resistivity needs to be minimized.
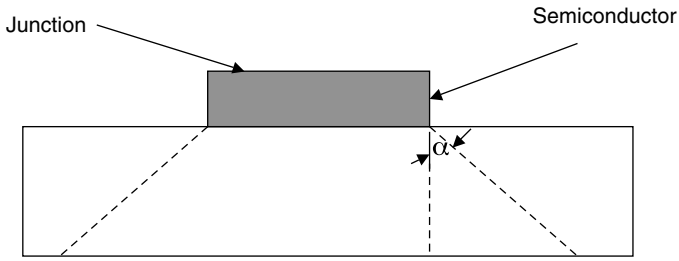
FIGURE 8.1
Spreading-angle definition. (From Krum, A., *Thermal Management Handbook*, Electronic Packaging and Interconnection Series, Eds., Krum, A. and Sergent, J., New York: McGraw-Hill, 1998. chap. 5. With permission.)

8.1.2 Thermal Conductivity

Because of the high thermal conductivity of copper (401 W/m·K), it is an excellent heat spreader. As defined in Chapter 3, the spreading angle (α) of two materials bonded together as shown in Figure 8.1 is

$$\alpha = \tan^{-1} \frac{K_1}{K_2} \tag{8.1}$$

where
    K_1 = thermal conductivity of the current layer
    K_2 = thermal conductivity of the underlying layer

Example
For a copper sheet direct-bonded to a 96% alumina substrate, the spreading angle is calculated as follows:

$$\alpha = \tan^{-1} \frac{K_1}{K_2} = \tan^{-1} \frac{401}{21} = 87°$$

As the maximum spreading angle in any configuration is 90°, the spreading angle in this example can be considered extremely high.

8.1.3 Cost

In many ceramic interconnect applications (both substrates and packages), the conductor contains the precious metal, gold, the cost of which is extremely high. For a recent 1-year period, the New York gold price [3] was in the range of $580 to $620/oz. The price of copper for the same period

ranged from \$3.36 to \$3.70/lb [4]. The ratio of the price of gold to copper (without adjusting the differences in density of the two metals) is 2900:1. It goes without saying that copper is the material of choice when it comes to minimum cost.

8.1.4 Disadvantages of Copper

Copper readily oxidizes in most atmospheres and is rarely used as the final finish. This oxidation prevents reliable soldering and wire bonding at the next assembly. To prevent the oxidation, copper metallization is typically plated with nickel and, optionally, with a gold top coat. In some applications, the copper is hot-dipped with a tin-based material such as solder.

The temperature coefficient of expansion (TCE) of elemental copper is 16.8 ppm/°C [1]. This is more than twice the expansion rate of ceramics used for substrates and packages. Without proper consideration of the differential expansions in copper and the ceramics, stresses and strains can be introduced into the materials and joints that may lead to fracturing.

The reader is directed to Subsection 3.5.1 of this book for a more detailed discussion of thermal stress caused by mismatches in thermal expansions.

8.2 Electrical Performance

8.2.1 Electrical Resistance

The resistance (R) in ohms of a conductor as shown in Figure 8.2 is calculated from the equation:

$$R = \frac{\rho_0 L}{A} \ (\Omega) \tag{8.2}$$

where
  ρ_0 = bulk resistivity of conductor
  L = conductor length
  A = cross-sectional area of conductor

The cross-sectional area of the conductor is calculated as

$$A = w \times t \tag{8.3}$$

where
  w = conductor width
  t = conductor thickness
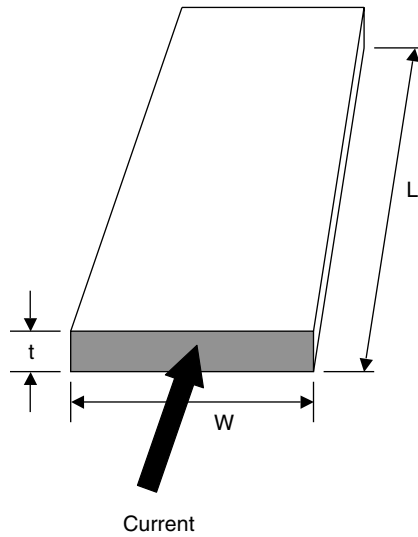
FIGURE 8.2
Resistance of a conductor. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

Substituting Equation 8.3 into Equation 8.2 produces an equation for resistance using physical parameters:

$$R = \frac{\rho_0 \, L}{w \, t} \, (\Omega). \tag{8.4}$$

The sheet resistivity ρ, a parameter found on data sheets for thick- and thin-film materials, is defined as the *normalized resistivity* and is expressed as ohms per square ($\Omega/\square$). (The term *square* $\square$ refers to a length divided by a width of the same units and is dimensionless.) Typically, the resistivity of thin- and thick-film materials is specified in ohms per square ($\Omega/\square$) or milliohms per square ($m\Omega/\square$).

$$\rho = \frac{\rho_0}{t} \tag{8.5}$$

where t = conductor thickness.
The resistance of the conductor can now be expressed as follows:

$$R = \frac{\rho L}{w} \, (\Omega). \tag{8.6}$$
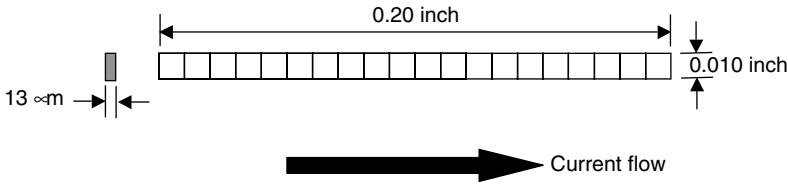
FIGURE 8.3
Thick-film copper conductor.

8.2.1.1   Thick-Film Copper Resistivity Example

A copper thick-film conductor, 0.2 in. long and 0.01 in. wide, is fabricated using the standard screen-printing process and is shown in Figure 8.3. The ink manufacturer's data sheet specifies a resistivity of 1.9 to 4.8 mΩ/□ for a 13-μm fired thickness [5]. Using the worst-case value of 4.8 mΩ/□, the resistance of the conductor is calculated using Equation 8.6.

$$R = \frac{\rho L}{w} = \frac{4.8 \times 10^{-3} \times 0.20}{0.01} = 0.096\,\Omega = 96 \ \textit{milliohms}$$

8.2.1.2   Direct Bond Copper Resistivity Example

A 0.008 in. thick copper conductor with the same length and width as the thick-film conductor described above is fabricated using the direct bond copper (DBC) process. The resistance is calculated using Equation 8.4 and found to be 16.9 mΩ:

$$R = \frac{\rho_0\,L}{w\,t} = \frac{1.72 \times 10^{-6}\,\Omega - cm \times 1/2.54\,cm/in \times 0.200\,in}{0.010\,in \times \ 0.008\,in} = 1.693 \ \mathrm{m}\Omega$$

$$R = 16.9 \ \mathrm{m}\Omega$$

8.2.2   Efficiency

In high-power applications, the efficiency (η) of a circuit is an important design parameter and is defined as follows:

$$\eta = \frac{\textit{Power output}}{\textit{Power input}} = \frac{P_{out}}{P_{in}} \tag{8.7}$$

Any power lost because of internal dissipation in conductors reduces the power output and thus reduces the efficiency. Examples of circuits where efficiency is usually a critical parameter include motor controls and DC/DC converters. Figure 8.4 shows a simplified block diagram for a DC/DC converter. Let the input be 100 V at 1.0 A. The input power to the converter is:
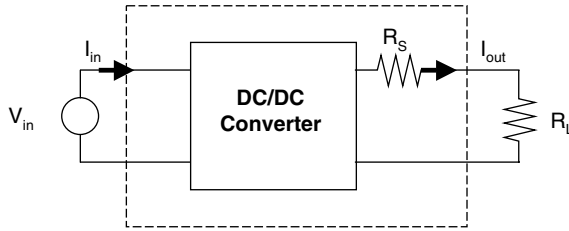
FIGURE 8.4
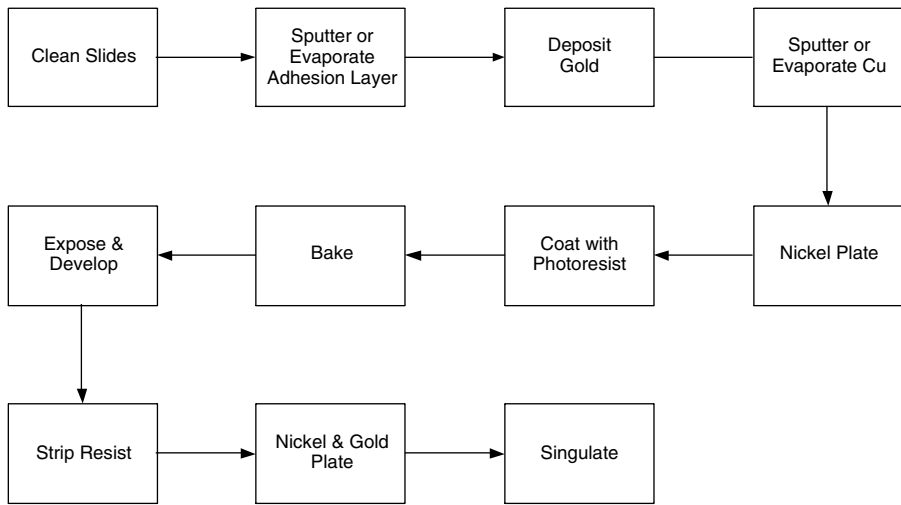Simplified block diagram of a DC/DC converter. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

$$P_{in} = V_{in} \times I_{in} = 100 \text{ V} \times 1.0 \text{ A} = 100 \text{ W} \tag{8.8}$$

Assume that the electronics portion of the converter has an efficiency of 90%. If the equivalent output-interconnect resistance R_s were zero, then the output power would be:

$$P_{out} = 0.9 \times 100 \text{ W} = 90 \text{ W}$$

The power lost in the electronics is $100 - 90 = 10$ W.

In the ideal case, the interconnect resistance would be zero. However, in the real world, R_s always has a finite value and needs to be considered when modeling the electrical performance. The power lost in R_s is calculated from

$$P_s = I_{out}^2 \times R_s \tag{8.9}$$

Assume that the converter's output current is 10 A and $R_s = 0.2$ Ω. Then the power lost (P_{RS}) in resistor R_s is

$$P_{RS} = I_{out}^2 \times R_s = 10^2 \times 0.2 = 20.0 \text{ W}$$

The overall power loss (P_{loss}) in the circuit in Figure 8.4 is

$$P_{loss} = 10 + 20 = 30 \text{ W}$$

From Equation 8.8, the overall efficiency of the converter is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{100 - 30}{100} = 70\%$$

The overall efficiency can be improved in one of two ways. The circuit designer can make circuit changes that will improve the 90% efficiency. The other way of improving the efficiency is to reduce the interconnect losses attributed to R_s by reducing the electrical resistance of the conductors.

8.2.3   Propagation Delay

The delay time in a circuit is equal to the sum of the delays in the active circuits and in the interconnections. The delay (t_d) introduced by interconnections is the product of the interconnect resistance (R) and the capacitance (C). This can be expressed as:

$$t_d = R\,C. \tag{8.10}$$

Changing a conductor metallization from an equal width and thickness of gold to copper will reduce the propagation delay by 27%. A copper conductor can be made narrower than a gold conductor and maintain the same propagation delay. This results in an increase in density without degrading the delay time.

8.3   Thermal and Mechanical Properties of Copper

Table 8.1 lists the various thermal and mechanical properties of copper.

Pure or elemental copper, also known as oxygen-free high-conductivity copper (OFHC), has a low annealing point. When annealed, the mechanical properties change as listed in Table 8.1.

TABLE 8.1

Thermal and Mechanical Properties of Copper

Parameter	Units	OFHC Cu	Annealed Cu
TCE	ppm/°C	17.0	16.4
Thermal conductivity	W/m·K	401	385
Modulus of elasticity	GPa	117	110
Shear modulus	GPa	44	46
Density	g/cm^3	8.9	8.96
Tensile strength, ultimate	MPa	261–441	210
Tensile strength, yield	MPa	49–78	33
Poisson's ratio	—	0.31	0.343

Sources: From CRC, *CRC Handbook of Chemistry and Physics*, Boca Raton, FL: CRC Press, 1984; MatWeb: The Online Materials Information Resource, 2002, www.matweb.com, accessed September 2003.

8.4   Direct Bond Copper (DBC)

DBC is a patented [7] process that was developed at the General Electric Company. In this process, copper is eutectically attached to oxygen-bearing ceramics such as alumina and beryllium oxide without any adhesive or bonding material. In the copper–oxygen phase diagram shown in Figure 8.5, copper and oxygen have a eutectic point at 1065°C. At this point on the phase diagram, there is 0.39% oxygen. When oxidized copper is placed in intimate contact with oxygen-bearing ceramics between 1065 and 1083°C (the melting point of copper), the copper fuses with the ceramic. It is imperative that the copper does not exceed its melting point in the direct bonding process. Figure 8.6 shows a cross section of DBC on alumina or beryllia oxide substrates. There is a thin layer of Cu-O between the ceramic and the copper. In ceramic interconnect applications, such as substrates and packages, the thickness of the copper foil can range from 0.001 to 0.020 in. Because annealed copper has a coefficient of thermal expansion (CTE) of 16.4 ppm/°C [6], which is many parts per million higher than that of the ceramic, it can place the ceramic in tension and possibly cause it to warp or to crack. To prevent warping and cracking due to CTE mismatch, manufacturers of DBC typically place equal amounts of copper on both sides of the ceramic. Usually, the circuit pattern is defined on one side of the ceramic, and a full sheet of copper is direct bonded on the back side. The equivalent CTE of 0.008 in. of copper direct bonded to a 96% alumina substrate (with equal amounts of copper on each side) is 6.8 ppm/°C [8].
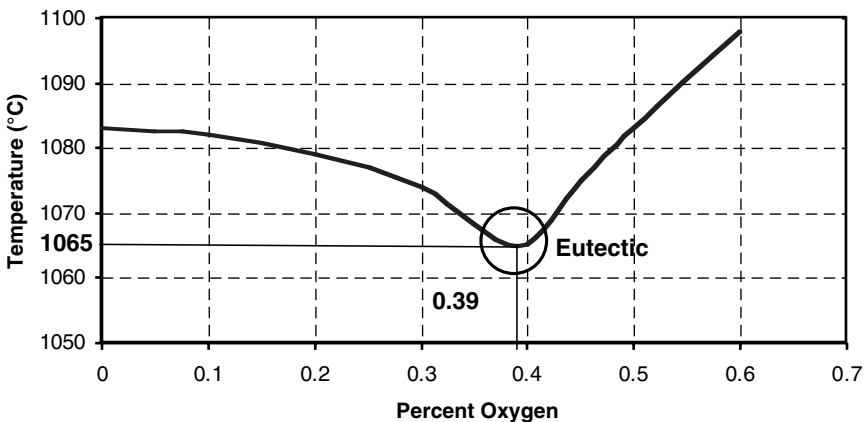
FIGURE 8.5
Cu-O phase diagram. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

Note: Not to scale
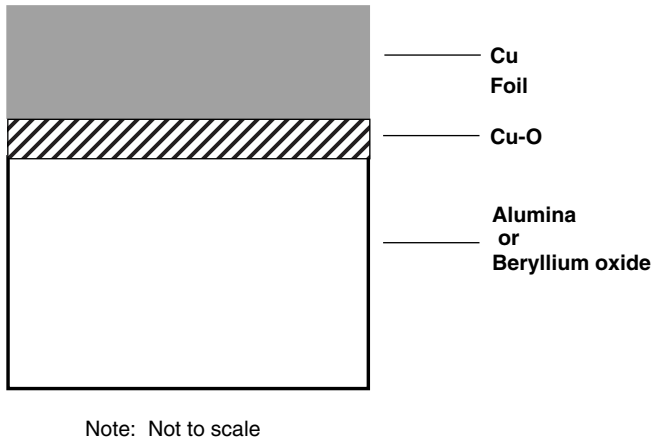
FIGURE 8.6
Cross section of DBC on alumina and BeO. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

Direct bonded copper exhibits high peel strengths — greater than 65 N/cm. Assembly steps, such as reflow soldering, at temperatures under 400°C do not significantly degrade the adhesion of the copper.

In principle, copper can be direct-bonded to any thickness of ceramic. However, for ceramics less than 0.010 in. thick, it is difficult to control the bending caused by the mismatch in CTE between the copper and the ceramic. Therefore, DBC manufacturers typically have a 0.010 in. thickness minimum on their ceramics. Thicker ceramics are less prone to bending [8,9].

In addition to bonding ceramics to copper, the DBC process can bond copper to copper, or copper to copper composites, and oxygen-bearing ceramics to copper composites [10].

DBC is used for its excellent heat-spreading capabilities and for its ultralow electrical resistance.

8.4.1   DBC Process

The process flow for DBC for oxygen-bearing ceramics, such as alumina and beryllium oxide, is shown in Figure 8.7. The process starts with the copper foil cut to the size of the ceramic and then oxidized. The foil is then placed in physical contact with the ceramic and placed in a furnace with the temperature between the copper–oxygen eutectic point of 1065°C and the melting point (1083°C) of copper. As a result of this controlled temperature excursion, the copper fuses with the ceramic. The bonded assembly of copper and ceramic is then cooled to ambient temperature. To define circuit patterns, the copper is typically etched using a wet-etching process. Photoresist is deposited on the metallized ceramic, baked on, exposed, and then developed. The entire substrate or package is then immersed in a liquid etch bath,
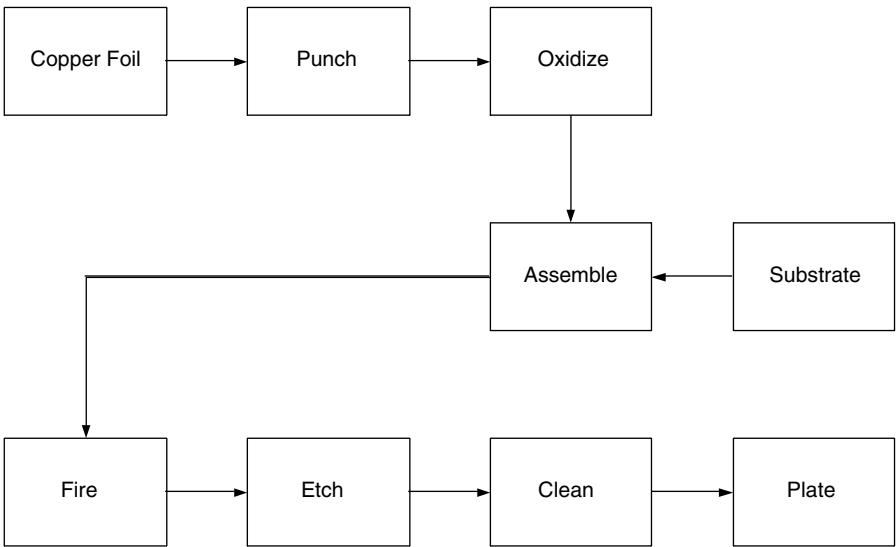
FIGURE 8.7
DBC process flow for BeO and Al$_2$O$_3$. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

consisting of either a strong acid or base solution, where the pattern is defined. After removal from the etch bath, the photoresist is removed. The resulting copper pattern is then plated with nickel and gold, if required.

If freely supported copper leads are required, the process is modified as shown in Figure 8.8. The copper foil is first stamped to size to form the circuit patterns and leads. Copper oxidation is the next step. The foil is then assembled to the ceramic and put through the furnace using the same temperature
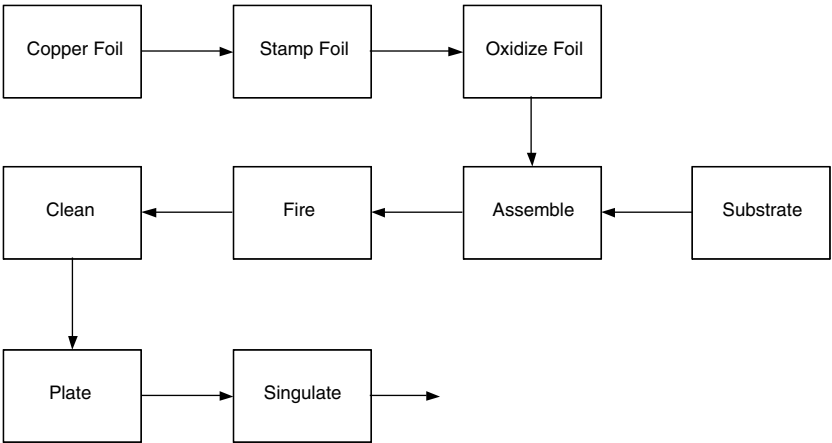
FIGURE 8.8
DBC process flow for DBC with freely supported leads.
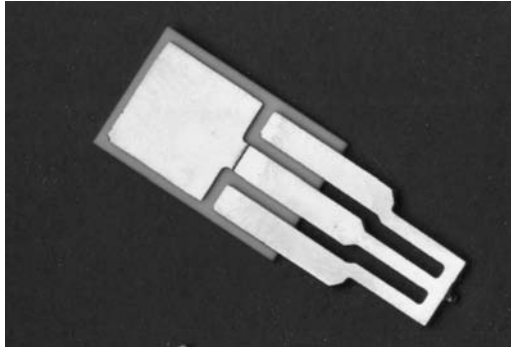
FIGURE 8.9
DBC with freely supported leads. (From Brush Wellman, Inc., DBC Product Literature.)
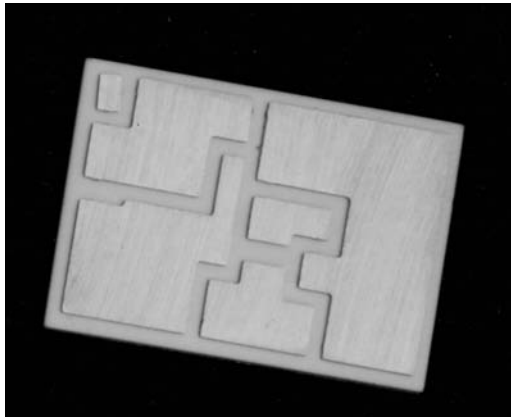
FIGURE 8.10
DBC-etched pattern. (From Hughes Aircraft, Product Literature, 1993. With permission.)

profile described above. The completed assembly is then plated with nickel and gold (if required). Figure 8.9 shows direct bonded copper metallization with freely supported leads. Figure 8.10 shows a DBC substrate with an etched conductor pattern.

When aluminum nitride (AlN) is bonded to copper with the DBC process, the surface of the ceramic first needs to be converted with heat and oxygen to alumina. This results in a thin layer (1–2 μm) of oxygen-bearing alumina. The cross section of copper direct bonded to AlN is shown in Figure 8.11 [11]. The oxidized AlN is then placed in the furnace with the copper foil in the same manner as with alumina and beryllium oxide. The process flow for DBC on AlN is shown in Figure 8.12.

Multiple etched patterns can be made on the ceramic prior to singulating the substrate with either laser scoring or diamond cutting [12].
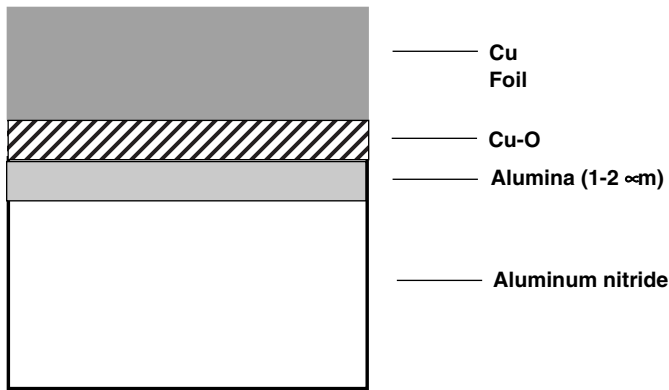
Note: Not to scale

FIGURE 8.11
Cross section of DBC on AlN. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)
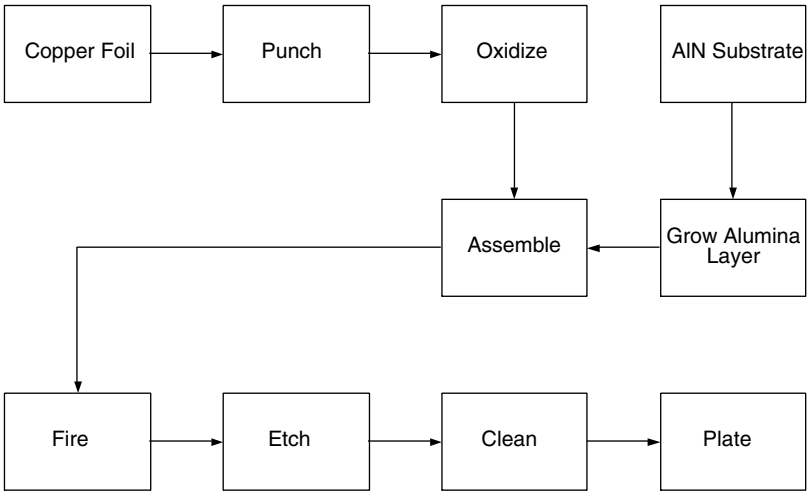
FIGURE 8.12
DBC process flow for AlN.

8.4.2 Thermal Spreading in DBC

As described in Section 8.1, copper promotes excellent heat spreading. When copper is direct-bonded to ceramic substrates, the equivalent thermal conductivity (K_e) of the ceramic substrate assembly is significantly higher than without the copper and can be defined using the following equation [13]:

$$K_e = \frac{\sum\limits_{i=1}^{n} K_i t_i}{\sum\limits_{i=1}^{n} t_i} \qquad (8.11)$$

where

K_e = equivalent thermal conductivity
K_i = thermal conductivity of each material
t_i = thickness of each material
n = number of materials.

8.4.2.1 Example of Equivalent Thermal Conductivity of DBC

A DBC substrate is made with two layers of copper, 0.008 in. thick and 0.025 in. thick 96% alumina as shown in Figure 8.13. Find the equivalent thermal conductivity.

The dimensions are first converted to metric.

$$t_1 = 0.008\ in \times 2.54 \times 10^{-2}\ m\ /\ in = 2.03 \times 10^{-4}\ m$$

$$t_2 = 0.025\ in \times 2.54 \times 10^{-2}\ m\ /\ in = 6.35 \times 10^{-4}\ m$$

Using Equation 8.11, the equivalent thermal conductivity is calculated.

$$K_e = \frac{\sum\limits_{i=1}^{n} K_i t_i}{\sum\limits_{i=1}^{n} t_i} = \frac{(401 \times 2.03 + 21 \times 6.35 + 401 \times 2.03) \times 10^{-4})}{(2.03 + 6.35 + 2.03) \times 10^{-4}} = 169.2\ W\ /\ m - K$$

By bonding the copper to the alumina, the effective thermal conductivity of the substrate or package is increased from 21 to 169 W/m·K.
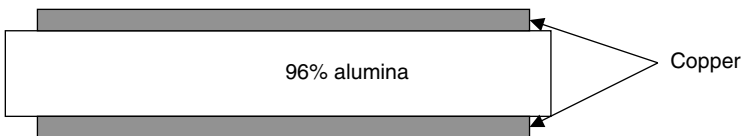
FIGURE 8.13
DBC equivalent thermal conductivity. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)
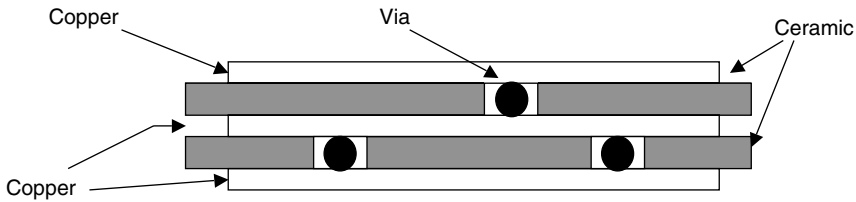
FIGURE 8.14

Multilayer DBC. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

8.4.3 Multilayer DBC

Multilayer structures of DBC substrates can be made using the same copper–oxygen eutectic principle. Two sheets of copper can be bonded together or a sandwich of several copper–ceramic layers can be made as shown in Figure 8.14.

To make electrical connections between the front and back of a DBC substrate, vias are required. The process starts with a hole in the ceramic formed with either mechanical drilling or with laser ablation. A copper sheet is then direct-bonded to one side. The via is formed by placing either a copper ball or a copper blank in the hole, placing the second sheet of copper on the ceramic, and firing using the standard DBC process. When the copper ball is used as shown in Figure 8.15, its diameter is slightly larger than the thickness of the ceramic. When a copper blank is used, its thickness is less than the thickness of the ceramic. An alternate technique for fabricating the via is to press the front copper conductor to the back conductor and then electrically weld the two together [11].

When the thick copper, such as that used in the DBC process, is etched to form the interconnect pattern, the sidewalls of the conductor are typically
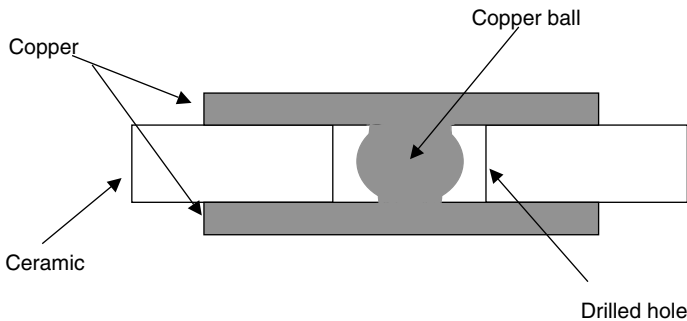
FIGURE 8.15

Cross section of a copper ball used for a via in DBC substrate.
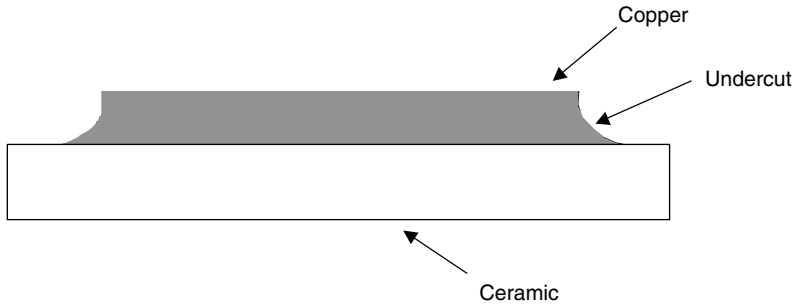
FIGURE 8.16
Etched DBC conductor sidewall showing undercut. (From Schulz-Harder, J., DBC Substrates as a Base for Power MCM's, in *EPTC*, Singapore, 2000. With permission.)

undercut as shown in Figure 8.16. The amount of undercutting is approximately equal to half the conductor thickness. For narrow conductor widths with thick copper, the undercutting needs to be taken into account when calculating the electrical resistance.

The width of etched copper conductors is a function of the copper thickness. A 0.010-in.-wide conductor is one manufacturer's minimum when used with 0.005-in.-thick copper. For 0.012-in.-thick copper, the minimum line width increases to 0.0275 in. The spacing between etched conductors ranges from 0.010 to 0.030 in., depending on copper thickness [8].

Many users of DBC specify electroless nickel plating to prevent the copper from oxidizing. Typically, this electroless nickel plating is 50 to 400 μin. thick and provides excellent solderability. This may be followed by a flash plating of gold, 0.4 to 6.0 μin. thick [8].

Ultrasonic aluminum wire bonding is easily accomplished with the nickel-plated DBC. It should be noted that ultrasonic wire bonding of aluminum wire to copper can be effected; the resultant bond is not as reliable as with the nickel plating. Gold thermocompression or thermosonic wire bonding requires at least 50 μin. of gold plating.

The use of free-standing leads in the DBC process gives an advantage in the subsequent assembly steps; lead attachment is not required. In addition, there are no solder joints between the leads and the substrates. This leads to a more reliable assembly.

By using the multilayer DBC process and free-standing leads, hermetic packages can be formed. An example is shown in Figure 8.17. The extremely wide leads have a very low voltage drop and very high current-handling capability.

8.4.4 Resistors

From a temperature standpoint, the processing of thick-film resistors is compatible with the DBC process. The DBC joining process occurs between 1065
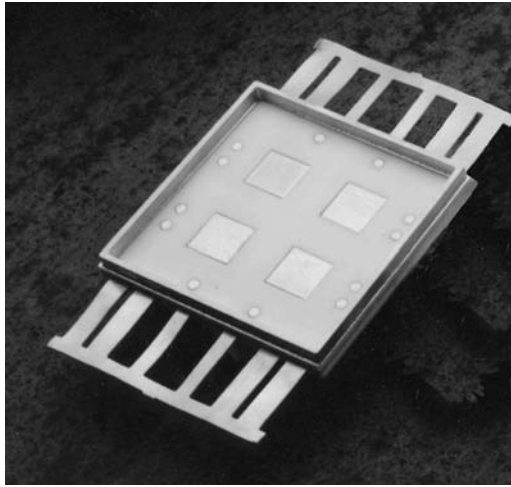
FIGURE 8.17
DBC package. (From Hughes Aircraft, Product Literature, 1993. With permission.)

and 1083°C and subsequent oven excursions for thick-film resistor firing at 900°C will not have any effect on the adhesion of the copper to the ceramic. However, the thick copper conductors may interfere with the screen and not allow accurate deposition of resistor inks. Sufficient openings in the copper pattern are required for the screen to contact the ceramic.

Instead of screen-printing thick-film resistors on DBC substrates, many manufacturers use resistor chips.

8.5 Active Metal Brazing (AMB)

Active metal brazing (AMB) is a process to braze metals, such as Kovar®*, titanium, copper, and molybdenum, to ceramics. The process does not require a metallization on the ceramic. For this chapter, only copper brazing will be addressed. The AMB process is used by some manufacturers as an alternative to DBC as it provides higher adhesive strength while using a less critical furnace profile. It also does not rely on oxide formation as in the DBC process.

8.5.1 AMB Process

The process, as shown in Figure 8.18, starts with the application of the braze material in the form of a film, powder, or paste. The braze materials may be

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* Kovar is a registered trademark of Carpenter Technology, Inc.
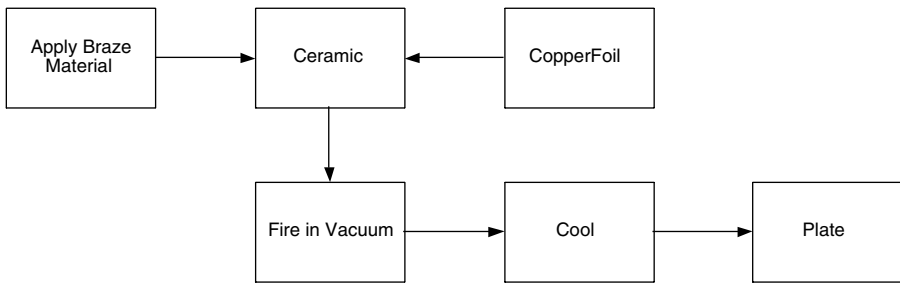
FIGURE 8.18
Active metal braze process flow.

titanium, hafnium, or zirconium. The copper, the braze material, and the ceramic are then heated to a temperature higher than the melting point of the braze material in a vacuum 10^{-5} torr or better. The vacuum atmosphere is required to prevent the copper from oxidizing. The furnace temperature profile is not as critical as in the DBC process because it relies only on raising the temperature into the liquidus region and does not have a maximum. The active metal in the braze alloys reacts with the surface of the ceramic forming a liquidus with the oxygen in the system, which then acts to bond the metal to the ceramic.

After the temperature is returned to ambient, the part is then cleaned and plated in a manner similar to that used for DBC. Although etching of the copper is easily accomplished with standard etching solutions, there is a rather tenacious, electrically conductive reaction layer remaining on the ceramic, which can be removed with aggressive mechanical abrading [14].

After plating, the resultant brazed copper has the same wire bonding and solderability characteristics as DBC [15].

8.5.2   AMB Characteristics

Because the AMB process uses copper sheets as the metallization, the electrical and thermal performances are identical to that of DBC. It should be noted that the ceramic interaction with the active metal in the braze material has a high thermal conductivity and can be neglected in most thermal analyses.

8.6   Thick-Film Copper

Thick-film copper metallization is typically selected for the low cost of the conductor inks in comparison to gold inks. Other thick-film conductor inks, such as silver and palladium silver, are also used when low material cost is

the objective. As pointed out in an earlier section, silver metallization is subject to reliability-degrading migration.

Copper conductors can be deposited and defined in either one of two processes: thick-film screen printing and etched thick film. In the former process, thick-film inks are forced through a screen in a definite pattern, dried, and fired. In the latter process, a blanket coat of conductor ink is applied to the ceramic with a screen and fired. It is then etched to the final pattern using classical photolithographic techniques. Line widths in this etch process can be as narrow as 0.001 in., whereas the classical screen-printed conductor can only be as narrow as 0.004 in.

The firing process for thick-film copper is different from that of other thick-film conductors. Because copper readily oxidizes in the presence of oxygen, the standard thick-film firing process must be modified to prevent the oxidization. Instead of air flowing through the furnace, dry nitrogen with less than 10 ppm of oxygen is used [5].

Multilayer conductor patterns can be used with copper conductors. The design of the conductors and dielectrics is the same as with gold and silver-based thick-film inks. However, the dielectric materials used for copper inks are specially formulated for firing in a nitrogen atmosphere with low oxygen content. The copper via-fill materials used with copper conductors are also specially formulated.

8.6.1 Copper Ink Formulations

Thick-film copper conductor inks are not pure copper. The ink consists of a functional material of copper, a solvent, a temporary binder, and a permanent binder. The permanent binder tailors the CTE to that of the substrate. It also aids in the adhesion of either the substrate or the dielectric. The thick-film firing process in nitrogen burns out the solvent and temporary binders. This leaves just the copper and the permanent binder. In addition to tailoring the CTE, the permanent binder significantly reduces both the electrical and thermal conductivities of the conductor. A typical fired conductor thickness is 15–18 μm. If it were pure copper, it would have a sheet resistivity of 0.94–1.13 mΩ/$\square$. The 9924 thick-film copper conductor material from EI DuPont Electronics specifies a sheet resistivity of 1.9–4.8 mΩ/ for the same thickness. This results in the published resistivity of this thick-film material being only 23% of the resistivity of pure copper.

Thick-film ink manufacturers do not publish thermal conductivity data for their conductor and via-fill inks. Work by Harshbarger [16] and Krum [17] has shown that the thermal conductivity of thick-film conductor inks is approximately 20% of that of pure metals. A first-order approximation of the thermal conductivity of thick-film conductor inks is to multiply the percentage of the published value of electrical conductivity (the reciprocal of resistivity) of the ink and the thermal conductivity of the pure metal in the ink. For copper thick film, as described in the above example, the electrical

conductivity is only 23% of the electrical conductivity of pure copper. There-fore, the thermal conductivity can be approximated by

$$K = 23\% \times 401 = 92 \text{ W/m·K.}$$

8.6.2   Metallizing Processes

In the thick-film process, the ceramic can be metallized with a circuit pattern in one of two ways: screen printing the pattern or etching the pattern.

8.6.2.1   Screen Printing

In the classical method of thick-film metallization shown in Figure 8.19, conductor ink pastes are forced through defined openings in a stainless steel screen mesh. The ink pattern on the substrate is then dried and fired. The drying of the conductors is typically for 10–15 min at 120°C. The firing profile is typically a temperature ramp from ambient to 900°C, a dwell of 10 min at this temperature, and a ramp down to ambient. As stated earlier, the firing is done in a nitrogen atmosphere. The overall firing cycle is approximately 1 h in length. For multilayers, layers of dielectric materials are screen printed over the conductor patterns with openings for interlayer interconnections. After two to three printings of a dielectric layer, the substrate is again dried and fired. Via-fill inks are screen printed in the openings, dried, and fired. Some substrate manufacturers may use a stencil instead of a screen to fill the vias. Additional conductor patterns are then applied in the same manner as with the first conductor layer. Line widths as fine as 0.004 in. are possible with this process.

8.6.2.2   Etched Thick Film

In the etched pattern process as shown in Figure 8.20, thick-film conductor ink is blanket-coated onto a ceramic substrate using standard thick-film screening. After drying and firing, the pattern is etched using a photolitho-graphic process. Line widths as fine as 0.001 in. are made with this process.

A variation on the above photoetching process uses thick-film inks that are photosensitive. This eliminates the need for the photoresist application and removal steps. Although photosensitive conductors and dielectrics for use with gold and silver are available, similar materials for use with copper are not.

8.6.3   Thick Film with Plated Copper

To make use of the excellent thermal and electrical properties of plated copper, an adhesion layer is required between the ceramic and the copper. One tech-nique for doing this is to apply a thick-film adhesion layer on the ceramic.
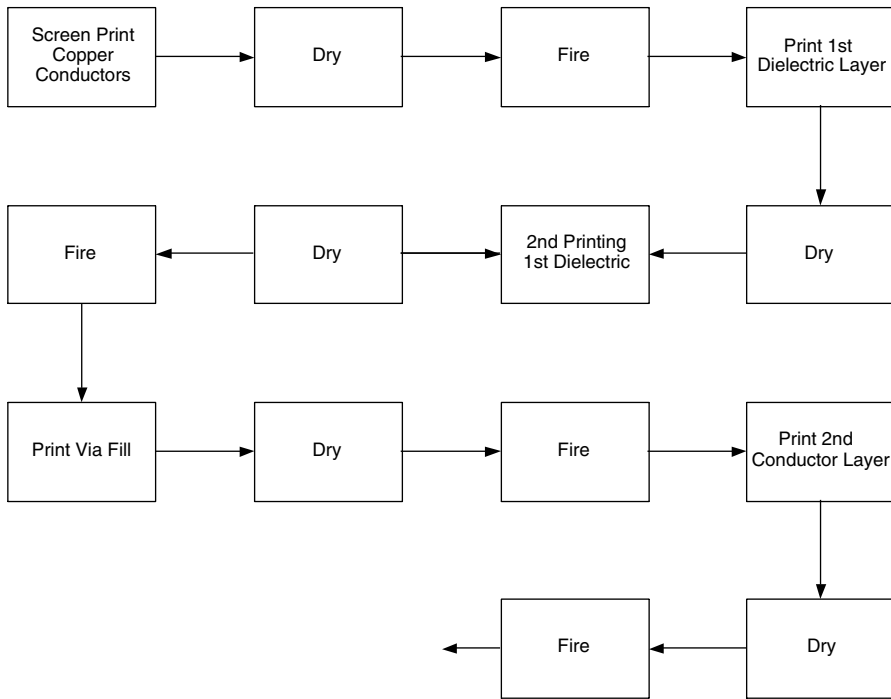
Note: Two dielectric printings are shown. Some manufacturers use 3 or 4.

FIGURE 8.19
Screen printing — thick-film copper process flow for two conductor layers.

8.6.3.1   Process

A copper metallization technique that combines both thick-film and copper plating is offered by one manufacturer [18]. This process starts with the screen printing of thick-film conductors on the alumina or beryllium oxide ceramic. After drying and firing, the conductors are electrolytically copper plated to a thickness ranging from 0.001 to 0.010 in. The sheet resistivity of the conductors can be as low as 70 $\mu\Omega/\square$. Line widths for thick conductors (0.010 in.) can be as narrow as 0.008 in. A cross section showing the layer buildup of plated copper on thick film is shown in Figure 8.21. Metallized through-holes and solid vias are available in this technology. Because the solid through-holes are filled with silver thick film, the thermal conductivity can be approximated at 20% of bulk silver's 419 W/m·K, that is, 83 W/m·K.

This process is capable of fabricating screen-printed resistors as well as fine-line conductors. Because this process uses thick-film inks, it is also capable of multilayers when compatible dielectrics are used.

This thick-film/plated-copper process yields conductors with both high thermal conductivity and low electrical resistivity. A very good first-order approximation of both parameters is to use the values for pure copper: 401
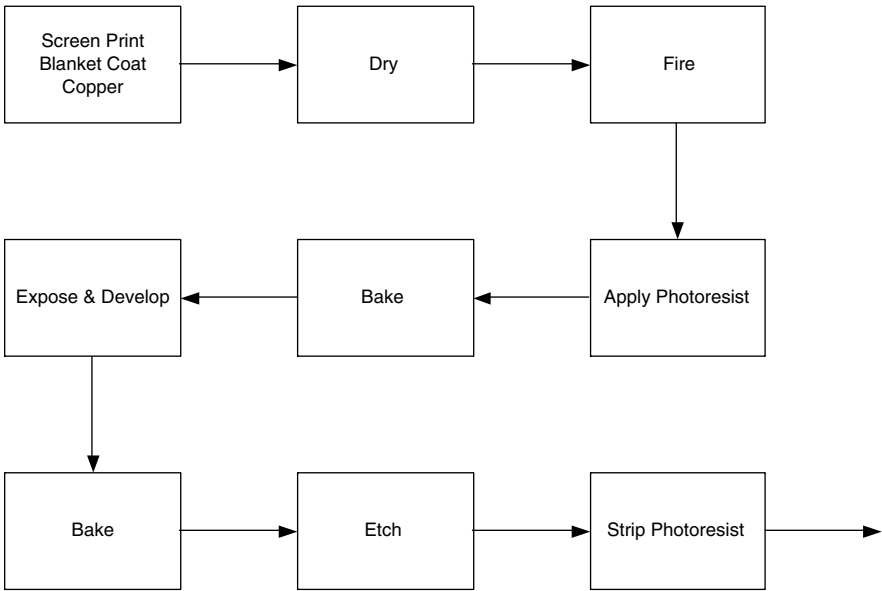
FIGURE 8.20
Etched thick-film process flow. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)
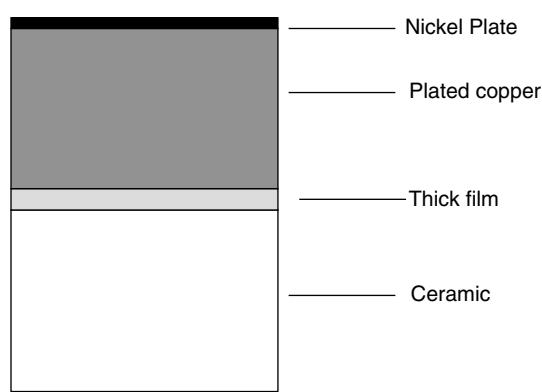
FIGURE 8.21
Layer buildup for plated copper with thick-film adhesion layer. (From Remtec, Remtec Product Data, http://www.remtec.com, accessed September 2003.)

W/m·K and 1.72 μΩ·cm. However, to be exact, the influence of the thick-film base layer needs to be taken into account. For a semiconductor mounted on a plated copper conductor over the thick film as shown in Figure 8.22a, the heat will flow from the semiconductor, through the die attach, through the copper conductor, through the thick-film adhesion layer, and into the
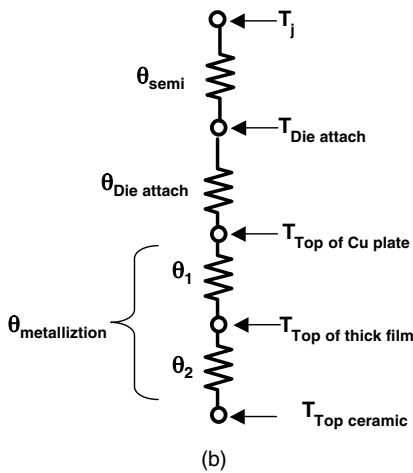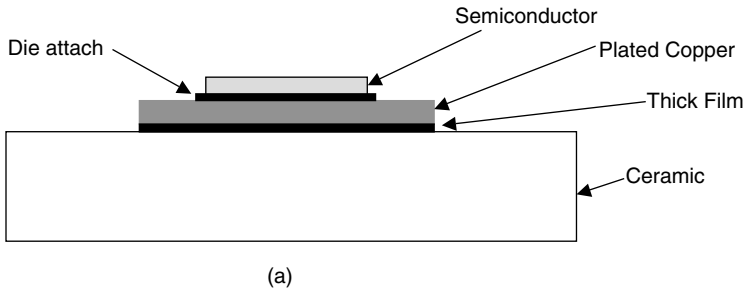
FIGURE 8.22
(a) Cross section of thick film with plated copper. (From Remtec, Remtec Product Data, http://www.remtec.com, accessed September 2003. With permission.) (b) Analog of thermal model.

ceramic. Figure 8.22b shows the electrical analog for this thermal path. The thermal resistance from semiconductor junction to the top of the substrate is

$$\theta_{Total} = \theta_{semi} + \theta_{die\ attach} + \theta_1 + \theta_2. \tag{8.12}$$

The portion of the heat path of interest here is the thermal resistance of the metallization, $\theta_{metallization,}$ which is equal to the sum of the thermal resistances in the vertical direction of the plated copper (θ_1) and the thick-film adhesion layer (θ_2).

$$\theta_{metallization} = \theta_1 + \theta_2. \tag{8.12}$$

The plated copper top layer of the conductor has a thermal conductivity of 401 W/m·K and spreads the heat extremely well.

From Equation 3.22 (in Chapter 3), the thermal resistance for an area A can be calculated as follows:

$$\theta_1 = \frac{t_1}{k_1 A} \tag{8.13}$$

$$\theta_2 = \frac{t_2}{k_2 A} \tag{8.14}$$

where
  t_1 = thickness of plated copper
  k_1 = thermal conductivity of plated copper
  t_2 = thickness of thick film
  k_2 = thermal conductivity of thick film

Combining Equation 8.12 to Equation 8.14

$$\theta_{metallization} = \frac{t_1}{k_1 A} + \frac{t_2}{k_2 A}. \tag{8.15}$$

In the thick-film/plated-copper process, the equivalent sheet resistivity parallel to the plane of the substrate is the parallel combination of the resistivity of each layer.

$$\frac{1}{\rho_{equiv}} = \frac{1}{\rho_{thick\,film}} + \frac{1}{\rho_{plated\,Cu}}. \tag{8.16}$$

8.6.3.2 *Thick Film with Plated Copper Electrical Resistivity Example*

A 0.002 in. thick copper is plated over a DuPont 9924M copper ink 13 μm thick. Find the equivalent sheet resistivity.

The sheet resistivity of one vendor's [5] thick-film conductor ranges from 1.9 to 4.8 mΩ/□. For this example, 2.0 mΩ/□ will be used.

The bulk resistivity of plated copper is 1.72 μΩ·cm. The thickness of this layer is first converted to centimeters.

$$0.002\,in \times \frac{2.54\,cm}{in} = 5.08 \times 10^{-3}\,cm.$$

The sheet resistivity is calculated using Equation 8.6:

$$\rho = \frac{\rho_0}{t} = \frac{1.72 \times 10^{-6}\ \Omega - cm}{5.08 \times 10^{-3}\ cm} = 0.339 \times 10^{-3}\ \Omega\ /\square = 0.339\ m\Omega\ /\square$$

Using Equation 8.16, the equivalent sheet resistivity is calculated.

$$\frac{1}{\rho_{equiv}} = \frac{1}{\rho_{thick\,film}} + \frac{1}{\rho_{plated\,Cu}} = \frac{1}{2} + \frac{1}{0.339} = \frac{1}{3.44}$$

$$\rho_{equiv} = 0.289\ m\Omega/\square.$$

By plating the conductor with 0.002 in. of copper, the sheet resistance was reduced from 2.0 mΩ/$\square$ to 0.289 mΩ/$\square$, an 85% reduction.

8.6.3.3 *Thick Film with Plated Copper Thermal Example*

A chip whose effective area is 10 × 10 mm is soldered to a conductor of plated copper on thick film. Find the thermal resistance of the metallization. The thick-film thickness is 10 μm. The plated copper thickness is 0.002 in.
Converting the plated copper thickness to meters:

$$0.002\,inch \times 2.54 \times 10^{-2}\ \frac{m}{inch} = 5.08 \times 10^{-5}\ m.$$

Assume that the thermal conductivity of the thick-film copper is 20% of pure copper.

$$\theta_{Total} = \frac{t_1}{k_1\,A} + \frac{t_2}{k_2\,A} = \frac{5.08 \times 10^{-5}}{401 \times 10^{-4}} + \frac{10 \times 10^{-6}}{0.2 \times 401 \times 10^{-4}} = 2.51 \times 10^{-3}\,^{\circ}C\,/\,W.$$

If the entire copper layer (the thick-film and the plated copper) were treated as pure copper, the thermal resistance would have been:

$$\theta_{Total} = \frac{t_1}{k_1\,A} = \frac{5.588 \times 10^{-5}}{401 \times 10^{-4}} = 1.39 \times 10^{-3}\,^{\circ}C\,/\,W.$$

Although the percentage difference in the two calculations is rather significant, the overall thermal resistance in the copper thick-film can be considered negligible. If the thick-film ink were silver-based instead of copper-based, then the thermal resistance degradation would be considerably less.

8.6.4 Multiple Conductor Printings

To lower the electrical resistivity of a thick-film conductor, some manufacturers print multiple printings of the same copper conductor ink using the same pattern. This process can provide a fired-ink thickness of 20 to 25 μm and a resistivity of approximately 1 to 2 mΩ/□.

8.6.5 Thick-Film Copper Finishes

For substrates metallized with thick-film copper that will see subsequent soldering, manufacturers typically plate them with nickel and optionally with a top layer of gold. Some manufacturers will solder dip their copper thick-film substrates after nickel plating. The resulting metallization has the same solderability and wire bondability characteristics as DBC and plated copper.

8.7 Thin Film

The thin-film process is defined as the deposition of conductive, resistive, and insulating materials with a thickness of one micron or less onto a ceramic or other insulating substrate. For this chapter, only conductive materials will be discussed [19].

The typical thin-film process, as shown in Figure 8.23, starts with the deposition of a seed or an adhesion layer to the ceramic using either a vacuum evaporation or a sputtering process. The ceramic materials used for thin film include alumina, beryllium oxide, and AlN. This seed or adhesion layer consists of one of the following materials: tantalum, chrome, Nichrome, titanium, or titanium–tungsten. As the name suggests, the layer provides good adhesion to the ceramic substrate and subsequently deposited layers. The thickness of the seed layer ranges from 50 to 300 nm.

The seed layer is followed by the sputtering or evaporation of a thin, (2-μin.) gold layer used as a barrier. The conductor layer is then deposited with sputtering or evaporation. Although many thin-film applications use gold for the conductor layer, copper is the material of choice for high-current designs and for circuits with high interconnect densities. The thickness of the deposited copper can range up to 0.001 in. When a thick layer (greater than 50 μin.) of copper is required, many manufacturers electroplate instead of using thin-film deposition techniques, because it is more cost-effective and time efficient. The plated copper process will be discussed in detail in Section 8.8. To prevent oxidation of the copper layer, nickel is plated onto the metallization. Subsequent gold plating is optional. At this point, the substrate is blanket coated with metallization. A cross section of the metallization is shown in Figure 8.24.

FIGURE 8.23
Thin-film process flow. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)
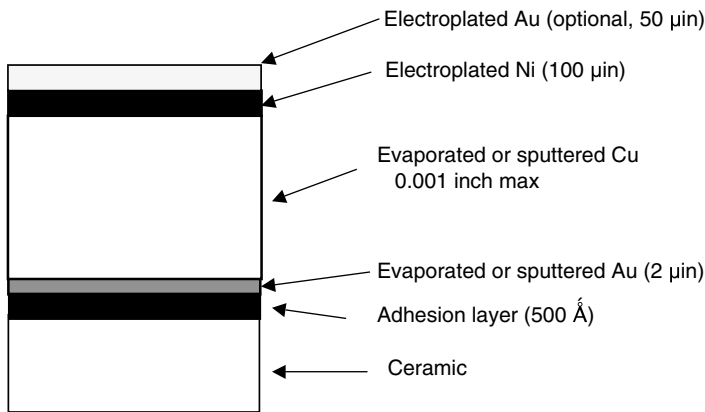
FIGURE 8.24
Thin-film copper cross section. (From Krum, A., Course Notes, UCLA Extension, Engineering 881.152, Power Hybrids: Design and Processing, April 1995. With permission.)

Using standard photolithographic processes, conductor patterns are defined. This starts with the coating of the metallized substrate with photoresist. The resist is then baked on. The conductor patterns are then defined by exposing and developing the photoresist through the conductor mask. Following a short bake, the conductor (and underlying seed layer) is etched. At this point, the remaining photoresist is stripped leaving the final conductor pattern. If deposited thin-film resistors are part of the substrate design, they are now defined with a different mask and additional photolithographic

steps. Typically, multiple patterns are fabricated on a ceramic slide. After the patterns are defined, the individual substrates are singulated.

There is a variety of photoresist materials on the market. Some of these photosensitive materials are negative types and some are positive. Both wet and dry resist materials may be used. It is beyond the scope of this section to discuss the advantages and disadvantages of each. The reader is directed to the references for additional information on the subject [20–22].

If the subsequent assembly process calls for thermocompression or thermosonic wire bonding, the gold plating of the conductors is required. If ultrasonic aluminum wire bonding will be used, the plated nickel layer is sufficient.

Because the adhesion layer in thin film is usually a resistive material such as Nichrome, chrome, or titanium–tungsten, precision-integrated substrate resistors are available.

8.8   Plated Copper

As discussed in Section 8.7, copper can be deposited with evaporation or sputtering to a thickness of 0.001 in. maximum. Although this method of copper deposition works, it is not very efficient because of the amount of time required to deposit that large amount of metal. In lieu of sputtering or evaporating the copper, electroless or electrolytic plating can be used.

Copper can be plated on the surface conductors of both high-temperature cofired ceramic (HTCC) and low-temperature cofired ceramic (LTCC) packages and substrates. On internal layers, on HTCC, the conductors must be composed of high-resistivity refractory metallization.

8.8.1   Electroplating Process

Copper can be electroplated onto the substrate in two techniques. In the first process, as shown in Figure 8.25a, an adhesion or seed layer is deposited on the ceramic. This adhesion layer can be thin film, either sputtered or evaporated, thick film, or refractory metallization. A sputtered or evaporated gold layer is deposited on top of the seed layer for thin-film metallization. Copper is then electroplated to the required thickness. This is followed by electroplated nickel and an optional gold electroplate. Figure 8.26 shows the buildup of plated copper metallization.

Conductor patterns are defined in the metallized ceramic substrate using the same photolithographic processes discussed in the Section 8.7.

An alternative to the above process calls for selective plating of the thick copper layer only on those conductors requiring the improved electrical and thermal conductivities. This process, as detailed in Figure 8.25b, starts in the
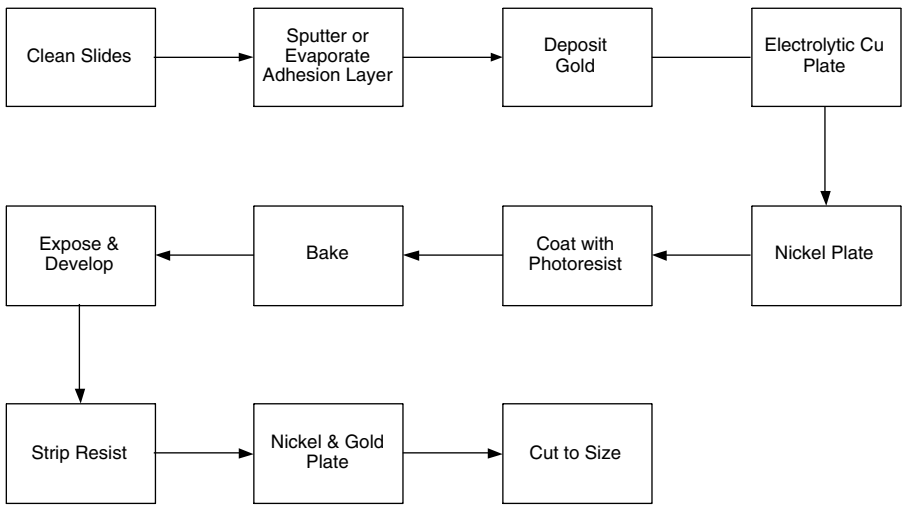
FIGURE 8.25A
Process flowchart for plated copper with thin-film adhesion layer (without resistors). Copper is blanket plated.
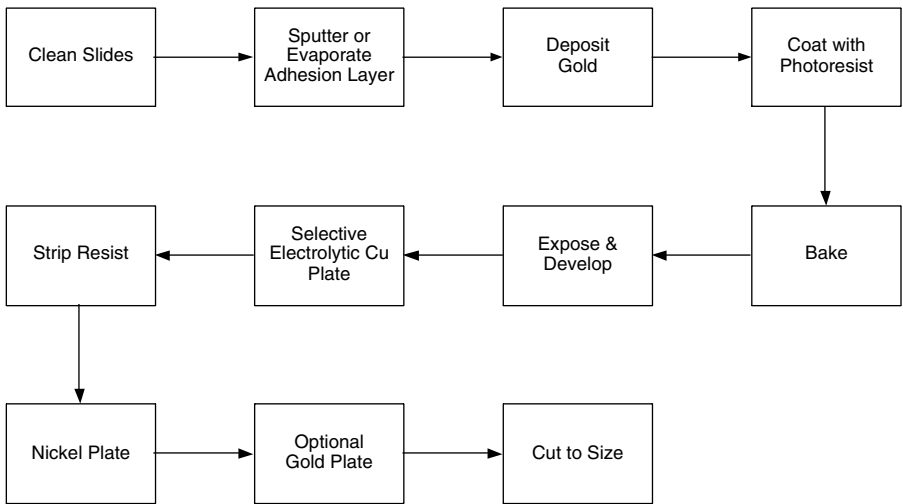
FIGURE 8.25B
Process flowchart for plated copper with thin-film adhesion layer (without resistors). Copper is selectively plated.

same manner with the deposition of an adhesion layer and a thin gold barrier layer. The process changes at this point. The metallized ceramic is coated with photoresist, baked, and developed. What is left is a pattern of photoresist covering those areas where copper plating is not required. The exposed metallization is then electroplated with copper to the desired thickness. The
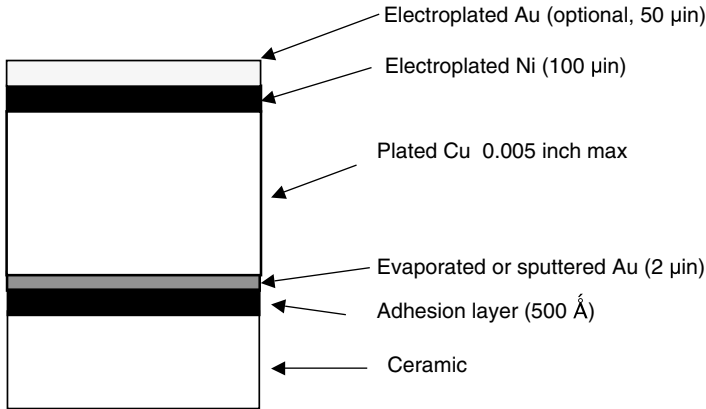
FIGURE 8.26
Layer buildup for plated copper with thin-film adhesion layer.

remainder of the process — photoresist strip with nickel and gold plating — is the same as in Figure 8.25a. The advantages to this technique are twofold. First, the fine lines without significant etch undercutting can be made for low-current signals along with thick copper-plated conductors for the high-current signals. The second advantage is that thermocompression and thermosonic wire-bonding sites do not have the reliability-degrading thick, soft copper underneath them.

A survey of the vendors of the plated copper process [20,21] indicates a maximum plated copper thickness of 0.005 in. This corresponds to a sheet resistivity of 0.135 mΩ/□. There are variations to this process with respect to the nickel and gold layers, which are a function of the manufacturing facility.

If the subsequent assembly process calls for thermocompression or thermosonic wire bonding, plated copper under the wire-bond sites should be avoided. This can be accomplished by selectively plating the copper. When the adhesion layer is Nichrome or titanium–tungsten, then precision-deposited thin-film resistors can be fabricated.

The plated copper process can be used with alumina, AlN, and beryllium oxide substrates.

When the seed or adhesion layer is a thin-film material, then the completed substrate can have integral resistors. The definition of the resistors requires the use of an additional mask step.

Line widths as fine as 0.002 in. are available with the selectively plated copper process whereas 0.005 in. is the minimum line width for the etched blanket-coated copper substrates.

8.8.2   Electroless Process

The electroless copper plating of ceramics was originally developed at PCK Technology Division of Kollmorgen Corporation [23]. A process flow
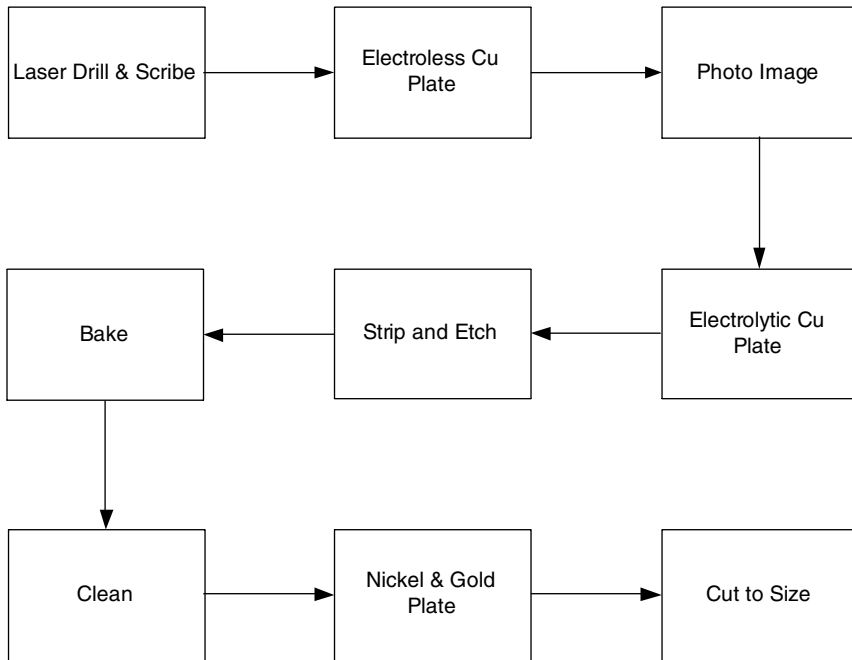
FIGURE 8.27
Electroless plated copper.

diagram is shown in Figure 8.27. The unique portion of this process, the electroless copper plating step, starts with the treating of the ceramic surface with a melt of one or more alkali metal compounds, and then exposing the surface to an acidic halide solution. The treated ceramic surface is then exposed to a copper plating bath to form a uniform metal layer. The ceramic is photo imaged in the classical manner and then electrolytically copper plated. After stripping and etching to obtain the required pattern, the metallized ceramic is baked, cleaned, and nickel plated. For some subsequent assembly processes, a top plating of gold may be required. If the substrate slide contained multiple images, then the last step is singulation.

The ceramic material typically used for this process is 96% alumina. Other ceramics, such as other purity aluminas, beryllium oxide, and AlN may also be used. Thicknesses of the ceramic range from 0.010 in. to as high as 0.085 in. The process is capable of making line widths and spaces as fine as 0.003 in. for copper thicknesses of 0.001 in. For copper 0.0025 in. thick, the recommended line widths and spaces are 0.005 in. For 0.0035 in. thick copper, 0.010 in. lines and spaces are used.

Because the copper used for the metallization is essentially pure copper, the electrical resistivity is 1.72 $\mu\Omega\cdot$cm. For 0.001 in. thick copper, this equates to 0.677 m$\Omega/\square$. The thickest copper used, 0.0035 in. thick has a sheet resistivity of 193 $\mu\Omega/\square$.

The electroless plated copper process is capable of making through-hole vias in the ceramic. The via walls may be metallized or the entire via filled. The minimum size of through-ceramic vias is a function of the laser used for machining.

To prevent blistering in the large areas of copper plating, vent or relief holes in the copper metallization are required. These holes relieve stress during process temperature excursions. The manufacturer of substrates using this process recommends that the vent holes be used whenever a copper pad area exceeds $\frac{1}{4}$ square inch. The holes should be 0.010 in. in diameter on a 0.050-in. pitch. Because vent holes in the metallization will introduce voids, they are not recommended on pads located directly under a high-heat-generating device.

No nickel or gold plating is required for ultrasonic wire bonding of aluminum wire to the plated copper. For gold ball bonding, a gold plate over the copper is required. For soldering, nickel plating is required over the copper [24].

8.8.3   Plating Considerations

As discussed in the previous sections, copper can be either electrolytically plated to an entire surface, and then photographically defined using etching, or selectively plated. In both cases, the entire surface of the part is electrically at the same potential and is then connected to a power supply during the plating operation.

For those packages and substrates where the pattern is defined first, either with thick-film or refractory metallization, electrolytic copper plating requires that the traces be electrically connected. To accomplish this requires the use of temporary shorting bars.

Electrolysis plating does not require the connection of the traces. However, the thickness of the plating using this process is considerably less than with the electrolytic plating process.

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9

Integrated Passives in Ceramic Substrates

Heiko Thust and Jens Müller

CONTENTS

9.1   Introduction

Passive integration is an effective technique to increase the component density. It is defined as a combination of circuit carrier (substrate, board, and interconnections) with passive components like resistors, capacitors, inductors, and line elements in one technology. Passive elements may be integrated on the surface or embedded in a multilayer structure of the substrate. The goal is to achieve:

- Reduced module sizes
- Lower system costs (component reduction)
- Improved electrical performance and thermal performance
- Higher reliability (reduced number of I/O)

The combination of several integrated passives in one package to realize a certain filter response is called integrated passive device (IPD) or passive integrated device (PID). Functional blocks, such as a low-pass filter, are integrated in one package that can be handled like one component. This approach has the further advantage of using a known good filter for assembly.
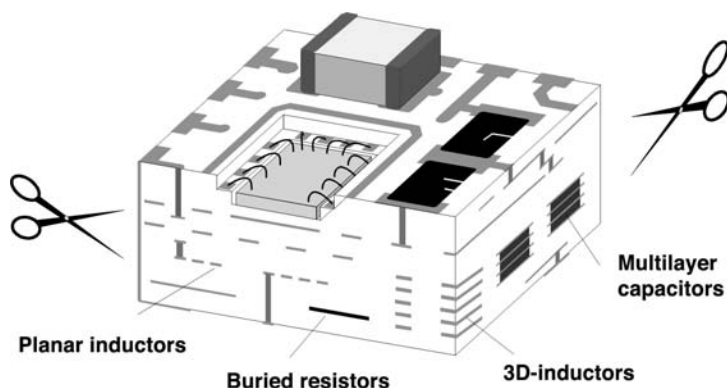
FIGURE 9.1
Vision of a system-in-package with integrated passives in LTCC.

More functionality is achieved by further adding one or more ICs to the module. Fully functional blocks in one package are referred to as *system-in-packages* (SiPs). A vision of this is depicted in Figure 9.1.

Besides the wide use of printed resistors for various applications, the focus of integration for capacitors and inductors is mainly for the radio frequency and lower microwave band of the frequency spectrum. Applications of interest are front-end modules for GSM (Global System for Mobile Communications), filter modules for various wireless applications, and Bluetooth technology.

In particular, low-temperature cofired ceramics (LTCC) is a convenient technology for the manufacturing of band-pass filters for a frequency band of 380–2400 MHz as required by radio telephony systems.

However, one might ask, is there really a need for passive integration? The answer is yes. Its major driving factors are:

- Size (the grown ratio between passives and active devices)
- Cost
- High-frequency performance
- High reliability

In Reference 1, it is stated that the ratio between passive and active components is about 9:1 for a mobile phone. Furthermore, the passives occupy 80% of the space and account for 70% of the cost. Three hundred components is the average passive component count in cellular phones. Road maps for these applications show a clear trend toward higher integration on the chip side. From six ICs necessary for the phone function in 1998, it decreased to one for the third generation of cell phones in 2004 [2]. According to a study by Prismark [3], the need for the embedded component density will grow to about 30 passives/cm^2 in the year 2010.

Integrated passives can be divided into groups of lumped and distributed elements by virtue of their electrical nature. Both types can be realized as
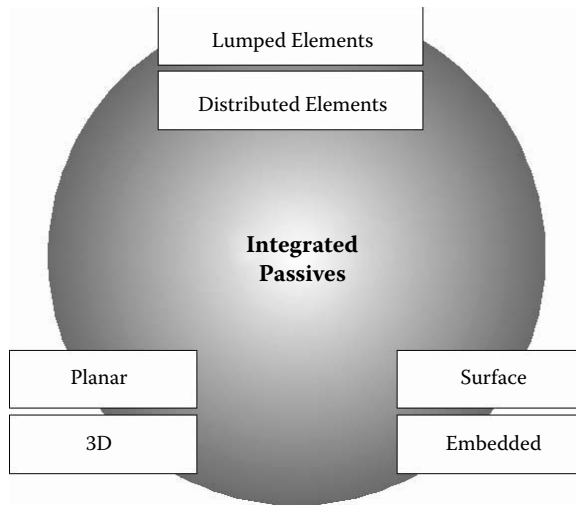
FIGURE 9.2
Classification of integrated passives.

embedded or on the surface of the substrate. According to their mechanical structure, we further distinguish between three-dimensional (3-D) and planar elements (Figure 9.2).

To achieve the goals mentioned in the preceding text, these integrated passives have to fulfill a set of requirements; namely:

- Low tolerances
- Good manufacturability
- High stability and reliability
- Good trimmability

All these are determined by material and design. Their impact is explained in the following sections.

9.2   Materials and Technologies for Lumped Elements

The process of printing, drying, and firing (especially, cofiring in LTCC technology) requires a matched thermal coefficient of expansion (TCE) and chemical compatibility between inks and substrates or tapes during all processing steps. A complete matched material system of substrates/tapes, conductors, dielectrics, resistors, glass-protection inks, etc., is necessary.

It is not advisable to combine materials from different suppliers or different systems, because the material compositions are different and may vary.
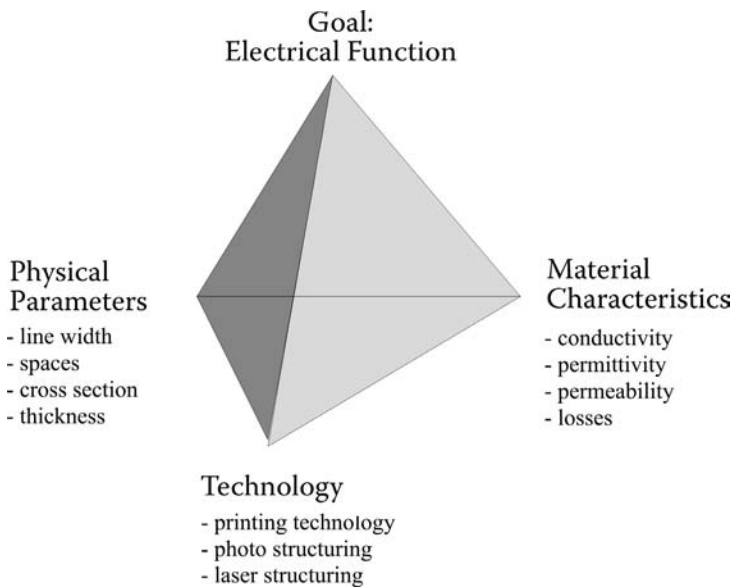
FIGURE 9.3
General correlation between material, technology, physical parameters, and the electrical function as the target.

Recent problems are mainly related to:

- Material incompatibility in the thermal coefficient of expansion
- Mismatched shrinkage during firing (especially, in LTCC technology)
- Interaction of two or more different materials on their common boundary

The desired electrical function or element is influenced by the following factors:

- Material properties (related to the chosen substrate/tape and ink system)
- Technology constraints (e.g., conductance and via resolution)
- Physical design topics such as line lengths or distances to other printed components or features (Figure 9.3 [4])

9.2.1 Resistors

Resistors are widely used in microelectronic circuits. To allow a broad range of applications, printed resistors should exhibit the following properties:

- Wide range of sheet resistivities
- Reproducible sheet resistivities

- Small or possibly zero temperature coefficient of resistance (TCR)
- Long-time stability of resistance and TCR
- High-power dissipation capability per area
- Stability against high voltage
- Low electrical noise

Depending on the resistor type, additional properties are desired. Surface resistors (fixed value) need to be stable against environmental impacts that may occur during circuit fabrication and assembly, as well as during circuit operation. Because of manufacturing tolerances, it should be possible to trim these components. Variable surface resistors like potentiometers must be mechanically stable even without a protective cover glass. Their surface must be conductive to allow the desired electrical contact. Cofire resistor pastes for buried LTCC resistors require a matched shrinkage to the tape and must be chemically compatible with the surrounding material. Usually, glasses in the resistors tend to interact with the tape glass, which leads to a shift in the ratio of resistive particles. This process causes different resistances per unit area as well as changes in their TCRs. Multiple refirings of the LTCC substrate should result in small or, at least, predictable resistance changes.

The first resistor ink system with a wide range of sheet resistivities was developed in 1958 by J. D'Andrea. This palladium and silver system (PdO/Ag) had a high firing temperature influence on the sheet resistivity, caused by the complicated chemical–dynamical process. The wide range of resistances that this composition could achieve was one main reason for the rapid growth of thick-film technology since then.

Today a much wider range of sheet resistivities, with smaller temperature coefficients and an increased stability due to the firing of the ink system based on RuO_2, BiO_2RuO_7, and $Pb_2Ru_2O_6$ or IrO is achieved.

Typical thick-film resistor (TFR) inks are composed of the following components:

- Ruthenium compound powder
- Additives (e.g., TCR modifier)
- Glass matrix
- Binder and solvents (to achieve printable inks)

For low RuO_2 concentrations, the particles are nearly fully separated, and the ink shows a high resistance. With the increase of the RuO_2 concentration, an increase in chain formations can be observed. With a 30% concentration of RuO_2, almost all particles touch one another, and the ink shows low resistance. In the sintering process, RuO_2 reacts with the glass and diffuses into the glass barriers that results in semiconductor characteristics, mainly hopping conductivity.
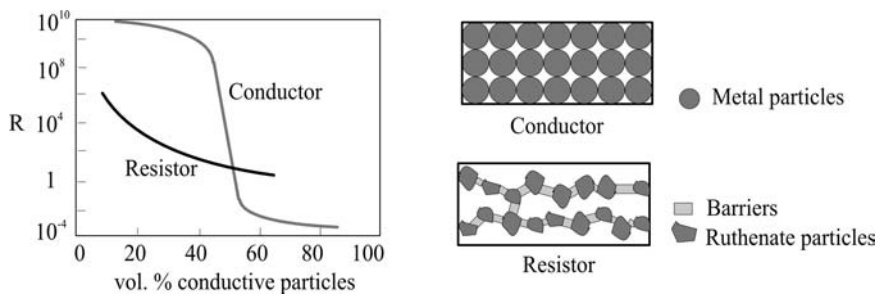
FIGURE 9.4
Different conduction mechanisms of thick-film conductors and resistors.

All models of resistor conduction mechanism are based on a network of conductive chains in the microstructure with segments of different couplings [5–7].

Conduction mechanisms are determined by:

- Metallic conduction
- Tunnel mechanisms and hopping conduction through glass barriers
- Direct tunnel conduction between metal oxide particles

Metallic conduction is only used in inks with very low resistances. The glass-barrier effect, explained by the other mechanisms, allows a broad range of sheet resistivities vs. the ratio volume of metal-oxide particles (Ruthenate — ruthenium compounds like RuO_2 or BiO_2RuO_7) to the glass matrix. With 6 to 60% of ruthenate, sheet resistivities between 1 mΩ/$\square$ and 10 Ω/$\square$ can be achieved (Figure 9.4).

Today, thick-film surface-processed resistors offer the following advantages:

- Tolerances of <0.5% in ranges from milliohms to megaohms
- TCR of <100 ppm/°C in the temperature range from –55 to 125°C
- TCR of <50 ppm/°C in the temperature range from 0 to 70°C
- Identical resistors can achieve a TCR tracking of 10 ppm/°C

Furthermore, surface resistors can be laser trimmed and thus enable cost-effective implementations for a variety of designs. On the other hand, buried resistors are available today with limited range of resistances from <100 Ω to over 100 kΩ with wider tolerances.

9.2.2 Capacitor Materials

Capacitor dielectrics for ceramic circuits are available as tapes and pastes. The latter are used for plate capacitors on both the surface (e.g., standard thick-film technology) and within a multilayer structure. Electrodes are made

of typical conductor materials. Gold and platinum are recommended by material suppliers. Silver or silver palladium may be applicable as well. In some designs, the material combination will be determined by other constraints. It is recommended that the compatibility be verified between dielectrics and conductor in these cases. Capacitor pastes or tapes used within an LTCC structure need to be matched to the shrinkage behavior of the LTCC (if free sintering is applied). Furthermore, the capacitor dielectrics must be chemically compatible to the glass of the LTCC to avoid a change of its dielectric properties and should be closely matched to the TCE of the LTCC ceramic tape to avoid stress-related cracks.

Materials that possess a high permittivity or dielectric constant are referred to as *high-K dielectrics*. They are usually based on ferroelectric materials (often bariumtitanate ($BaTiO_3$), barium–strontium–titanate, or mixtures with different curie temperatures). Ferroelectrics are insulating materials that keep a part of the polarization after applying a static electrical field to it (spontaneous polarization hysteresis). The permittivity of $BaTiO_3$ ferroelectrics can be in the range of 1000 to 4000 depending on the grain size [8]. At the curie temperature (around 120°C), the permittivity will reach its maximum. To reduce the temperature characteristics, curie temperature shifters and permittivity depressors are used. They both stabilize the temperature coefficient of capacitance (TCC) for the ambient temperature range of typical applications. However, the improved temperature behavior is paid at the expense of a lower permittivity. Controlling processing parameters are essential for the repeatability of the dielectric constant. In particular, the sintering temperature and the peak time have an important impact on the final capacitance value. Most high-K materials are not stable. They tend to exhibit reduced dielectric constants with time. The largest drop occurs shortly after the firing process. Because of the temperature sensitivity of the dielectrics, the capacitors' characteristics will follow X7R or worse.

Because sintering temperatures of the high-K materials are above 850°C, they do not really densify. They are more or less embedded in the glass matrix, which acts as a sinter aid. A high permittivity requires little low-K glass, thus being rather porous after firing under thick-film conditions. To prevent moisture from penetration into the dielectrics, the high-K structure must be sealed with another hermetic layer.

Lower- and medium-K values (ranging from 10 to 160) are achieved with nonferroelectric dielectric materials. Magnesium titanate or titaniumoxide are typical exponents. These dielectrics are not subject to a permittivity reduction over time and can be tailored to negative positive zero (NPO) characteristics.

9.2.3 Inductor Materials

Traditional inductors in thick-film technology are made of printed conductor patterns on the prefired ceramic or LTCC tape. The dielectric substrate

TABLE 9.1

Examples of Buried Coils and Ferrite Tapes in LTCC

Part Description	Inductance [μH]
Silver conductive spiral coil buried in LTCC	2.0
Silver conductive spiral coil with 2 layers ferrite tape[a] (one each side buried in LTCC)	3.5
Silver conductive spiral coil with 4 layers ferrite tape[a] (two each side buried in LTCC)	6.5

[a] Each layer about 60 μm thick.

Courtesy of ESL. With permission.

itself serves only as a carrier material without any contribution to the inductance value. Increasing the inductance is possible with materials having a permeability larger than one. Ferrites cast as cofired tape, compatible with the LTCC process (sinter profile, dielectric tape, conductor inks, and via-fill inks), allow an increase of the inductance value. Inductors can be entirely embedded in the ferrite.

NiZn ferrite is a suitable material due to its high resistivity and relatively simple processing [9,10]. The highest permeability (350) is obtained when the tape is fired at a temperature of more than 1000°C, which results in a large uniform grain structure. The use of silver-based conductors restricts firing temperatures to less than 950°C. Peak temperatures around 900°C decrease the permeability to around 200.

The examples described in Reference 9 and shown in Table 9.1, were made with a spiral buried between one and two layers of ferrite tape embedded between dielectric tape layers (Figure 9.5). The parts were fired at 875°C for 30 min with a heating rate of 10°C/min. The inductance can be increased with the number of tape layers. The tape can also be used to manufacture surface-mounted inductors and transformers [11].
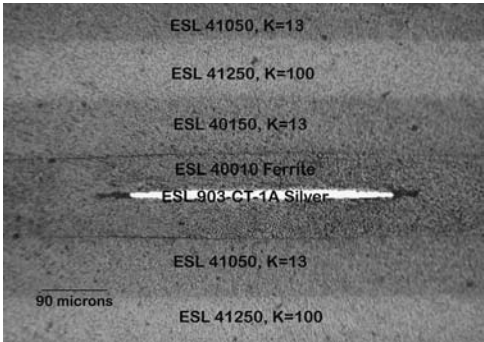
FIGURE 9.5
Examples of buried coils and transformer arrangement with ferrite tapes in LTCC. (Courtesy of ESL.)

1. Embossing tool adjustment

4b. Photo structuring (FODEL)

4a. Screen printing

2. Pressing under temperature

UV exposure

F, T

3. Separation

spray developing

embossed tape
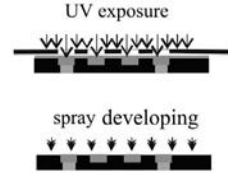
FIGURE 9.6
LTCC embossing process and ditch-filling technologies.

Conductive loss is often a limiting factor to achieve high-quality inductors. For some applications, a very high current-carrying capability is required. Both needs can only be met with a conductor thickness much higher than typically achieved by screen printing. However, the increase of the conductor thickness should not result in a decrease of the structuring accuracy.

Increased conductor thickness is possible through the formation of the conductor cross section by hot embossing of unfired LTCC tapes. Green LTCC tape shows plastic behavior, caused by the composite from glass–ceramics and organic binders. Between 50 and 90°C, the tape will be soft and has the ability to flow during an embossing process under pressure. After the embossing, the ditches or canals must be filled with conductor ink (Figure 9.6). During the following lamination, the ingrained conductors will not deform, unlike printed or photostructured conductors.

The embossing process uses already established methods of microsystem technology (MST) [12] in combination with LTCC technology. It allows the manufacture of multilayer conductors with a high ratio of conductor height to width. The advantage compared to other structuring methods such as laser cutting [13] or etching with acetone [14] is a very high structure resolution. Embossing is a parallel process (the full structure of a layer is processed in one step) and is compatible with the LTCC process.

Hot embossing uses the plastic flow rating of unfired LTCC tape. An inverse profile of the desired conductor profile (embossing tool) is used to form the tape under pressure and temperature [15]. In Reference 16, tools that are formed with a special two-step etching process are used (Figure 9.7). Step one is the anisotropic plasma etching followed by an Advanced Silicon Etching (ASE®) process with an inductive-coupled plasma (STS-ICP-ASE®). A low-cost method based on printed circuit board (PCB) is also possible.

An example of an embossed structure in LTCC is shown in Figure 9.8. Two methods of ditch filling have been demonstrated. Ditches up to a depth of 100 μm can be filled by simple multiple-pass screen printing. The second method is based on photostructuring of pastes. Photostructuring offers excel-
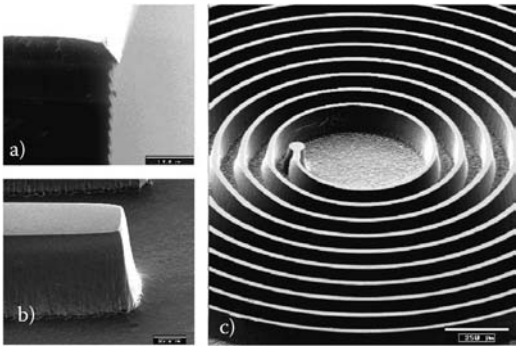
FIGURE 9.7
Picture of an Si-embossing tool and details: (a) after anisotropic plasma etching, (b) after STS-ICP-ASE®, (c) complete tool. (From Albrecht, A. et al., Alternative ways to high current structures in LTCC, *Proceedings of the 14th IMAPS-EMPC Conference*, Friedrichshafen, Germany, 2003, pp. 408–411. With permission.)
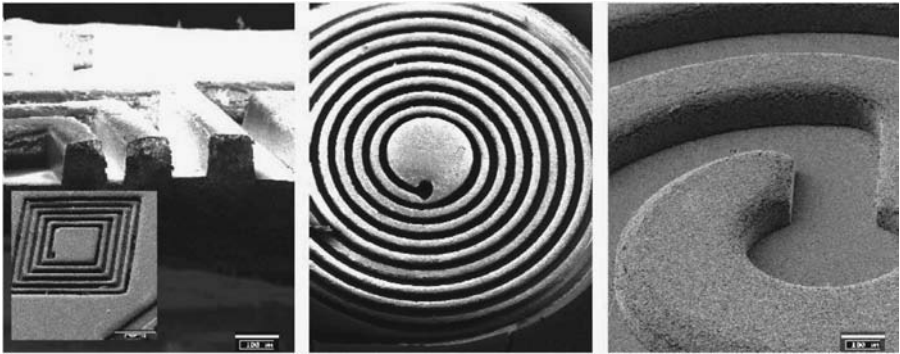
FIGURE 9.8
Embossed structure in LTCC tapes.

lent resolution and a superior edge quality. Although, only a thin layer is exposed, the unexposed paste in the ditches is protected against developing by the polymerized layer (Figure 9.9). Figure 9.10 shows an example of a silver-filled spiral inductor. The area resistance could be reduced to about 0.6 mΩ/($\square$).

9.3 Design of Lumped Elements

Lumped-element design, in general, is little supported by conventional computer aided design (CAD) systems. Passive integration is usually limited to resistor design. Reasons for this are that the high-frequency-component
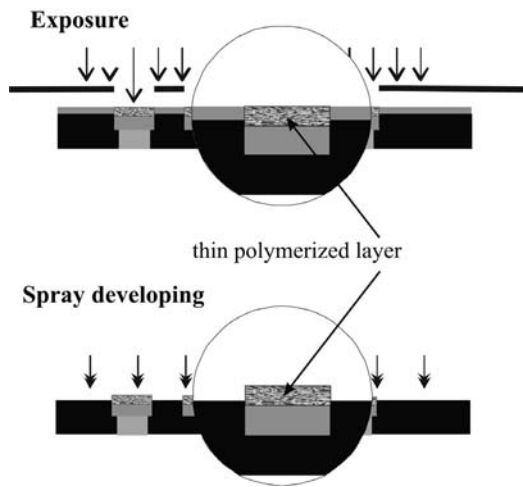
FIGURE 9.9
Photostructuring of filled ditches.
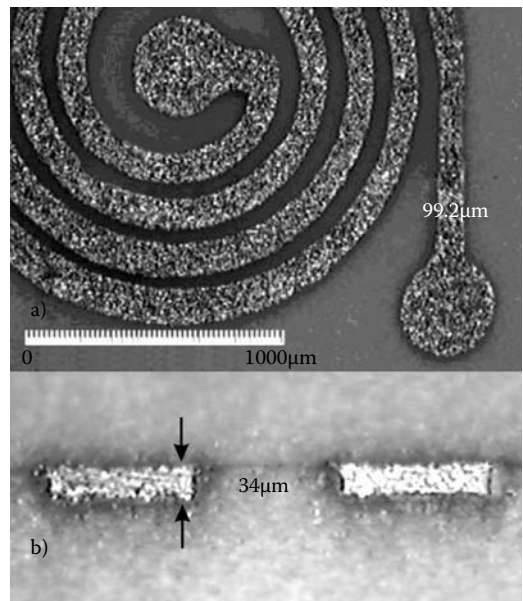
FIGURE 9.10
Ag-paste-filled coil structure: (a) top view, (b) cross section.

properties are difficult to determine because they are influenced by the surrounding layout. Depending on the element type, one or several of the following approaches can be applied:

- Closed form equations (capacitors and resistors)
- Semiempirical formulas (inductors, e.g., Reference 17)
- 3D-EM-field simulations
- Database (library with S-parameters of known standardized components)

The most difficult element to design is the printed inductor. A variety of semiempirical equations is available for the different shapes. These are typically based on the practical try-and-measure method. However, the wide-band-frequency behavior of inductors is difficult to predict [18]. It is heavily influenced by inherent parasitics and adjacent component interactions. In most cases, electromagnetic field simulations are used for fine-tuning and verification of the design.

9.3.1 Design of Resistors

Resistor inks are available in a broad range of sheet resistivities (1 Ω/□ to more than 10 mΩ/□). The sheet resistivity is derived from the paste bulk resistance normalized to a certain thickness (e.g., 25 μm dried thickness). Therefore, TFRs are determined by their width-to-length ratio and the characteristics of the paste applied (Equation 9.1). Figure 9.11 shows a typical rectangular TFR design.

$$R = \rho \cdot \frac{l}{A} = \rho \cdot \frac{l}{h \cdot w} = R_{sq} \cdot \frac{l}{w} \tag{9.1}$$

where l, w, and h denote the resistor length, width, and thickness, respectively, R_{sq} is the sheet resistance in Ω/□, R is the resistance value in Ω, and l/w denotes the aspect ratio in squares □.

A typical resistor consists of resistive material and two terminations made of a high-conductive material. Extreme aspect ratios should be avoided. These ratios are confined in the range provided by Equation 9.2:
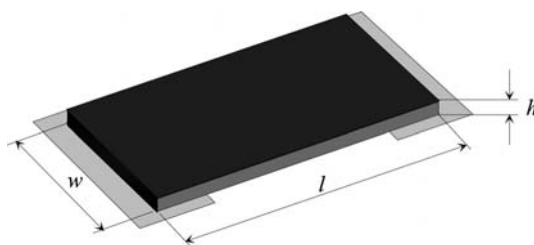
FIGURE 9.11
Rectangular resistor dimensions.

$$0.5 \leq {}^l/_w \leq 5. \tag{9.2}$$

Thick-film resistors can be processed with a tolerance of about ±25%. Laser trimming increases the resistance value. Therefore, a resistor is designed to a lower value than desired and will be trimmed to its target value later on. Besides the resistance value required, the power dissipation density is required to design a thick-film resistor. The power dissipation density ($P_{density}$ in mW/mm²) is a paste property, which is specified in the data sheet. It is typically related to a 50% trim cut (maximum allowable trim length) and application on prefired alumina. For a stable resistor, the minimum area A_R is determined by the maximum circuit power dissipation requirement, as in Equation 9.3:

$$A_R \geq \frac{P_{max}}{P_{density}}. \tag{9.3}$$

Using the area, Equation 9.1 takes the form of Equation 9.4:

$$R = R_{sq} \cdot \frac{A_R}{w^2}. \tag{9.4}$$

The width w and the length l of the resistor are calculated using these equations:

$$w = \sqrt{\frac{R_{sq}}{R} \cdot A_R} \tag{9.5}$$

$$l = w \cdot \frac{R}{R_{sq}}. \tag{9.6}$$

An example of a design is given in Reference 19. Hat-resistor designs are used in circuits requiring extreme trim ranges. An advantage of this resistor type is the nearly linear trim sensitivity in the hat region (Figure 9.12).

The base of a hat resistor can be considered as a rectangular resistor. The hat has minor influence on the untrimmed resistor. Therefore, the base resistor is designed according to the required start value of the trim range. The maximum resistance value of the hat is achieved when the resistor is cut in two halves (Equation 9.7):

$$R_{max} = \frac{2 \cdot l_H}{0.5 \cdot w_H} \cdot R_{sq} = 4 \cdot R_{sq} \cdot \frac{l_H}{w_H}. \tag{9.7}$$
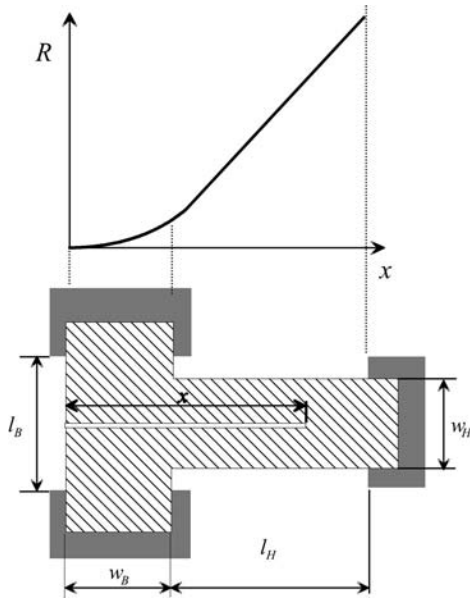
FIGURE 9.12
Trimming behavior and dimensions of a hat resistor.

The hat length is determined by the trim range R, as shown in Equation 9.8:

$$l_H = \frac{\Delta R \cdot w_H}{4 \cdot R_{sq}} = \frac{R_{max} \cdot w_H}{4 \cdot R_{sq}} \tag{9.8}$$

Hat resistors are not useful for radio-frequency designs because of self-resonance effects. In the process chain, thick-film resistors are always fired in the last 850°C sintering cycle to avoid resistance changes due to refirings.

In LTCC technology, resistors are available as cofire or postfire resistors. The latter can be considered as typical thick-film resistors. Cofire resistors may be on the substrate surface or embedded in the tape. The possibility to integrate resistors in inner layers of LTCC has been known for years. Still today, there is little experience to manufacture them with the same performance as postfire resistors. Material interactions with LTCC contents, firing conditions (air vs. covered), and shrinkage are some of the reasons. Base materials and processing parameters are usually well defined and qualified for the LTCC process. Therefore, it is necessary to find resistor pastes that fit into these boundary conditions. Another aspect is related to the postprocessing of LTCC circuits. Whereas postfire resistors are fired in the last 850°C step, cofired resistors see further high-temperature cycles. It is important to understand the resistance-shift behavior to establish design rules. Typically, the designs are based on the experimental approach. The mentioned tolerances for standard thick-film resistors will apply as well. Buried resistors are

mainly used in applications not requiring tight tolerances. Possible ways to adjust embedded resistors to get lower tolerances are described in Section 9.4.

9.3.2   Design of Capacitors

Two categories of capacitors are available in ceramic technology. The planar or interdigital capacitor (Figure 9.13) can be printed on the surface or inside a ceramic package. The second type is the plate capacitor that consists of two or more electrodes with dielectrics in between (Figure 9.14).

9.3.2.1   *Interdigital Capacitors*

The capacitance is determined by the bulk permittivity, the spacing s between the fingers and the finger length l (Figure 9.13). This type is suitable for values from 0.05 to 1 pF with reasonable dimensions and can be used for DC blocking on microwave signal lines. The simplest interdigital capacitor consists of two parallel lines. The size is limited by the printing accuracy of the gaps. Lines and spaces as small as 50 µm were achieved (Figure 9.15). Smaller spacings can be achieved by laser ablation, etching, or photo-defined

l - *length*
w - *width*
s - *space*
h - *distance to ground*

N - *number of segments*
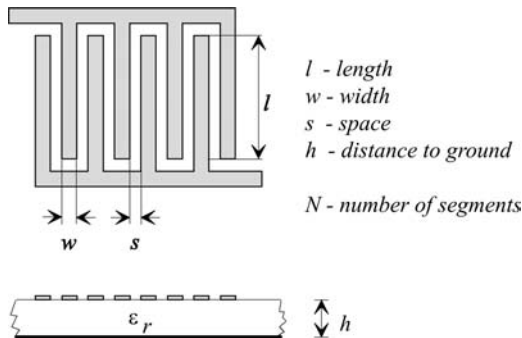
FIGURE 9.13
Interdigital capacitor.
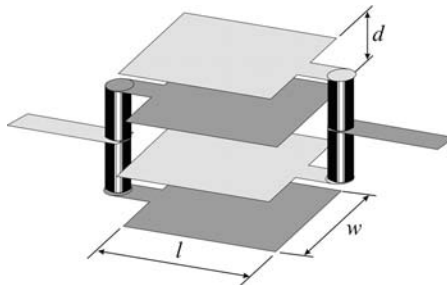
FIGURE 9.14
Plate capacitor.
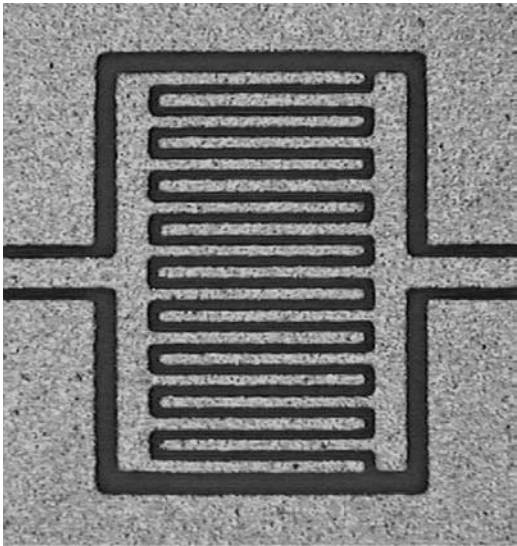
FIGURE 9.15
Printed interdigital capacitor with 50-μm lines and spaces. (Courtesy of Micro Systems Engineering GmbH & Co., Germany.)
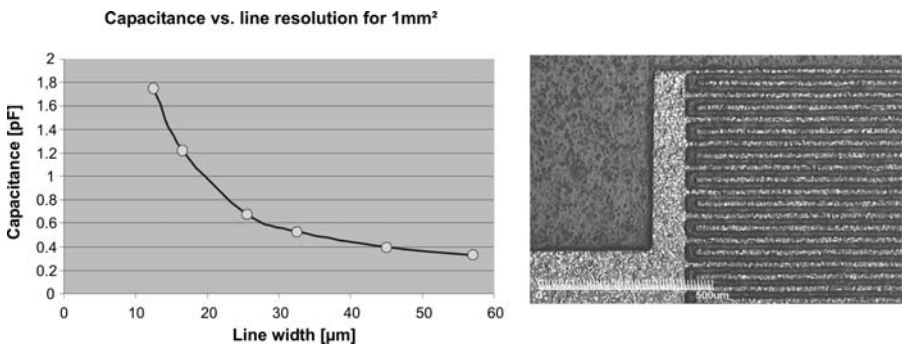
FIGURE 9.16
Capacitance density for interdigital capacitors in Fodel®-Technology.

pastes. The graph in Figure 9.16 shows the relation between line resolution and capacitance density of a 1-mm² finger capacitor.

Interdigital capacitors offer high-quality factors because dielectric losses of the substrate and the surrounding air (if printed on the surface) are very low. Conductor losses mainly contribute to the overall loss.

Typical interdigital capacitors are designed with equal spacings and line widths. They can be calculated using Equation 9.9 [20]:

$$C\left[pF\right]=\left(N-1\right)\cdot l\cdot 5.66pF \ / \ m\cdot\left(\varepsilon_{r1}+\varepsilon_{r2}\right) \tag{9.9}$$

where

ε_{r1} = relative dielectric constant of the substrate
ε_{r2} = relative dielectric constant of a thick cover layer ($>s$, $\varepsilon_{r2} = 1$ for air)

For standard alumina (permittivity ≈ 10), Equation 9.10 was developed [6]:

$$C = K_c \cdot (N - 1) \cdot l \cdot \frac{w}{w + s} \tag{9.10}$$

with $K_c = 1.1 - 1.2\ pF/cm$.

9.3.2.2 Plate Capacitors

Higher capacitance values are obtained with plate capacitors. The capacitance depends on the material permittivity, its thickness, and the plate area (Figure 9.14). If we omit the inhomogenities of the electrical field at the plate edges (fringing field [21]) the capacitance can be determined by Equation 9.11:

$$C = \varepsilon_r \cdot \varepsilon_0 \cdot \frac{A}{d} \cdot (n - 1) \tag{9.11}$$

where d is the distance between the plates, n is the number of plates, and A is the area of the plates.

Using standard alumina, the substrate itself can be used as the capacitor dielectrics. However, because of the considerable thickness of substrates (250 μm or more) and the relatively low permittivity of about 10, the capacitance density is very low (e.g., 0.34 pF/mm² @ $d = 250$ μm).

Larger capacitance values are obtained with high-K dielectrics in a multilayer printing technique. At least six printing and firing steps are required to build up a high-K capacitor in thick-film technology (Figure 9.17). The
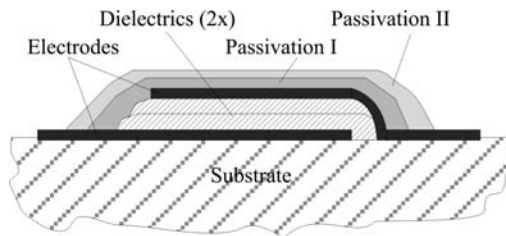
FIGURE 9.17
Cross-sectional view of a printed high-K capacitor.

double-layer system of passivation is necessary to seal the capacitor to prevent moisture penetration. Cost, tolerance, and size for these elements cannot compete with surface-mounted capacitors.

LTCC plate capacitors can achieve very good quality factors and NPO characteristics. The dielectric losses in the tape are small, and silver electrodes offer superior conductivity. Therefore, these capacitors are suitable for RF filters with high selectivity. Tolerances are mainly caused by tape-thickness variations and layer-to-layer alignment accuracy. The latter can be compensated by design. Combinations of different plate sizes (larger plate opposite to a smaller one) reduce the amount of fringing-field-related deviations [22]. Typical LTCC vendor thickness tolerances are specified below ±7% [23] to account for lot-to-lot variations. Within one manufacturing lot (with a considerable amount of tape), thickness tolerances are more in the range of less than ±2%. If high-volume production is to be considered, a tighter customer specific lot-to-lot tolerance needs to be agreed with the material supplier. With a typical fired tape thickness of about 95 μm per layer, a capacitance density of approximately 0.73 pF/mm² is achievable. To improve the capacitance efficiency, the following methods (a–d) can be applied:

a. Adding of layers and reducing tape thickness (Figure 9.18a)
b. Insertion of one layer of high-K tape (Figure 9.18b)
c. Filling of holes with high-K material (Figure 9.18c)
d. Locally printing high-K paste (Figure 9.18d)

Multilayer capacitors can be easily realized in LTCC technology. The suitable range lies between 0.4 pF and 5 pF. Of course, larger capacitances are possible by extending the plate size and the number of electrodes. But this approach is not size- and cost-effective. To achieve a high capacitance density, the dielectric thickness of a plate capacitor should be as thin as possible, and the permittivity of the dielectrics should be as high as possible. These requirements are difficult to achieve with the tapes available having a permittivity of about 8. Though thinner tapes have become available, there are limits in the manufacturability due to the incompatibility with the installed tape-handling systems.
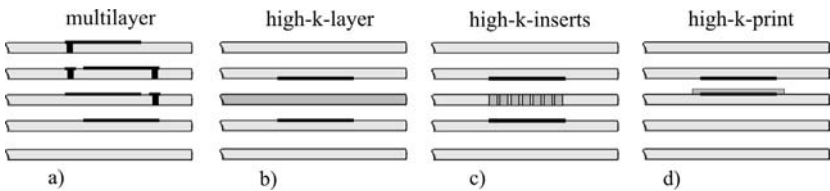
FIGURE 9.18
Methods to increase the capacitance density with high-K materials in LTCC: (a) multilayer, (b) high-K layer, (c) high-K inserts (paste or tape), (d) high-K print with paste.

Inserting an entire tape layer of high-K material requires a tape that should meet the following requirements:

- Matched shrinkage to base tape during firing
- Tape sinters hermetically to avoid moisture penetration into the package (sufficient densification)
- Matched TCE to base tape
- No material interactions with the base tape dielectrics (both ways)
- Compatibility to conductor and via-paste systems
- Compatibility to general tape-processing methods (handling, etc.)

High-K tapes with unmatched shrinkage can be used if constraint sintering is applied to the substrate [24]. The high-K material should be symmetrically inserted in the layer stack to avoid distortion and warping. Because most high-K materials do not fully densify during the LTCC firing cycle, the edges of the substrate are moisture-sensitive. Tapes compatible with a variety of tape systems, with permittivities ranging from 50 to about 250, have been introduced recently [25].

A solution to locally inserted high-K material has been introduced earlier [26]. This so-called tape insert array method eliminates some of the requirements mentioned in the preceding text. However, the processing method is rather complex and was therefore not introduced into series production. The most promising and cost-effective method considered is type d [27]. The electrodes are printed on the top of the first tape and on the rear side of the second layer. A high-K paste is printed over the first electrode twice for isolating electrode one from electrode two in the layer stack. Electrical connections to both electrodes can be realized by vias placed directly in the center of the plates or by conductor traces leaving the electrodes within the plane (Figure 9.19).

The printing solution addresses both variables in the capacitor design. The thickness of the dielectrics is minimized, and the permittivity is increased simultaneously. The high-K paste has to have the following features:

- Matched shrinkage to tape during sintering
- Pin-hole-free printability

a)   b)
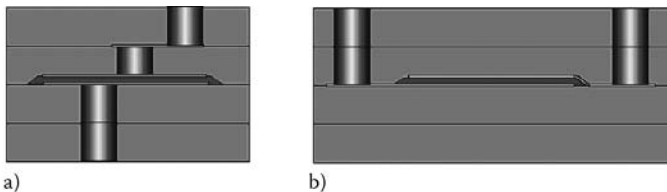
FIGURE 9.19
Contact solutions for plate capacitors: (a) central, (b) peripheral.
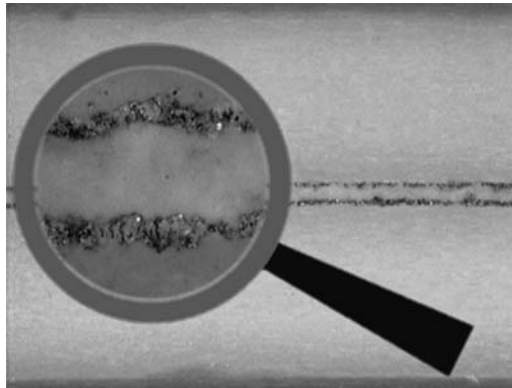
FIGURE 9.20
LTCC high-K capacitor with printed dielectric layer.

- Controlled thickness (for low-capacitance variations)
- Compatible with electrode and via materials
- Stability to refirings

Furthermore, the whole capacitor should not lead to a remarkable topology on the LTCC surface after firing. This method should, therefore, not be applied on tapes thinner than 130 µm or on tapes with a low compressibility. Warping of the circuit due to a slight mismatch of the shrinkage or the TCE can be prevented by always arranging the capacitors symmetrically in the package. Because the LTCC seals the buried capacitor hermetically, it is not sensitive to humidity. Results of the evaluation of a high-K paste are given in Reference 28. About 20 pF/mm^2 were achieved with a printed thickness of approximately 25 µm (Figure 9.20). Refirings showed little impact on the capacitance (Figure 9.21). Because of variations in the printing process, only a tolerance of ±15% is possible. These capacitors are not suitable for RF filtering but can be used for decoupling purposes.

9.3.3 Design of Inductors

Inductors can be designed in multiple shapes. They mainly consist of conductor traces arranged in such a way as to allow a common oriented magnetic field, so that the overall inductance is increased. Because of this field effect, inductors are susceptible to ambient influences caused by neighboring components and other electrical structures (especially, ground planes). Therefore, these influences are to be considered in every inductor design (see, Section 9.6). Thick-film technology allows inductor values from one nanohenry to several microhenries whereas the upper limit is mainly determined by the circuit area available. Printed inductors can be divided into planar and three-dimensional structures.
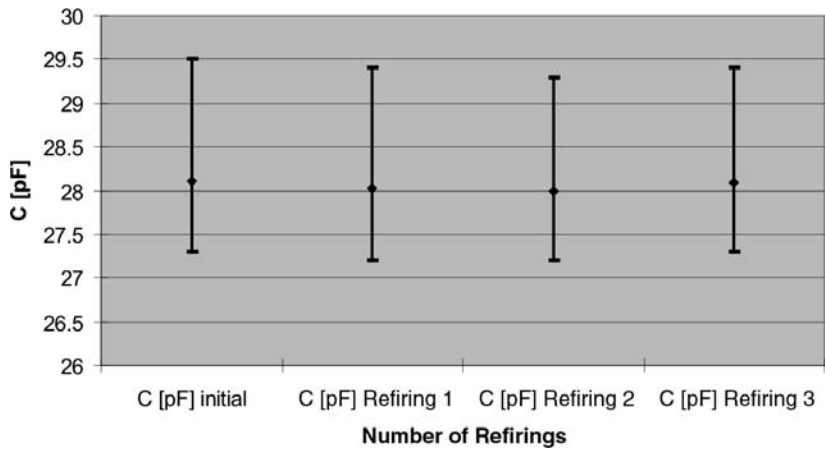
FIGURE 9.21
Refiring stability of LTCC high-K capacitors (shown are minimum, maximum, and mean values).

9.3.3.1 Planar Inductors

Planar inductors are suited for both thick-film, thin-film, and LTCC applications. Typical members of this group are meander and spiral inductors (Figure 9.22). Meander inductors offer the lowest inductance vs. size. Their inductance value is determined by the length and the unit line inductance. Because of the adverse magnetic-field orientation of adjacent line segments, there is no increase of the overall inductance [6]. The inductance is directly proportional to the meander length. Meander inductors are usually used for low inductances and delay lines. Because the meander is more or less a transmission line, the distributed character is dominating in most cases.

Spiral coils (circular or rectangular) provide higher inductance/area. In general, the inductance is dependent on line width, line spacing, number of turns, and inner-window size (Figure 9.23). The inductance density is mainly determined by the conductor line resolution. Figure 9.24 depicts the relation between line resolution and inductance for an area of 6 mm². Many of the design formulas available in literature are parametric equations based on
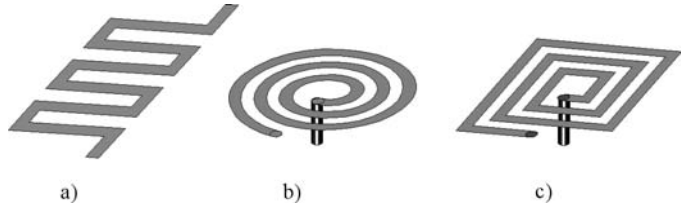
FIGURE 9.22
Planar inductor shapes: (a) meander, (b) circular spiral, (c) rectangular spiral.
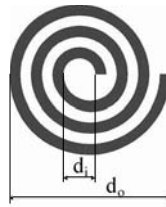
FIGURE 9.23
Inductor parameters for Equation 9.12.
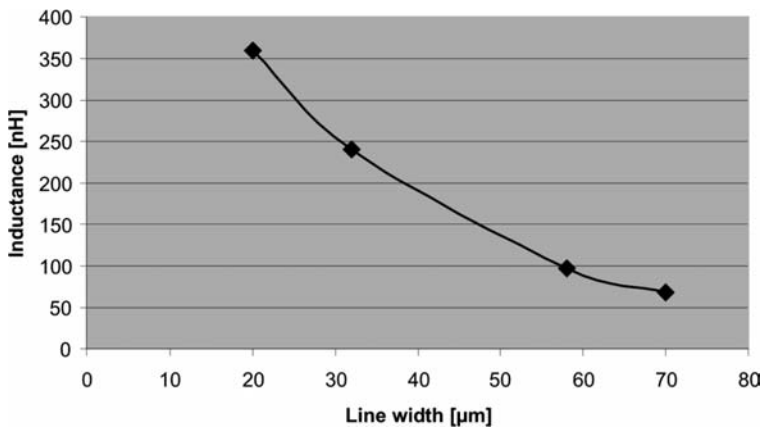
FIGURE 9.24
Inductance value vs. line resolution for rectangular spiral coils with 6 mm² area.

measurements and interpolation. They are valid for defined boundary conditions only. One example is Equation 9.12, developed by Burkett [29].

$$L[nH] = \frac{0.8a^2n^2}{6a + 10c}$$

$$a = \frac{d_o + d_i}{4}; \quad c = \frac{d_o - d_i}{2}$$

(9.12)

n = number of turns; d_o, d_i in mil.

The equation was developed for inductors on 15-mil ceramic substrates with a ground plane. For other boundary conditions, it can only provide a rough estimation.

Remke and Burdick [31] derived a closed-form equation based on the inductances of circles. Circular spiral coils are divided in several circles with mean (turn) diameters. The overall inductance is calculated as the sum of

all mutual inductances (each circle to all remaining) and external self-inductance of each circle (Equation 9.13). The inner self-inductance is neglected because it will be reduced with higher frequencies by the skin effect.

$$L_{spiral} = M_{total} + L_{external} \tag{9.13}$$

with M_{total} being the mutual inductance and $L_{external}$ the external self-inductance.

$$M_{total} = 2 \cdot \sum_{k=1}^{n-1} \sum_{j=k+1}^{n} \mu_0 \sqrt{ab} \left[\left(\frac{2}{k_1} - k_1 \right) K(k_1) - \frac{2}{k_1} E(k_1) \right] \tag{9.14}$$

with: $k_1 = \dfrac{\sqrt{4ab}}{a+b}$, $a = r_0 + (k - 0.5)(w + s)$, $b = r_0 + (j - 0.5)(w + s)$

where
  r_0 = radius of the first winding
  w = conductor line width
  s = spacing between conductors

The elliptical integrals of first and second order are:

$$K(k_1) = \int_0^{\pi/2} \frac{d\phi}{\sqrt{1 - k_1^2 \sin^2 \phi}}, \quad E(k_1) = \int_0^{\pi/2} \sqrt{1 - k_1^2 \sin^2 \phi}\, d\phi.$$

Both integrals can be solved numerically. Routines for this purpose are included in standard math tools.

Calculation of the external self-inductance is based on the method of selected mutual inductances. The mutual inductance of two circular current paths (zero line width) with the spacing w (coil line width) and the mean radius c is equal to the external self-inductance of a conductor circle with same dimensions (Figure 9.25). For n turns, it is of the form,
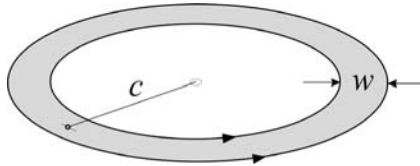
FIGURE 9.25
Method of selected mutual inductances.
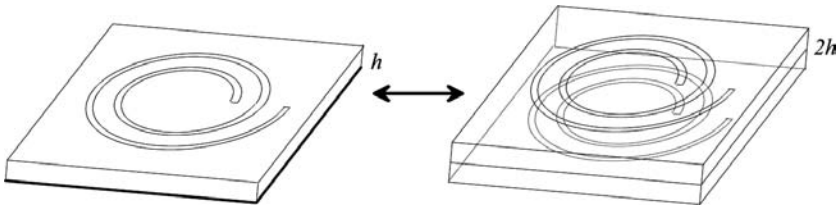
FIGURE 9.26
Model of the current image method for inductors with ground planes [31].

$$L_{external} = \sum_{k=1}^{n} \mu_0 \left(2c - w_1\right) \left[\left(1 - \frac{k_2^2}{2}\right) K\left(k_2\right) - E\left(k_2\right) \right] \tag{9.15}$$

with: $k_2 = \dfrac{\sqrt{4c\left(c - w_1\right)}}{2c - w_1}$, $w_1 = \dfrac{w}{2}$, $c = r_0 + \left(k - 0.5\right)\left(w + s\right)$.

Ground planes under spiral coils reduce the inductance values. This effect is taken into account by applying the image-current method (Figure 9.26). A second coil with identical dimensions but opposite current flow is located under the spiral inductor with a spacing of twice the ground–plane distance *h*. The full set of equations can be found in Reference 31.

Planar circular inductors are considered ground less if their distance to the adjacent ground plane is larger than the inner diameter of the coil [32].

The inductance of rectangular spiral inductors is about 20% higher compared to the circular inductor with the same dimensions whereas the quality factor is higher for circular inductors.

Coil designs are usually not optimized for line width and, subsequently, smallest outline, because their quality factor is influenced by the line width, adversely. On the other hand, wide lines cause high parasitic capacitances, thus, reducing the self-resonance frequency. In particular, the crossing conductor has a major impact. The lowest stray capacitance is achieved by a high wire-bond loop (Figure 9.27). Countless design combinations are available for each inductor. It has to be decided which coil parameter, besides the
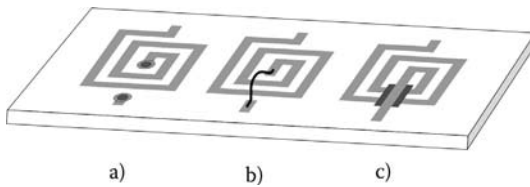
FIGURE 9.27
Interconnection methods for spiral coils: (a) through-hole vias, (b) wire bond, (c) crossing technique.
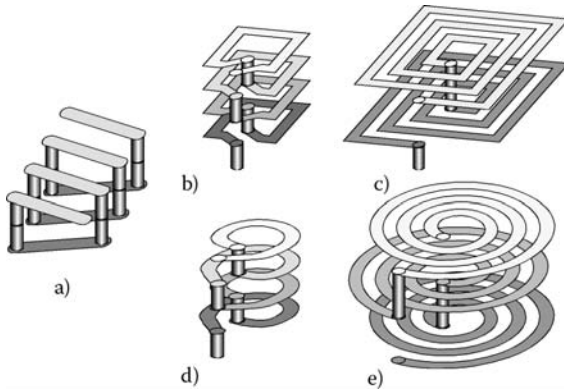
FIGURE 9.28
LTCC inductor shapes: (a) horizontal solenoid, (b) vertical solenoid, (c) sandwich inductor, (d) vertical solenoid, (e) sandwich inductor.

inductivity required, matters most (size, quality, and self-resonance frequency). Verification of these design parameters by simulation tools is recommended to avoid multiple design cycles.

9.3.3.2   3-D-LTCC Inductors

LTCC provides several options to design inductors using the third dimension. Figure 9.28 shows some examples. Coils with a helical shape can be arranged vertically (Figure 9.28a) or horizontally (Figure 9.28b and Figure 9.28d) in a layer stack. If combined on a substrate, the mutual influence of the magnetic field is low because the field lines are concentrated in perpendicular directions. The combination of spiral inductors with the helix shape results in a sandwich inductor (Figure 9.28c and Figure 9.28e). Very high inductances can be realized with this coil.

Closed-form equations for designing these inductors are not available. However, several parametric equations are known for wire-wound solenoids (Figure 9.29). One equation is provided in Reference 33 of the form:

$$L[nH] = \frac{22n^2 \cdot D[cm]}{\left(1 + 2.2 \cdot \dfrac{l}{D}\right)} . \tag{9.16}$$

In typical LTCC applications, the semiempirical expression for short coils ($D > l$) will apply [34].

$$L[nH] = 6,28n^2 D[cm] \cdot \left\{ \ln\left(\frac{4D}{l}\right) - 0.5 \right\} . \tag{9.17}$$
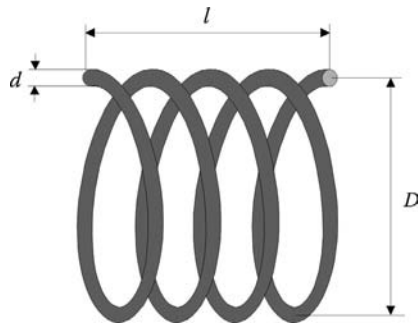
FIGURE 9.29
Dimensions for a solenoid.

n = number of turns
l = (n-1)x t   t = tape thickness
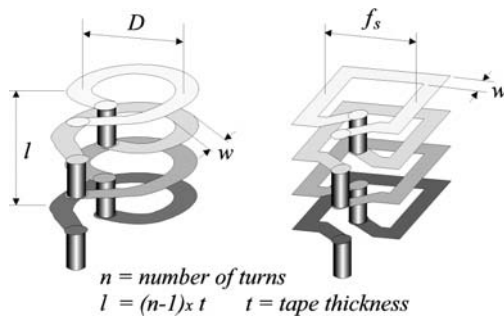
FIGURE 9.30
LTCC solenoid coil parameters.

The equations are valid for a small wire diameter in comparison to the coil diameter ($d \ll D$). For LTCC solenoid coils, the line width w needs to be considered. It reduces the diameter by w (Figure 9.30).

Using the tape thickness t, Equation 9.17 becomes,

$$L[nH] = 6,28n^2 (D-w)[cm] \cdot \left\{ \ln\left(\frac{4(D-w)}{(n-1)t}\right) - 0.5 \right\}. \qquad (9.18)$$

Including the form factor of 1.2, the inductance of rectangular coils can be calculated as follows:

$$L[nH] = 7,54n^2 (f_s - w)[cm] \cdot \left\{ \ln\left(\frac{4(f_s - w)}{(n-1)t}\right) - 0.5 \right\}. \qquad (9.19)$$
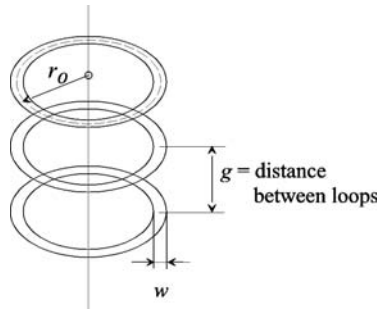
FIGURE 9.31
Model for the method based on Reference 31.

Results of this equation are in good agreement to measured values at low frequencies. At higher frequencies (> 10 MHz), the inductance value becomes smaller.

Alternatively, the concept of Remke and Burdick [31] can be applied to determine the inductance of solenoid LTCC inductors.

The mutual inductance between all circular loops according to Figure 9.31 becomes:

$$M = 2 \sum_{i=1}^{n-1} \sum_{j=k+1}^{n} \mu_0 \cdot r_0 \left[\left(\frac{2}{k_4} - k_4 \right) \cdot K(k_4) - \frac{2}{k_4} \cdot E(k_4) \right] \qquad (9.20)$$

with $k_4 = \dfrac{2r_0}{\sqrt{g_{ij}^2 + 4r_0^2}}$ and $g_{ij} = g \cdot (j - i)$ (distance of loops).

The expression for the external self-inductance of all loops is simplified to the following:

$$L_{external} = n \cdot \mu_0 \left(2r_0 - \frac{w}{2} \right) \left[\left(1 - \frac{k_5^2}{2} \right) K(k_5) - E(k_5) \right]$$

$$k_5 = \frac{2 \cdot \sqrt{r_0 \left(r_0 - \dfrac{w}{2} \right)}}{2r_0 - \dfrac{w}{2}}. \qquad (9.21)$$

The existence of a ground plane reduces the inductance values of three-dimensional inductors as well. This can be verified by measurements [35]. Figure 9.32 shows the inductance vs. height-above-ground for a rectangular
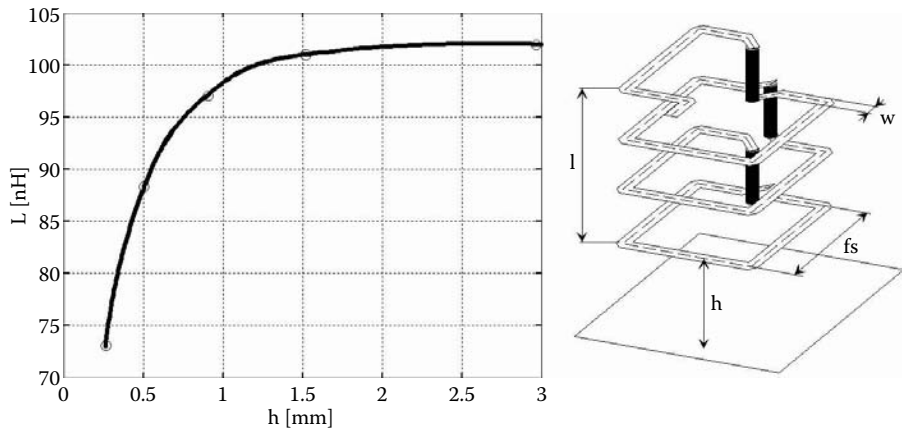
FIGURE 9.32
Inductance vs. distance-to-ground for a three-dimensional inductor (parameters: $n = 4.5$; $w = 400\ \mu m$; $f_s = 3.5$ mm) measured at 30 MHz.

solenoid coil. It is assumed that the ground plane impact vanishes if the distance-to-ground becomes larger than the inner diameter of the coil.

The windings of solenoid coils are typically stacked above each other. The wider the line, the higher is the parasitic capacitance between windings and the lower is the self-resonance frequency. Alternative solutions are shown in Figure 9.33. If sufficient space is available in the layout, windings can be designed with an offset in location or diameter [36]. Half windings in each layer not only increase the distance between turns, but also increase the number of layers. Sandwich coils as shown in Figure 9.28c and Figure 9.28e are made of spiral inductors in several layers. Very high inductance value/ area can be achieved. To determine the inductance of this coil type, the
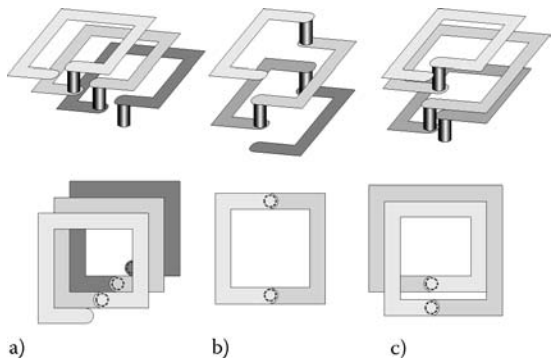
FIGURE 9.33
Design options to reduce the interlayer capacitance of solenoid coils.
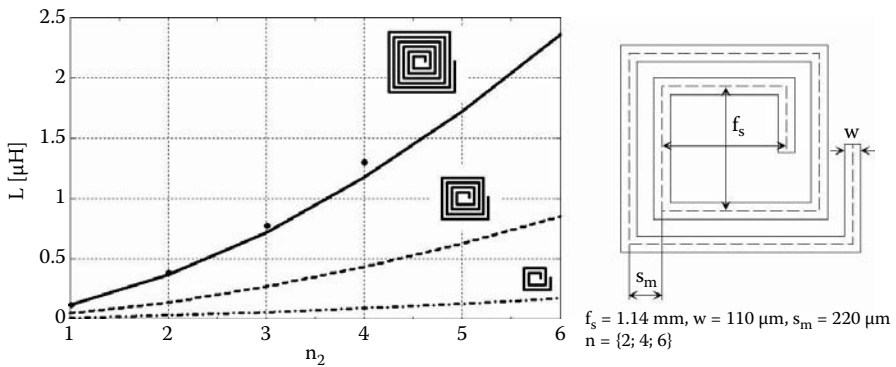
FIGURE 9.34
Calculated and (·) measured inductance values for rectangular spiral inductors vs. number of layers @ 1MHz.

approach from Remke and Burdick [31] can be adapted once again. The full mathematics is given in Reference 35. Figure 9.34 depicts results of calculation and measurement for rectangular sandwich coils.

9.4 Trimming of Lumped Elements

9.4.1 Resistor Trimming

As mentioned earlier, printed resistors can be produced with a limited accuracy of ±(20–25%) only. The variation in these tolerances is attributed to the paste properties and the processing conditions. A lot of applications require much tighter tolerances. Therefore, the fired resistors need to be trimmed to the required value [8,37,38].

9.4.1.1 Collective Resistor Trimming

With collective trimming, all elements of a circuit will be changed, e.g., by multiple-firing conductors and resistors. Examples of resistors of the DuPont 2000 series are shown in Figure 9.35 and Figure 9.36 [37]. Changing of sinter parameters during the process is unusual in production; however, postfiring is often used in practice. Both the resistance value and the TCE are changed with thermal treatment.

9.4.1.2 Trimming of Single Resistors

The most-used method for single-element trimming is made by mechanical changing of the resistor area. In this process, a contact is made to the resistor, and the element is measured during trimming. The resistance change is
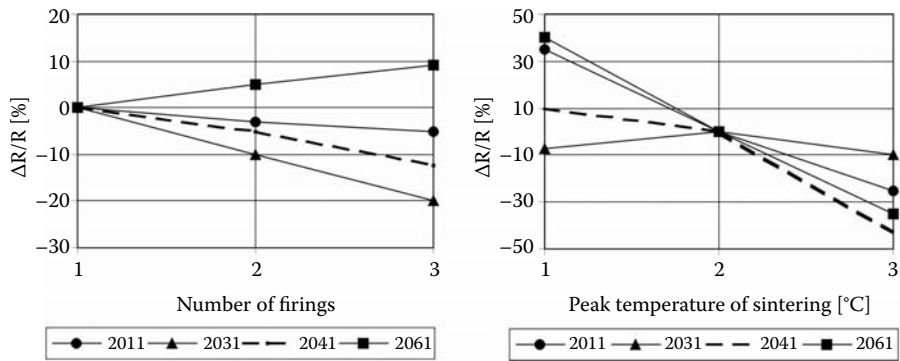
FIGURE 9.35
(a) Change of sheet resistance vs. number of firings and (b) change of sheet resistance vs. peak temperature of firing (resistor inks from DuPont 2000 series).
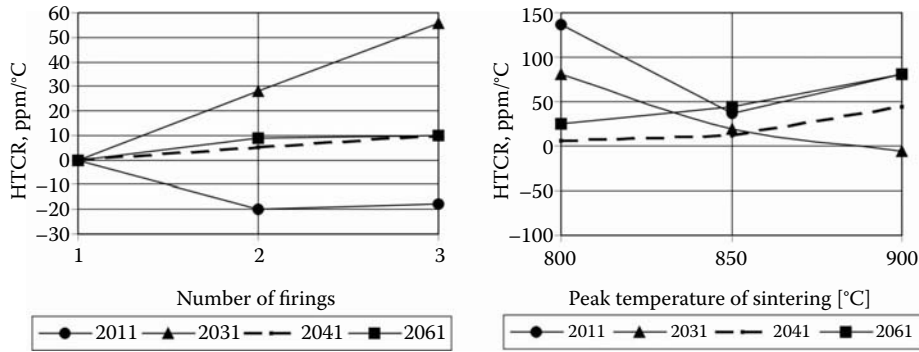
FIGURE 9.36
(a) Hot temperature coefficient of resistance (HTCR) vs. number of firings, and (b) hot temperature coefficient of resistance (HTCR) vs. peak temperature of firing.

obtained by reducing the cross section of the resistor, resulting in uptrimming. Resistors are designed to about 70–80% of the target value to allow for uptrimming. The process is made by laser cutting with a Nd:YAG laser (typical method) or sandblasting (traditional method). The latter is seldom used today. Al_2O_3 or SiO powder is blown by nozzles with diameters of 0.2–0.5 mm on the resistor surface to remove material. Such mechanical systems are slow, and the accuracy of the end value is limited (>1%). Sandblasting is applied in RF applications or on high-voltage resistors because the wider cuts show lower parasitic effects.

The mentioned methods are not applicable if the elements are buried deep in the circuit (multilayer or LTCC). Alternatively, trimming by high-voltage pulses can be applied. Types of resistor arrangements and trim possibilities are shown in Figure 9.37.

a)	b)	c)	d)
top or bottom layer post- or co-fired	**buried under top layer**	**buried under two layers**	**deep buried**

Trimming Possibility

Laser	**Laser through top layer**	**Laser through hole in the cover layers**	**High voltage pulse trimming**
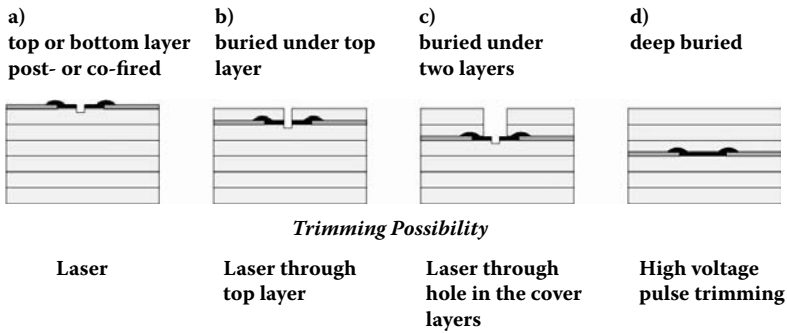
FIGURE 9.37
Types of resistor arrangements in multilayer or LTCC modules and their trimming possibilities.

9.4.1.3   Laser Trimming of Resistors

The short wavelength of Nd:YAG lasers (λ = 1.06 µm) allows small cut widths. The destruction of the resistive layer and the underneath is minimized. The laser beam energy is absorbed by the resistor leading to material heating, melting, and vaporization. The vaporized material must be removed by vacuum to avoid contamination of the circuit.

Laser cuts are formed by a series of overlapping spots (typical 25–50 µm diameter, 50–200 nsec). Short pulse duration together with a high peak power but low average laser power provides rapid vaporization with minimum heat flow into the resistor region. Thermal shocks are avoided and microcracking is minimized, thus resulting in better resistor stability. The laser-cutting parameters need to be optimized for each resistor paste to achieve the best results. Laser trimming requires contact pads to measure the resistance during trimming (Figure 9.38). Figure 9.39 depicts different shapes of cuts and the resulting change $\Delta R/R_o$ [37,38].

The fastest and most frequently applied trim shape is the Y-cut (Figure 9.39a). Because of the increasing trimming sensitivity and possible hot spots in the remaining resistor area, the trim length must not exceed 50% of the resistor width. If a wide linear trim range is required, hat resistors can be used. Better conditions are achieved with the L- or J-cut (Figure 9.39b1 and Figure 9.39b2). The J-cut is more stable because the trim kerf ends in the shadow area. Possible cracks do not deteriorate the resistance value. For high-voltage or high-frequency resistors, abrasive or shave cuts are applied. A mixed approach for both coarse and fine trimming is realized by the double-Y or shadow cuts (Figure 9.39d). The second cut with low trim sensitivity is made in the shadow of the first cut allowing very precise results. Serpentine cuts (Figure 9.39e) are used for large resistance changes. Digital cuts (Figure 9.39f) allow only discrete trim steps. However, the trimmed resistor is very stable because the cut is not in the current path.
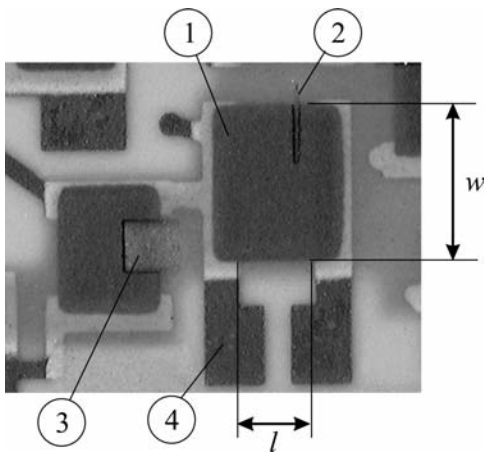
FIGURE 9.38
Photo of trimmed resistors: (1) termination, (2) Y-cut; (3) shave cut, (4) measuring contact pad
[37].
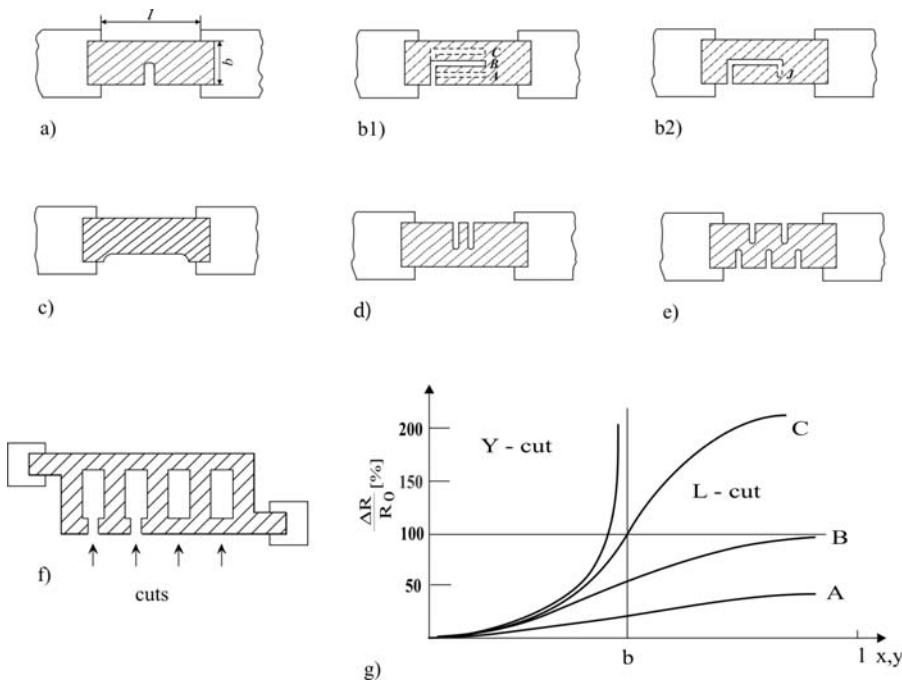
FIGURE 9.39
Types of resistor trim cuts: (a) Y-cut, (b1) L-cut, (b2) J-cut, (c) shave cut, (d) double-Y or shadow
cut, (e) serpentine cut, (f) digital cut, (g) principal trim behavior for Y- and various L-cuts.
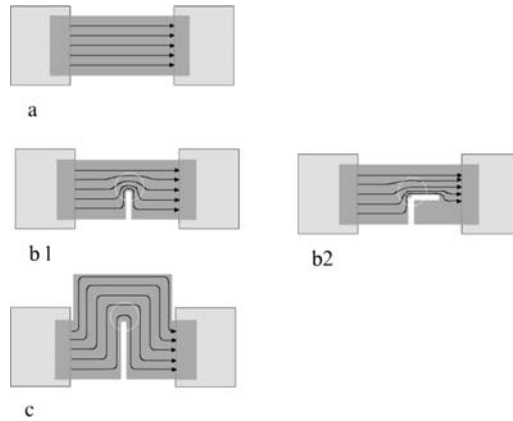
FIGURE 9.40
Current line distribution: (a) untrimmed resistor (homogeneous!), (b1) Y-cut (white circle: in-homogeneous, high density), (b2) L-cut (white circle: fewer inhomogeneous, lower density), (c) hat resistor (white circle: nearly homogeneous!).

The laser cut influences the electrical behavior and the stability of resistors. Owing to the current density at the end of cut (Figure 9.40), the power density is increased (hot spot). Such hot spots can produce microcracks, decrease the long time stability, and may even destroy the resistor. In addition, the power-dissipation density is reduced (design impact), and the noise is increased, especially if the laser power was too high.

9.4.1.4   Trimming of Buried Resistors

Resistors buried in LTCC are out of direct access. In general, the following three strategies of embedded resistor trimming are available ([39]; Figure 9.37):

1. Laser cutting with high power through one thin tape (Figure 9.37b)
2. Laser cutting through a preprocessed slot in the cover layer (Figure 9.37c)
3. High-voltage pulse trimming (Figure 9.37d)

The first method depends strongly on the tape thickness and the tape material used. Three to four cuts are often necessary to open the first layer (Figure 9.41). Sometimes, the resistance values of a test circuit are shifted
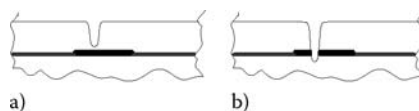
FIGURE 9.41
Phases of laser trimming: (a) open the cover layer (b) cut into the resistor.
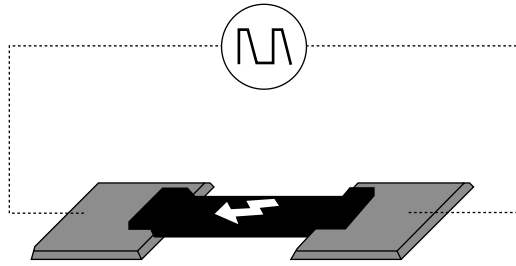
FIGURE 9.42
High-voltage pulse trimming of s.

negative again by an additional cut in the same kerf. With common laser equipment, it was very difficult to select the proper laser parameters for a clean smooth cut as required for a stable resistor [40].

The second method was investigated within the European project integrated buried capacitors and resistors (IBCAR) [41]. The resistors were placed on the second layer, and the first layer was provided with slots or cutouts, which were simply made with a punch tool during via formation. This process requires isostatic lamination to avoid material flow into the slots and to maintain an equal pressure distribution over the entire laminate (controlled shrinkage). The third method, high-voltage pulse (HVP) trimming of resistors, is based on internal discharges using both resistor terminations as electrodes for applying the high-voltage energy to the resistor body (Figure 9.42) [40,42–45,48]. This so-called pulse voltage-trimming method was introduced to adjust resistor values of TFRs from 10 $\Omega/\square$ to 100 k$\Omega/\square$. By applying an optimal dosage of electrical energy, it is possible to trim buried resistors without any damage of the resistor body or change in resistor geometry.

The general behavior of thick-film resistors (TFR) during HVP trimming depends on the resistance of the paste used:

1. Resistors with low sheet resistivities increase their value during HVP trimming (Figure 9.43a).
2. Resistors with high sheet resistivities decrease their value during HVP trimming (Figure 9.43b).

The pulse voltage-trimming sensitivity depends on the ink composition, especially the particle size and the mixing ratio of RuO_2 and glass frits [7,46]. Several commercial inks from various producers have been investigated and trimmed by HV pulses with a wide range of results.

During trimming of low-value resistors, a relatively high current flows through the resistor and heats up the conductive microstructures interrupting some of the weak conductive paths [42,44]. This process increases the resistor value of low-ohmic resistors.
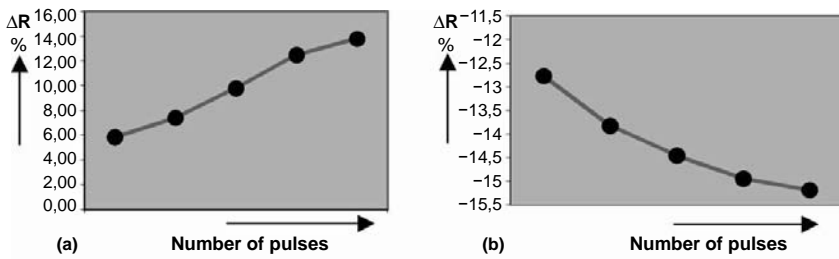
FIGURE 9.43
Trimming of resistors: (a) sheet resistance < 100 Ω/□, (b) sheet resistance > 100 Ω/□.

On the contrary, high-ohmic resistors are decreased by supplying electrical energy. With the same voltage applied, the resulting current is much lower. The electrical charge transport by high-ohmic resistor systems depends on the phenomena of tunneling and hopping conduction [7,47,48]. A few conductive paths may exist in a high-ohmic resistor system. Low electrical current causes low electrical energy and lower heating of microstructures. This amount of energy is not enough to interrupt conductive paths, which are responsible for an electrical charge transport. The different behavior may be explained by a resintering of microregions, which form new conductive paths. These additional electrical conductive paths increase the conductivity of the resistor and therefore decrease the resistance of a high-ohmic resistor. The dosage of electrical energy must be carefully controlled. Otherwise, the high electrical energy will damage the resistors. Again, the validity of the HVP method depends also on the physical composition of the resistors' pastes, the distribution of the microstructures inside the resistor, and the structure of glass matrix.

The main factor for adjusting resistor values is the energy of high-voltage pulses (EHVP). Excessive Joule heating in regions with a higher current concentration is avoided by using nanosecond pulses [43].

The efficiency of EHVP depends on the settings of the pulse parameters:

- Pulse amplitude v_i
- Pulse frequency f
- Number of pulses
- Type of resistor system

Experimental results point out that the energy supplied to the resistor and the resistor length is directly proportional. A possible setup for trimming by EHVP consisting of the following units was introduced [44,49] (Figure 9.44):

- HV-pulse generator — supply of HV pulses
- Ohmmeter — resistor value measurement before and after trimming
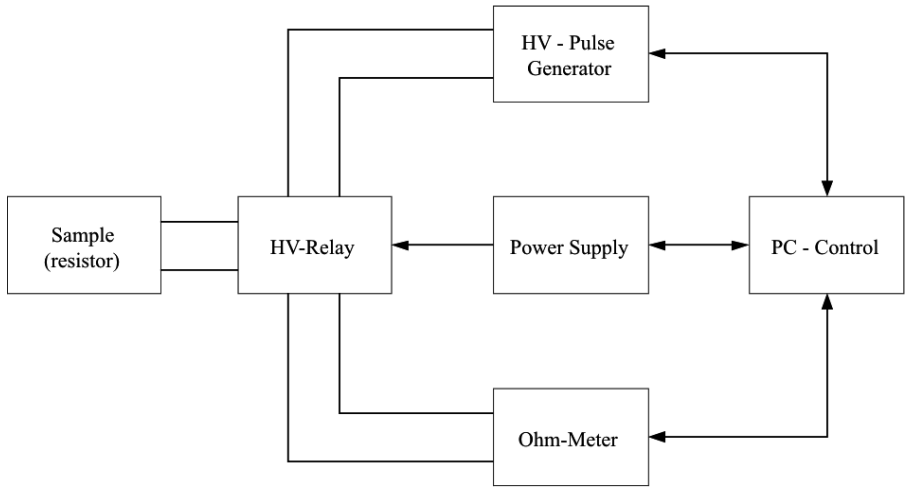
FIGURE 9.44
Setup of a EHVP trim system.

- HV relay — protection for ohmmeter
- PC — adjusting and controlling pulse parameters and trimming process (paste/parameter library)

The largest resistance change occurs at the beginning of trimming process with high voltage amplitude. This is a coarse-trimming mode, but on the contrary, there is a fine-trimming mode, which is executed by adjusting only the number of pulses, keeping the voltage amplitude and therefore the electrical energy constant. This constant electrical energy will be repeatedly supplied to the resistor and will change its value slightly.

The resistor performance like long-time stability or TCR does not depend only on the pulse voltage. The energy of the pulses must be carefully selected. Pulses with appropriate energy can act as an aging process. HVP-trimmed resistors often exhibit a better stability and TCR compared to untrimmed ones.

Advantages and applications of EHVP trimming method are:

- Possibility of trimming deep-buried resistors
- Downtrimming (for high-value sheet resistivities >10 kΩ/$\square$)
- Advantages for high-frequency application caused by decreased parasitic components without trimming cut
- Higher power capability (loss/mm^2) for trimmed resistors, caused by no trim cut and no decrease in resistor area
- Possibility of trimming microresistors (sizes < 100 μm × 100 μm)
- Improvement of TCR of several high-value resistors

TABLE 9.2

Comparison of Trimming Methods

Trimming Method	Advantages	Disadvantages/Limitation
Abrasive	Easy setup	Slow process
	Low costs	Dirty process
	Stable and low noise	Large cuts
		Decreased power density
Laser	High speed	Large investment
	Permits data logging	Intensive heat in trim area; possible
	Automated	cracks
	Relatively clean	Decreased power density
		Increased noise
		Reduced the long term stability
Energy of high-voltage pulses	Buried resistor trimming	High impact on layout.
	Downtrimming/uptrimming	Trim sensitivity of each ink must be
	Cut-free — no hot spots	derived by experiments
		Little experience available
		Hard and software development
		required

- Advantage for resistors on aluminum nitride (AlN) substrates (Laser cuts decrease the thermal conductivity of AlN in the region around the cut.)

A comparison of trimming methods [38] is shown in Table 9.2.

9.4.2 Capacitor Trimming

Capacitance variations associated with the manufacturing technology may not be tolerable for specific applications. Active tuning of circuit functions such as resonance frequency or filter response is necessary. Trimming by laser can be accomplished only if the component is located at the surface. Typically, capacitances will be reduced by trimming. Interdigital capacitors can be adjusted either continuously (Figure 9.45a) or in discrete steps (Figure 9.45b). The first method addresses the edge-coupling capacitance and is applied for fine-tuning. Mixing step- and continuous-trimming procedures lead to very fast and precise results.

a)   b)
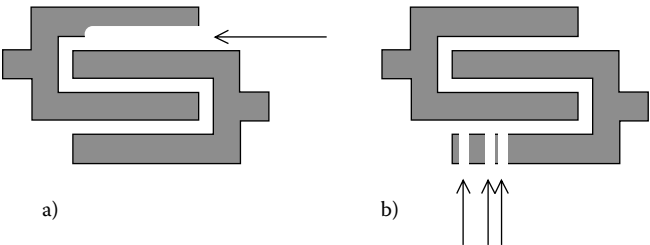
FIGURE 9.45
Trimming of interdigital capacitors: (a) continuous, (b) discrete.
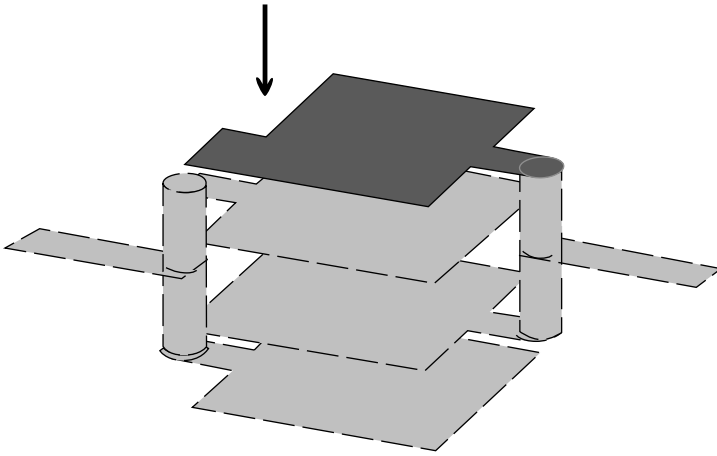
FIGURE 9.46
Trimming of plate capacitors by laser shaving.

a)   b)
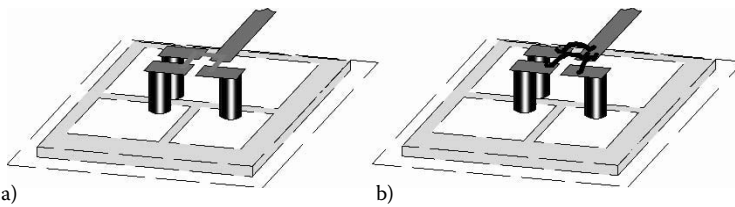
FIGURE 9.47
High-K-capacitor trimming.

Multilayer capacitors with the upper plate on the surface can be similarly trimmed. Large changes are obtained by separating an entire part of the plate. Small changes are achieved by shaving the edges (Figure 9.46). The upper plate area needs to be designed to allow the trim range required. In case of embedded high-K capacitors with typical tolerances of about ±15%, a second trimmable capacitor connected in parallel can be used for adjustment purposes.

Coarse trimming of high-K capacitors is possible by connecting a multi-structure electrode with separate vias (Figure 47a). Parts of the upper electrode can be separated by laser. Alternatively, the method can be applied if wire-bond technology is required for assembly (Figure 9.47b).

9.4.3   Inductor Trimming

Printed inductor structures can be adjusted by laser trimming. In general, three methods are possible. They are:

1. Increasing the inductor length
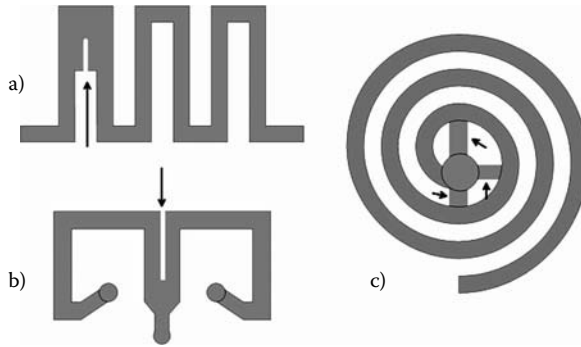
FIGURE 9.48
Trimming of inductors by increasing the effective current path.
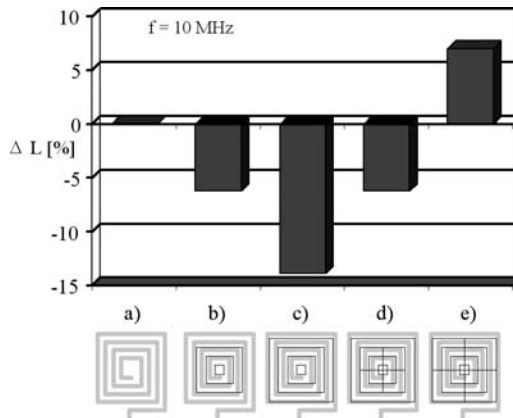
FIGURE 9.49
Inductor trimming by ground plane structuring with a laser.

2. Reducing the eddy current in ground plane structures
3. Tuning by bond wire inductances

The first method is based on increasing the effective electrical path by cutting into the conductor. It can be applied on meander and spiral type of inductors (Figure 9.48). The inductor is trimmed toward higher inductances.

The second method addresses the external mutual inductance of ground planes under inductors. By cutting certain shapes into the ground plane, it is possible to change the inductance value [50]. Figure 9.49 depicts a cut sequence. In steps b) and c, closed conductor rings were created. Their mutual inductance caused by eddy currents reduces the overall inductance of the rectangular spiral coil. Opening these rings reverses the effect, and the inductance becomes even larger than the initial value. This phenomenon is similar to a virtual increase of the distance to the ground plane. The sensitivity and trim range depend on the distance to ground. A close ground
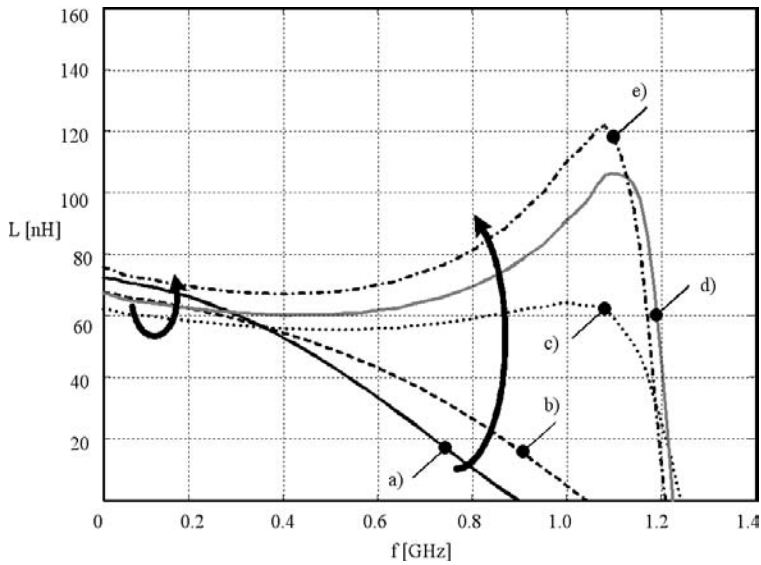
FIGURE 9.50
Impact of ground plane structuring on the frequency behavior of inductors (cut sequences are the same as shown in Figure 9.49).

plane allows large changes (up to 50%) whereas structuring of far-spaced ground planes offers only minor changes (<5%). Not only the inductance is trimmed, but also the RF characteristics are influenced as well. Figure 9.50 depicts both changes. The less the ground plane is active, the more the lumped element character dominates over the distributed one.

An alternative approach, which is very popular in microwave tuning, is based on the inductance of bond wires. Multiple wire bonds in parallel will reduce the inductance slightly compared to a single loop.

9.5 Lumped-Element Properties

9.5.1 Properties

9.5.1.1 Resistance Value

The resistance value of TFRs is defined by Equation 9.1 in Subsection 9.3.1. However, the termination that is overlapped by the resistor layer has an impact on the resistance (Figure 9.11). If silver-containing inks are used, the sheet resistivity changes owing to Ag-diffusion into the resistor body. The shorter the resistor, the more the diffusion influences the value of the resistor. This must be taken into consideration by introducing a correction factor in the design.

9.5.1.2   Thermal Characteristics

The TCR describes the change of resistance with temperature. For low-ohmic resistors, the TCR is positive, caused by the metallic conduction mechanism in the microstructure. For high-ohmic resistors, the TCR is negative, because of the semiconductor conduction mechanism. To avoid high TCRs, so-called TCR modifiers are added to the inks by paste manufacturers, assuring a low TCR over a wide temperature range.

Because the TCR is not linear in the temperature range of interest (typically, –55 to 125°C), it is divided into the ranges –55 to +25°C and +25 to +125°C (Equation 9.22 and Equation 9.23).

$$TCR_{\text{hot}} = \frac{R_{125} - R_{25}}{R_{25}\left(125°C - 25°C\right)} 10^6 \quad [\text{ppm/K}] \tag{9.22}$$

$$TCR_{cold} = \frac{R_{-55} - R_{25}}{R_{25}\left(-55°C - 25°C\right)} 10^6 \quad [\text{ppm/K}] \tag{9.23}$$

Standard TFRs show values smaller than ±100 ppm/K. In addition, the resistor's length-to-width ratio influences the TCR as well.

9.5.1.3   Voltage Stability

High voltages change the resistance value of TFRs. Beyond a certain limit, the changes are irreversible (see Subsection 9.4.1). Reversible changes are caused by self-heating effects (TCR) and the voltage-dependent conduction mechanism in the resistor. Ink data sheets specify the maximum voltage rating as the voltage that does change the resistance value less than 1%. For inks that are used currently, the values are typically between 50 and 100 V/mm.

9.5.1.4   Long-Time Stability

For trimmed and untrimmed resistors, data sheets normally specify for different aging conditions:

- Storage under temperature (1000 h at 125°C)
- Working under temperature (1000 h at power loss 5W/cm^2)
- Storage under humidity (1000 h at 85% air humidity and 85°C)

Typical resistor inks show long-time stability values of <0.2% for untrimmed resistors and <0.5% for trimmed resistors.

9.5.1.5 Noise Behavior

In TFRs, the current noise ($1/f$ behavior) dominates over the thermal noise. Current noise is caused by the conduction mechanism between the resistive particles in the microstructure. For noise characterization, the Quan-Tech noise measuring method is used:

$$NI\left[dB\right] = 20 \cdot \log \frac{U_r\left[\mu V\right]}{U_V} \qquad (9.24)$$

U_V = DC-voltage @ the power dissipation of 250 mW
U_r = procreated noise voltage in the defined frequency range

The noise index NI in dB is measured by a band-pass filter (bandwidth of 1 kHz between 618 Hz and 1618 kHz) [51]. A noise index NI = 0 dB corresponds to 1 μV noise voltage per 1 V DC voltage. For ruthenate-based TFRs, the noise index exhibits an increase proportional to the sheet resistivity and a decrease proportional to the resistor area [47,52].

9.5.1.6 Frequency Behavior

The frequency behavior of a TFR is influenced by layout (l/w ratio, shape), overall size, and material (conduction mechanisms inside [6]).

Over the used frequency range, a TFR shows a complex impedance $\underline{Z}$. It is influenced by geometrical dimensions (g) and by the conduction mechanism into the resistor layer (r) (Equation 9.25). For resistors with low sheet resistivities (<100 $\Omega/\square$), the imaginary part is inductive (Figure 9.51a); whereas with higher sheet resistivities (>100 $\Omega/\square$), it becomes capacitive (Figure 9.51b). For low and high sheet resistivities, the different RF behavior can be explained by the different conduction mechanisms [47,52,53].
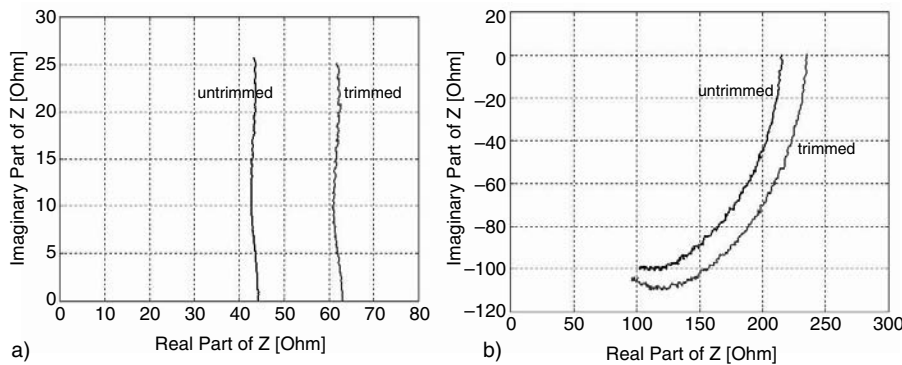
FIGURE 9.51
Frequency behavior DC to 3 GHz (Locus diagram) of buried resistors: (a) 10 $\Omega/\square$, (b) 100 $\Omega/\square$ (trimmed curve after high-voltage pulse trimming).

$$\underline{Z} = R + jX \cdot = function(R_g, R_r) + j\left[function(X_g, X_r)\right]. \tag{9.25}$$

Owing to the semiconductive behavior (hopping effect), the real part of high-ohmic resistor inks starts to decrease in relative low-frequency ranges (100 MHz to 1 GHz) by nearly $1/f$. Because of the material and geometrical impact, it is possible to obtain resistors with identical DC resistance but different RF behavior [54].

The equivalent circuit of printed resistors is shown in Figure 9.52 [53]. Depending on the sheet resistivity of the paste, the model will be simplified by omitting some elements. The capacitors C represent the influence of the ground plane. They are equal to the capacitance of a transmission line of identical dimensions (width, length, height above ground, etc.). Therefore, C reflects the equivalent line type (microstrip-like and stripline-like).

The parasitics are also responsible for the limited bandwidth of printed resistors. Their influence is, however, smaller compared to equivalent surface-mounted device (SMD) resistors.

9.5.2   Capacitor Properties

9.5.2.1   Capacitance Value

Capacitors are reactive elements. The impedance of an ideal capacitor contains only an imaginary part (Equation 9.26). The capacitance is determined by material (permittivity) and design parameters.

$$\underline{Z} = \frac{1}{j\omega C} \quad \text{or} \quad \underline{Y} = j\omega C \quad \text{with} \quad \omega = 2\pi f. \tag{9.26}$$

9.5.2.2   Capacitor Model

Real capacitors are equivalent to a series resonant circuit as shown in Figure 9.53. The model is valid for both interdigital and plate capacitors. The self-resonance effect is caused by parasitic series inductance L_s of the electrodes and connections such as conductor traces or vias. The series resistance of the electrode metal R_s and the dielectric losses (expressed by the parallel resistor R_p) in the tape or high-K material are contributing to the capacitor loss. To simplify the model, both parts can be combined in the equivalent series resistance R_s.

9.5.2.3   Self-Resonance Frequency

The frequency in which the series resonant circuit changes from capacitive to inductive behavior is called the *self-resonance frequency* (Equation 9.27). At this frequency, the imaginary part of the impedance is zero. Because the
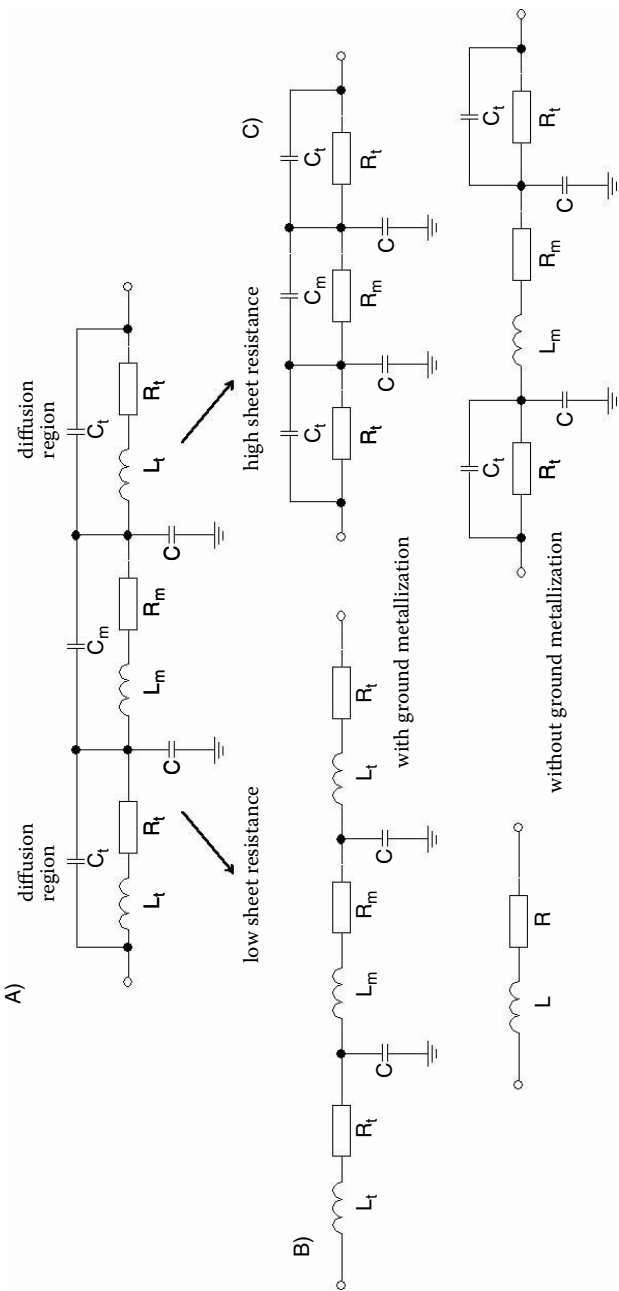
FIGURE 9.52
(a) General high-frequency model (equivalent circuit) of a printed resistor, (b) high-frequency model for low-ohmic resistors, (c) high-frequency model for high-ohmic resistors.
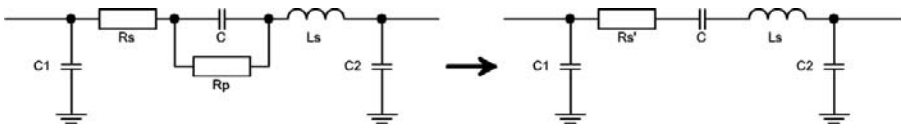
FIGURE 9.53
Model of printed capacitors in series.
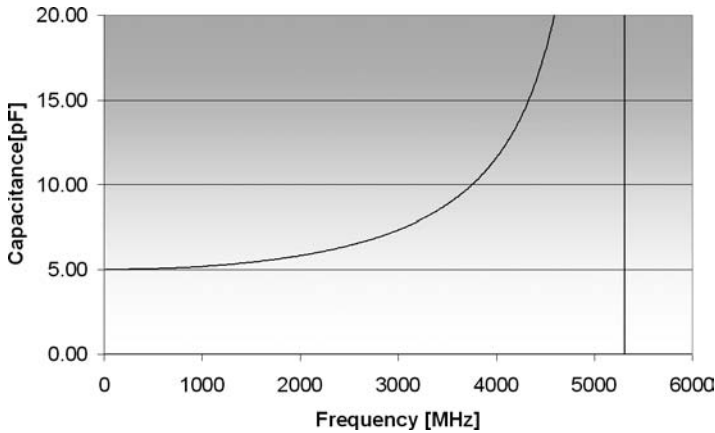
FIGURE 9.54
Capacitance vs. frequency for a typical capacitor.

capacitance value shows an increase up to the resonance frequency
(Figure 9.54), it is desired to reduce the parasitic inductance to the lowest
value possible.

$$f_s = \frac{1}{2\pi\sqrt{L_s \cdot C}} \tag{9.27}$$

Parasitic inductances are mainly caused by design. Figure 9.55 shows an
example of a shunt high-K capacitor with two different via connections. By
using parallel vias, the via-related inductance can be reduced and the reso-
nance frequency can be increased [28].

9.5.2.4   *Quality Factor and Loss Tangent*

The dielectric loss tangent or dissipation factor is a material property char-
acterizing the loss behavior of the dielectrics itself. It is defined as follows:

$$\tan\delta = \frac{1}{Q_d} \tag{9.28}$$
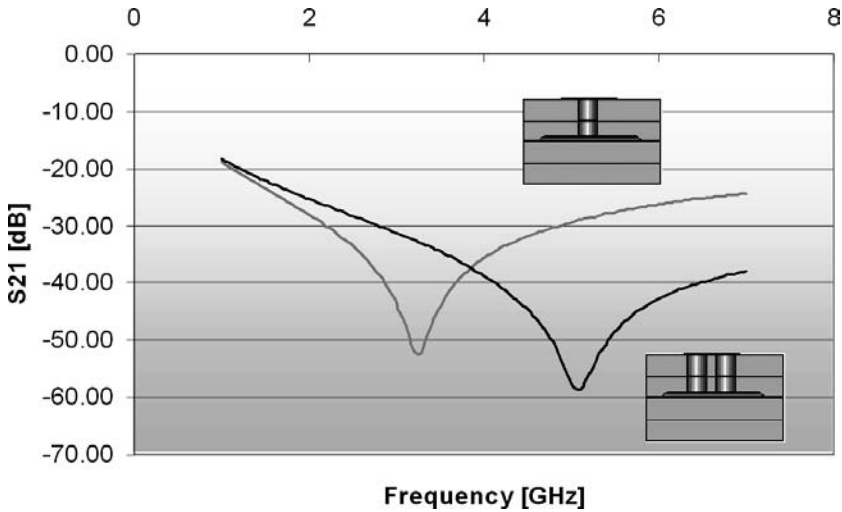
FIGURE 9.55
Self-resonant behavior of high-K capacitors with two different via connections (capacitance about 50 pF).

where Q_d denotes the quality factor of the dielectrics. Typical tan δ values for LTCC tapes are between 0.001 and 0.005. High-K materials usually have higher dissipation factors and show a stronger frequency dependency of tan δ (increasing dielectric losses with frequency) [35].

The overall quality of a capacitor can be determined using Equation 9.29. Q_s represents the conductor loss in the electrodes.

$$\frac{1}{Q} = \frac{1}{Q_d} + \frac{1}{Q_s} \ . \tag{9.29}$$

For a capacitor according to Figure 9.53, the quality can be calculated using the following:

$$Q = \frac{\left(\dfrac{1}{\omega C} - \omega L_S \right)}{R_S{}'} \ . \tag{9.30}$$

The quality is highest at low frequencies and it drops down to zero at the resonance point (Figure 9.56).

9.5.2.5 Breakdown Voltage

The breakdown voltage is a dielectric-material-related parameter. Typical values for LTCC is >1000 V/mil. Printed high-K capacitors have a rather
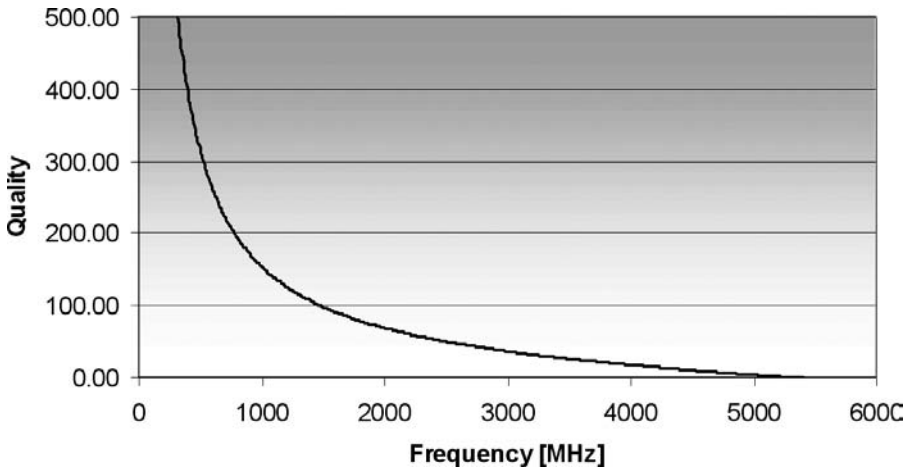
FIGURE 9.56
Quality factor vs. frequency for a capacitor.

thin dielectric layer (about 25 μm). Measured breakdown voltages for a capacitor material embedded in LTCC are in the range from 600 to more than 1200 V.

9.5.2.6 Temperature Coefficient of Capacitance (TCC)

The temperature sensitivity of the material permittivity causes capacitance changes with temperature. The TCC is defined as follows:

$$TCC\left[ppm\ /\ K\right] = \frac{\Delta C}{C_{25°C}} \cdot \frac{1}{\Delta T} \cdot 10^6 \tag{9.31}$$

Dielectric materials are classified according to their temperature suscepti-bility. Alumina and LTCC are very stable and belong to the class I materials. High-K materials show a higher temperature dependency (class II). Figure 9.57 depicts the capacitance vs. temperature for a printed high-K capacitor embedded in LTCC.

9.5.3 Inductor Properties

9.5.3.1 Inductance Value

Ideal inductors act as a pure reactance directly proportional to the frequency (Equation 9.32). They cause a current–voltage shift of 90° in an electrical circuit. The inductance value is influenced by design and material param-eters as described earlier.

Change of Capacitance Related to C @ 21°C
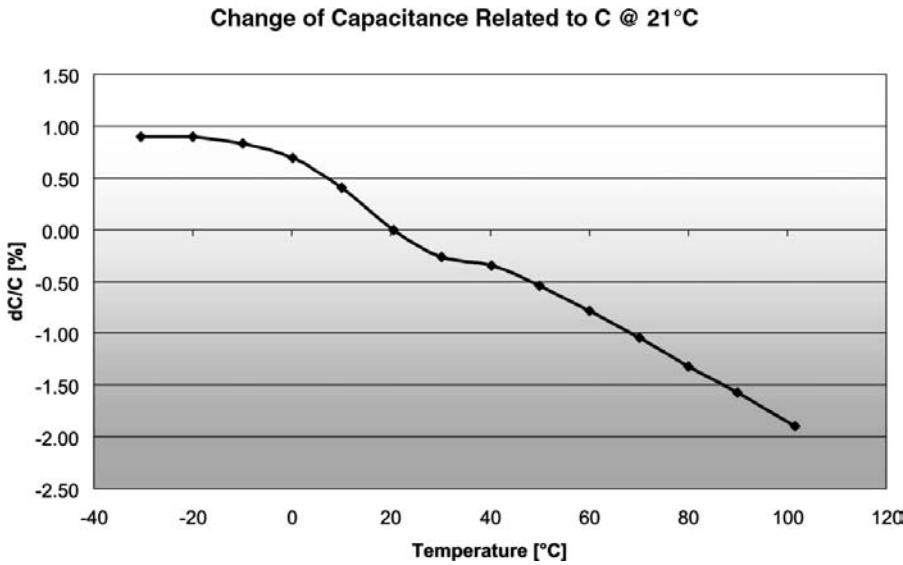
FIGURE 9.57
Capacitance vs. temperature for a high-K capacitor (ε_r about 60).

$$\underline{Z} = j\omega L \ . \tag{9.32}$$

9.5.3.2 Series Resistance

Because real coils will always exhibit ohmic losses, the phase shift will not be completely 90°, as shown in Equation 9.33:

$$\underline{Z} = R + j\omega L \ . \tag{9.33}$$

The real part of the impedance is not constant vs. frequency. The resistance is determined by the following:

- Specific resistivity of the paste material ρ
- Conductor cross section
- Skin effect
- Proximity effect
- Eddy current in a ground plane

With increased frequency, the current flow is more concentrated on the surface of the conductor trace (skin effect). The thickness δ where the current density has dropped down to 1/e (approximately, 36%), in comparison to the DC current density, is called the *skin depth*. The skin depth is only related to material constants and to the frequency by Equation 9.34.

$$\delta = \frac{1}{\sqrt{\pi \mu f \kappa}} \qquad (9.34)$$

with $\mu = \mu_0 \cdot \mu_r$ (effective permeability) and $\kappa = {}^1/_\rho$ (specific conductivity).

To simplify the calculation of the AC resistance of conductors, the entire current is supposed to flow within the skin thickness δ (Equation 9.35):

$$R_s = \frac{1}{\delta \cdot \kappa} = \sqrt{\pi \mu f \rho} \quad [\Omega]. \qquad (9.35)$$

Printed conductors have a cross section that depends on various process parameters (paste properties and printing parameters). Because of internal field distribution, flat conductors exhibit a current concentration on the edges. This effect is included by the form factor C_f [55,56]:

$$R(f) = C_f \cdot \frac{l \cdot R_s(f)}{2(w + t)} \qquad (9.36)$$

$$C_f = 1.0483 + 0.2176 \cdot \ln\left(\frac{w}{t}\right) + 0.7717 \cdot e^{-\frac{w}{t}} \qquad (9.37)$$

valid for $1 \le w/t \le 100$ (Figure 9.58).

9.5.3.3   Lumped Inductor Model

Lumped inductors in series connection are usually described by the π model as shown in Figure 9.59. The shunt capacitors depict the parasitic capacitances of coil windings to ground. Capacitive coupling between windings cause the self-resonance frequency f_p, as shown in Equation 9.38. Because of increasing effective inductance values in the vicinity of a parallel resonance, the inductors can only be used far below the self-resonance frequency (Figure 9.60).

l - length
w - width
t - thickness
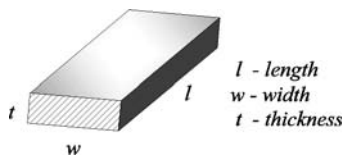
FIGURE 9.58
Ideal conductor cross section.
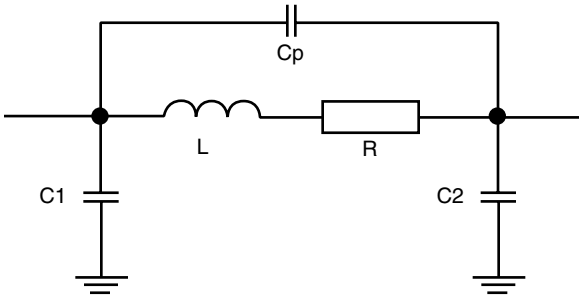
FIGURE 9.59
Lumped inductor-model.
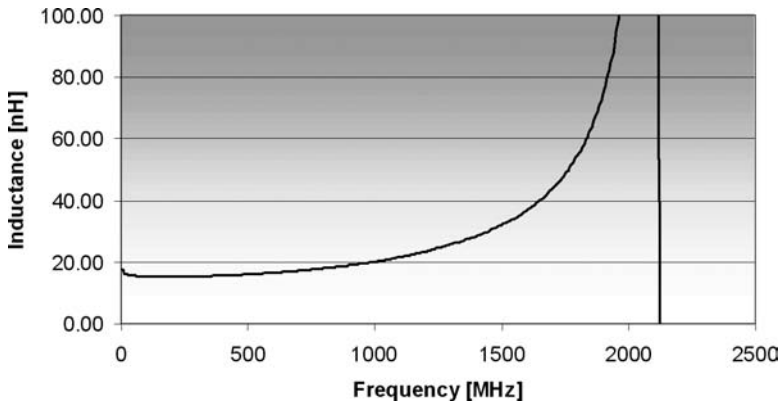
FIGURE 9.60
Inductance vs. frequency and self-resonance behavior for a lumped inductor.

$$f_p = \frac{1}{2\pi\sqrt{L \cdot C_p}} \tag{9.38}$$

The simple inductor model is valid up to the first resonance only. Second-order effects are not considered in this description. Figure 9.61 shows measured and simulated S-parameters of a three-dimensional LTCC inductor. If effects above the first resonance need to be included, a more sophisticated model needs to be established.

9.5.3.4 Quality Factor

The more frequently used parameter to describe the loss behavior of coils is the quality factor. Several definitions are available in the literature [57]. The *quality factor*, in general, is defined as the ratio between the imaginary part and the real part of the impedance (Equation 9.39):
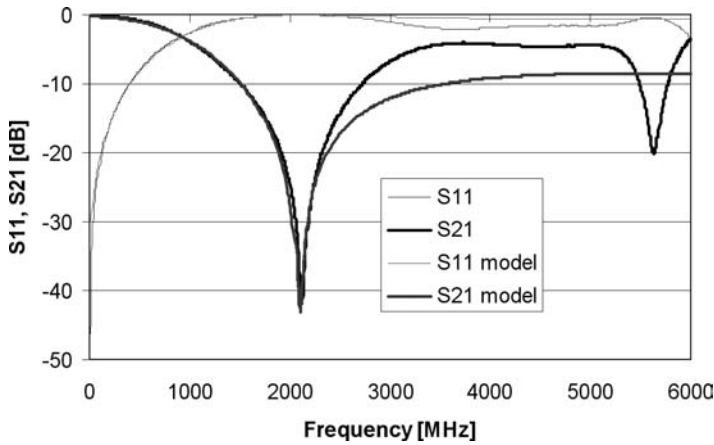
FIGURE 9.61
Comparison of measured and simulated S-parameters using the lumped Π-model.

$$Q = \frac{\mathrm{Im}\left\{\underline{Z}\right\}}{\mathrm{Re}\left\{\underline{Z}\right\}} \tag{9.39}$$

$\underline{Z}$ = impedance of the coil.
Applying the π model from Figure 9.58, the quality factor becomes:

$$Q = \frac{\omega L(1 - \omega^2 LC_p) - \omega CR^2}{R} \tag{9.40}$$

The quality factor is frequency dependent and is applicable to lumped coils only (Figure 9.62). Inductors that are not small compared to the signal wavelength reveal line transformation effects. The resulting quality factor derived from measured S-parameters appears to be negative.

9.5.3.5 High-Frequency Properties of Printed Inductors

Two frequency ranges are of interest in inductor characterization. The low range from kHz to about 100 MHz is dominated by the skin effect. The inner self-inductance virtually drops down to zero. The inductance value determined at high frequencies differs considerably from the value measured at a low frequency (Figure 9.63). The inner self-inductance is reduced by the square root of the frequency. Wider lines show a more significant inductance drop [35] compared to smaller lines.

The higher frequency range (*f* >> 100 *MHz*) is mainly determined by parasitics in the design; in particular, the ground plane influences the inductor character. A close ground plane may result in higher ground capacitances and, subsequently, a distributed behavior.
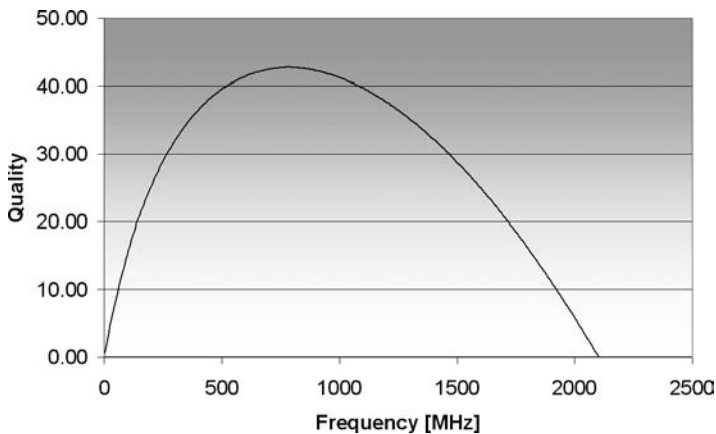
FIGURE 9.62
Quality factor for the lumped three-dimensional inductor according to Figure 9.59.
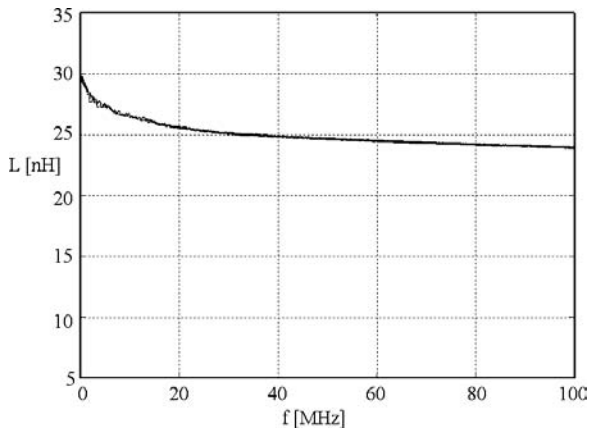
FIGURE 9.63
Inductance value vs. frequency for a rectangular spiral coil ($n = 3.5$, $f_s = 1$ mm, $w = 0.2$ mm, $s_m = 0.7$ mm, without ground plane).

If the interturn capacitance dominates (no ground plane or large distance) one or more resonances will appear (Figure 9.64a). With a full ground plane under a series-connected flat spiral inductor, a linelike character as shown in Figure 9.64b will appear. Three-dimensional inductors tend to be lumped owing to the self-shielding effect of the windings from the effect of the ground plane.
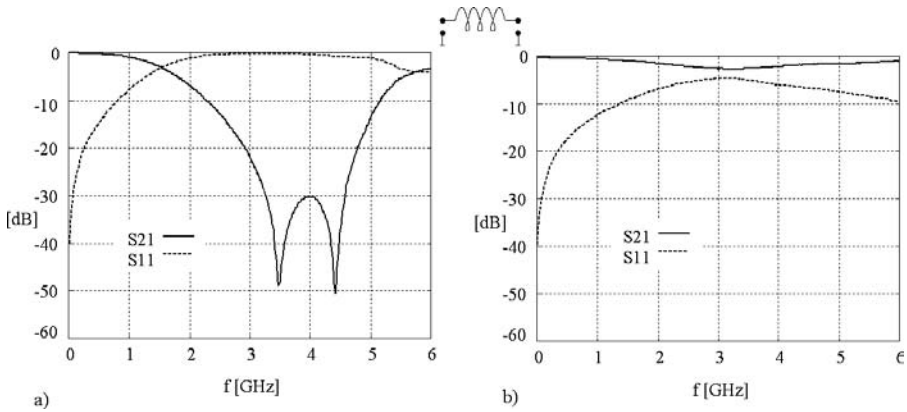
FIGURE 9.64
S-parameters of an inductor with: (a) lumped, (b) distributed behavior (both inductors have the same inductance value of 9.6 nH).

9.6   LTCC-Integrated Passive Devices

9.6.1   Concept of Passive Integrated LTCC Modules

Integration of passives in LTCC is also used to build components. Several elements can be combined in a multilayer structure to achieve a specific electrical function (e.g., a band-pass filter). These small-sized components have terminations allowing surface-mount assembly operations (land grid, castellation, or ball grid array [BGA]). Depending on the nature of these passive multicomponent devices, they are referred as *monolithic* (only LTCC elements) or *hybrid* [58] (mixture of embedded components and additional surface-mounted elements). Reasons for not implementing all passives in the hybrid type are:

1. Inductors or capacitors might be outside the useful integration range.
2. Area or number of layers required will be too large (costwise).

Hybrid filters are therefore a trade-off between scale of integration (module size), costs, and performance. Figure 9.65 shows an example of a hybrid design. If combined with active elements, tunable filters, or fully functional systems, or SiPs can be realized [59]. A very popular example is Ericsson's Bluetooth module.

The major advantage of the hybrid LTCC filter concept is the cost efficiency for small and medium volumes combined with a high scale of integration. Designs can be tailored to the specific application and produced on typical
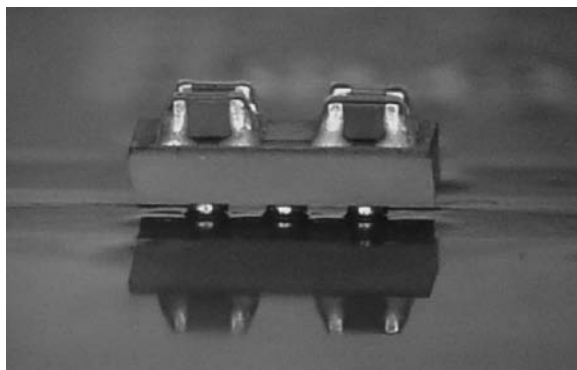
FIGURE 9.65
Hybrid LTCC filter (8-layer LTCC).

LTCC manufacturing lines. The layer count of the LTCC substrate is low compared to monolithic LTCC filters, which typically consist of many thin LTCC layers. Thin-tape processing requires special handling tools, which are not necessary for standard thicknesses (100–250 µm). Monolithic LTCC filters, on the other hand, are manufactured by several component suppliers for standardized applications in huge volume. With the high volume, the component prices are low.

9.6.2 Design of LTCC Filter Modules

An introduction to module design may be best illustrated through an example of a hybrid filter with passive surface-mount components on the upper side of the LTCC and a BGA interconnection on the lower side of the substrate [58]. The BGA package allows testing of the filter and easy assembly on the system board. Owing to the small dimensions, underfill is not required to achieve highly reliable interconnections. To allow automated pick and place, the SMDs are covered with a planarized glob top or overmolding compound (Figure 9.66). According to measurement results, the glob-top material influences the electrical performance at frequencies below 3 GHz only slightly [60].

Based on the system specification, a filter schematic is developed. A first sensitivity analysis (influence of component tolerances on the function) should be made to verify the manufacturability in general. Another technology-independent method uses typical parasitics, which are added to the schematic (e.g., capacitor with parasitic inductance or quality factor of an inductor). Both methods help to decide which filter type will perform best if several schematic structures are available.

Next, the schematic is divided into components to be and not to be realized in LTCC. This step is not necessary in the design of monolithic LTCC devices. After partitioning, the fine design of embedded components is done. There are many parameters that can be adversely varied, such as plate area vs.
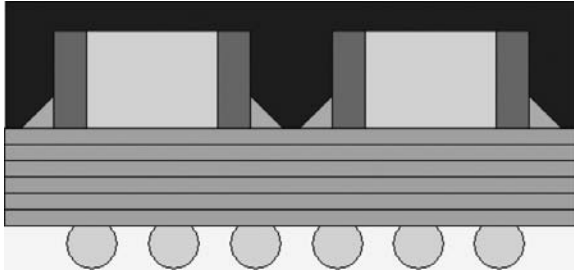
FIGURE 9.66
General construction of a hybrid filter.

number of layers for a capacitor, or number of turns vs. coil radius for
inductors. Optimization of these designs can be either driven by size con-
straints or costs (e.g., number of layers). The physical dimensions of each
component are obtained by using the following approaches:

- Closed-form or semiempirical equations [61]
- Known devices (component library)
- Parametric models [62]
- Electrical field simulations on predefined structures

A library with measured or simulated electrical parameters helps to reduce
the design time and increases the confidence in the design. New components
should be optimized or verified by a three-dimensional electrical simulation
until they show the correct behavior.

The designed LTCC components are arranged according to their intercon-
nections. Symmetries in the schematic should also lead to symmetries in the
placement to obtain equal conditions. The results allow a rough placement
study and size estimation (outline and number of layers). If the area of the
module is much larger than the area for the SMDs on top, some of the large
integrated components should be changed to an SMD type to get an opti-
mum in module size. The full design flow including electrical filter synthesis
is shown in Figure 9.67.

Finally, a module simulation including electrical models of the SMDs,
embedded components, wiring, and the module interface (e.g., solder
bumps) helps to find out possible problems due to parasitic cross-coupling
effects [63]. The internal elements can be modified to compensate these
effects. It might be even necessary to increase the distance between compo-
nents or to change their physical dimension. Process or material tolerances
are used to assess repeatability and manufacturability (Figure 9.68).
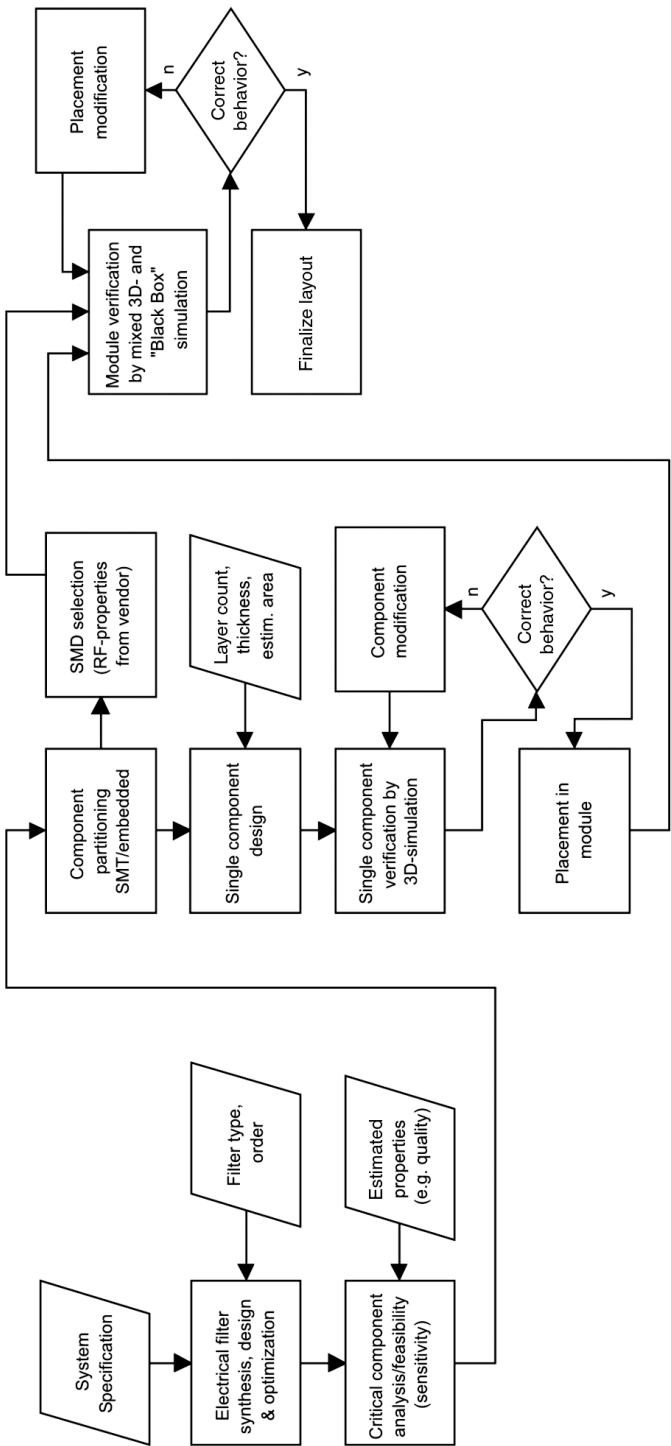
FIGURE 9.67
Design flow for hybrid RF filters in LTCC.
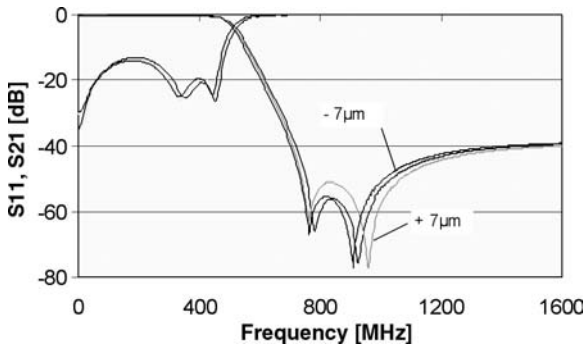
FIGURE 9.68
Influence of tape-thickness variation on the frequency response for a harmonic filter.

9.7   Distributed Elements

For microwave frequencies, passive integration is not limited to the lumped passive components mentioned in the preceding text. Structures made of line elements are used to create filters, resonators, couplers, etc. Depending on the line type chosen, these structures are on the surface (microstrip line) or embedded between ground planes (stripline). The latter provides reduced interactions with neighboring components because of the complete shielding. The size of these components is related to the signal wavelength. For frequencies above 20 GHz, such filters become small [58].

Components constructed of an arrangement of transmission lines and line sections, which are in the size of the signal wavelength, are called *distributed elements*. Their properties are based on the behavior of transmission lines. Wave impedance, unit line capacitance as well as inductance, and loss contributions are major design-relevant features. Because of the ratio of the line length to wavelength, these passive structures are applied for RF and microwave devices only. At lower frequencies and subsequently long wavelengths, cost and size will not meet the requirements of modern microelectronic systems.

Both thin- and thick-film technology allow planar microstrip or coplanar transmission lines. However, requirements on line and coupling-gap accuracy do not always permit traditional screen printing. Etching techniques or photosensitive paste systems offer a potential solution. LTCC provides more design freedom. Impedance-matched line transitions (e.g., from microstrip to stripline or to an embedded waveguide) are possible.

9.7.1 Materials and Technology

The material and the technology applied are similar to lumped-element design. Silver- or gold-based conductor systems offer the best conductivity. In general, the conductor loss dominates the loss behavior of LTCC-based elements. However, at frequencies above 10 GHz, the dielectric loss cannot be neglected. Because distributed elements are usually designed for microwave frequencies, the dielectric loss becomes more important. Losses in the dielectrics and in the conductive lines have a direct influence on filter selectivity and attenuation. Typical structures are based on the half or quarter wavelength. The size of these elements is inversely proportional to the square root of the permittivity. For lower or medium frequencies, higher K-values are necessary to shrink the designs. Several LTCC suppliers are developing materials that have a medium permittivity together with a low dissipation factor (Figure 9.69) [25].

9.7.2 Design Methodology for Distributed LTCC Components

Because of the complexity of designing multilayer distributed elements, only a general description can be given. The design methodology for filter design is shown in Figure 9.70. Based on the specifications of bandwidth, 3-dB frequencies, insertion loss, etc., the synthesis of the distributed filters is performed using software tools. The topology of the filter needs to be chosen to allow easy implementation and integration in LTCC technology (e.g., combline or hairpin). The number of poles and the transformation functions
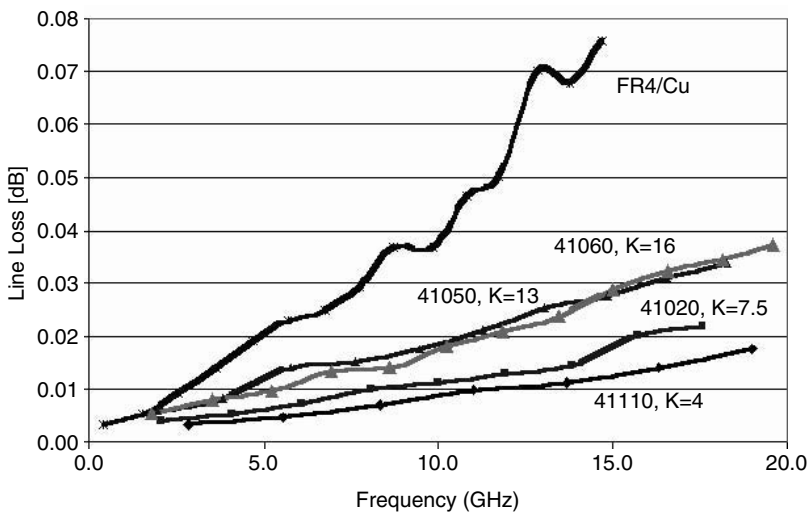
FIGURE 9.69
Comparison of the loss behavior of different LTCC materials. (Courtesy of ESL.)
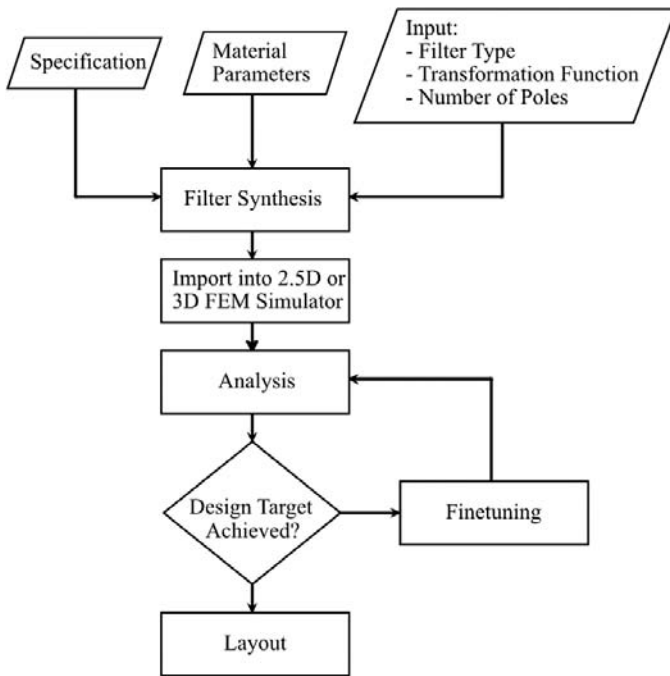
FIGURE 9.70
General flow for LTCC distributed filter design

(Chebychev or Elliptic) are to be defined to meet the specifications. Additionally, technology-relevant information such as layer thickness and permittivity are required.

The design proposal should be verified prior to manufacturing using a simulation tool, which is even possible on complex designs [64]. This 2.5- or 3-D electromagnetic simulation helps to predict manufacturability (yield) and tolerances based on technology-related variations such as line widths, layer thickness, and permittivity. Furthermore, the real boundary conditions of the component are included in the simulation. Fine-tuning of the layout may be necessary to account for fringing fields or other parasitics.

An important parameter for multilayer design is the stacking tolerance. It characterizes the layer-to-layer alignment. Typical deviations are in the range of ±30 μm. This might be critical for the position of edge-coupled lines. A practical solution is suggested in Reference 22 (Figure 9.71). Instead of using a straight line, two line segments are applied. A relative shift between layers leads to a higher coupling in one segment; but on the other hand, a lower coupling factor is achieved on the second segment. The overall coupling factor is kept almost constant; whereas in the conventional design, the coupling factors vary with position.
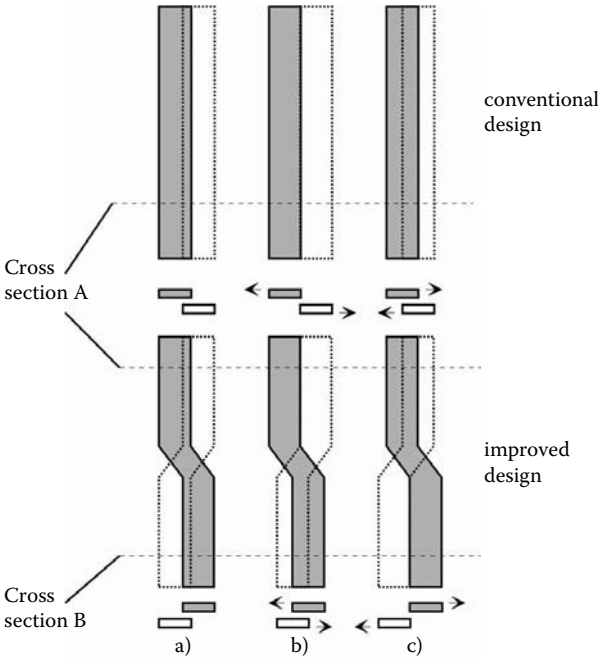
FIGURE 9.71
Design compensation of layer-to-layer misalignment for edge-coupled lines.

9.7.3 LTCC Line-Filter Design Example

An example for a filter design is given in Reference 58. Because of the considerably low working frequency of the UMTS (Universal Mobile Tele-communication System)-filter (about 2 GHz), a combline topology was chosen to achieve a small filter size. Figure 9.72 shows a drawing of the filter without external ground planes.

After optimization with an electromagnetic simulator, filters were manufactured using DuPont Tape 951. Silver metallization was applied for lowest conductor losses. Top and bottom ground plane metallization was Ag–Pd (for solderability). Multiple ground and signal interconnections were achieved with an array of solder bumps (BGA). Figure 9.73 depicts the LTCC filter element with the dimensions $14 \times 9 \times 3$ mm (14 layers).

A slightly higher attenuation was obtained in the pass band of the realized filter. This might have been attributed to the higher sheet resistivity of Ag–Pd on the top and bottom ground layers. However, the overall prediction of the filter behavior was in good agreement with the test results (Figure 9.74).
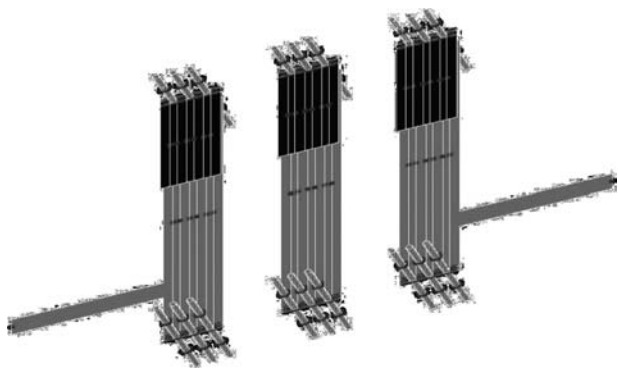
FIGURE 9.72
Combline-filter structure (top and bottom ground planes not shown).
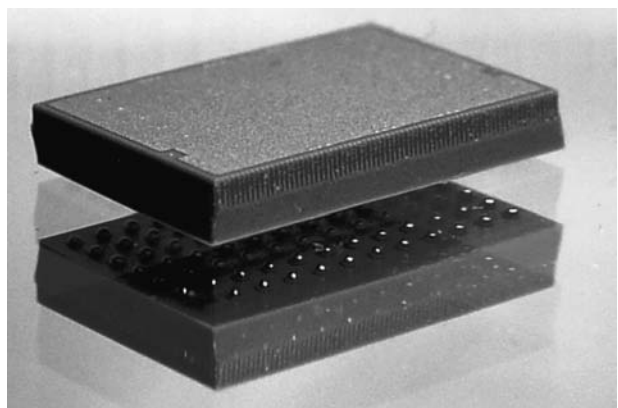
FIGURE 9.73
LTCC filter as a ball grid array.
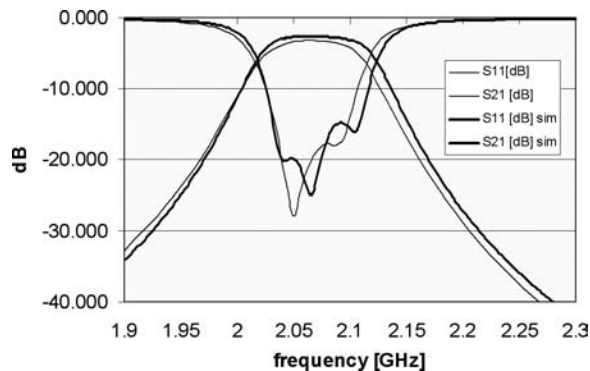
FIGURE 9.74
Comparison between simulated and measured frequency behavior of the combline filter.

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